ST7123

Datasheet

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LIST OF CONTENT

1   GENERAL DESCRIPTION

The ST7123 is a System-on-Chip (SoC) driver LSI designed for TFT LCD controller with a build-in touch panel controller and suitable for small to medium size portable devices such as mobile phone or tablet. ST7123 can support up to 720RGBx1680 (HD) dots panel and support 16,777,216-color. There is no internal RAM in ST7123. The 720-channel source driver has true 8-bit resolution, which generates 256 Gamma-corrected values by an internal D/A converter.

The ST7123 incorporates with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver. The built-in timing controller in ST7123 can support MIPI interface and included 4-lane/1-port display serial interface with low EMI noise and touch protocol via standard integrated circuit bus(I^2C) or serial peripheral interface(SPI). The ST7123 also supports a standby mode for power control consideration. For further power control, the dynamic backlight control function basing on displaying image content is also supported.

2 FEATURES

- Single-chip HD Amorphous TFT Controller/Driver.

- Display Resolution

■ 720RGB x 1680dots

- Display Modes (Color Mode)

■ Full Color: 16M, RGB=(888) max. Idle Mode Off

■ Color Reduce: 8-color, RGB=(111), Idle Mode On

- System Interfaces

■ MIPI DSI: MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01)

- Display Features

■ Outputs 256γ-corrected values using an internal true 8-bit resolution D/A converter to achieve 16,777,216 colors

■ Supports CGOUTR[1:22]/CGOUTL[1:22] GIP control signal

■ Individual gamma correction setting for RGB dots(1 analog/ 3 digital gamma)

■ Supports column/1-dot/2-dot/4-dot inversion

■ Power saving mode (standby mode)

■ Supports low frame rate mode

- Built-in Color Image Processing Functions

■ Support WB function

■ Support CDC function

■ Color enhance (CE 2.0)

◆ Sunlight Readability Enhancement (SRE)

◆ Sharpness Enhancement

◆ Hue adjustment

◆ Contrast Enhancement

■ Content adaptive brightness control (CABC 2.0)

- On Chip Function

■ Support VCOM ground level driving scheme

■ Internal oscillator for display clock generation

■ Timing controller

■ Built–in NVM to store VCOM/GVDD calibration and ID1~ID3

■ Built–in NVM to store analog gamma, digital gamma and color enhancement.

■ Built–in NVM to store panel timing, analog power setting, and etc.

- Supply Power Range

■ Logic power supply voltage (IOVCC): 1.65 ~ 1.95V

■ Positive analog power supply voltage (AVDD): 4.5 ~ 6.3V

■ Negative analog power supply voltage (AVEE): -4.5 ~ -6.3V

– Touch Feature

- Multi-touch coordinate sensing without ghost points

- 16-bits MCU optimized for capacitive sensing and other human interactions

- Supports up to 18x32 electrodes to provide the highest possible accuracy

 ◆ Scanner drive horizontal/vertical VCOM

 ◆ 64 analog front ends (AFEs) supports up to 576 receiver pads

- Supports I2C and SPI protocol for communication with the host

- 6 virtual button support

- Support passive stylus

- Support proximity

- Hopping frequency range from 50kHz to 120kHz to minimize noise interference

- High signal- to noise ratio (>50dB SNR) touch AFE enables

- Wake-up gesture

- Touch FW host download

– Optimized Layout For COG Assembly

– Operating Temperature Range: –30ºC to +75 ºC

3 BLOCK DIAGRAM

3.1 Block Function
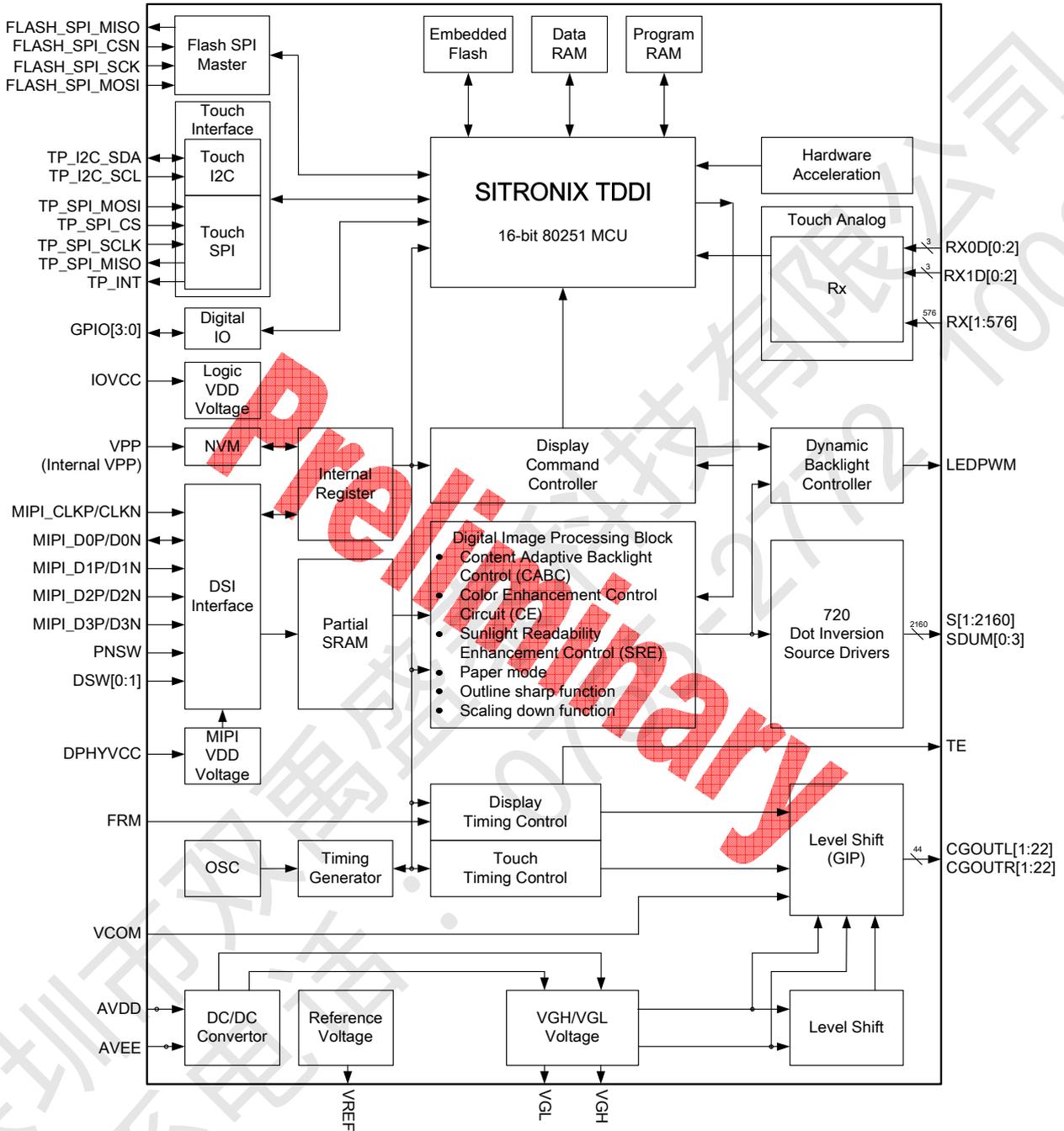
4 PIN INFOMATION

4.1 Pad Arrangement

4.1.1 Output Bump Dimension

Au bump height	9μm
Au bump size	24μmx90μm
	Pad1 to Pad813
	15μmx100μm
	Pad814 to Pad4091

ST7123
Face Up
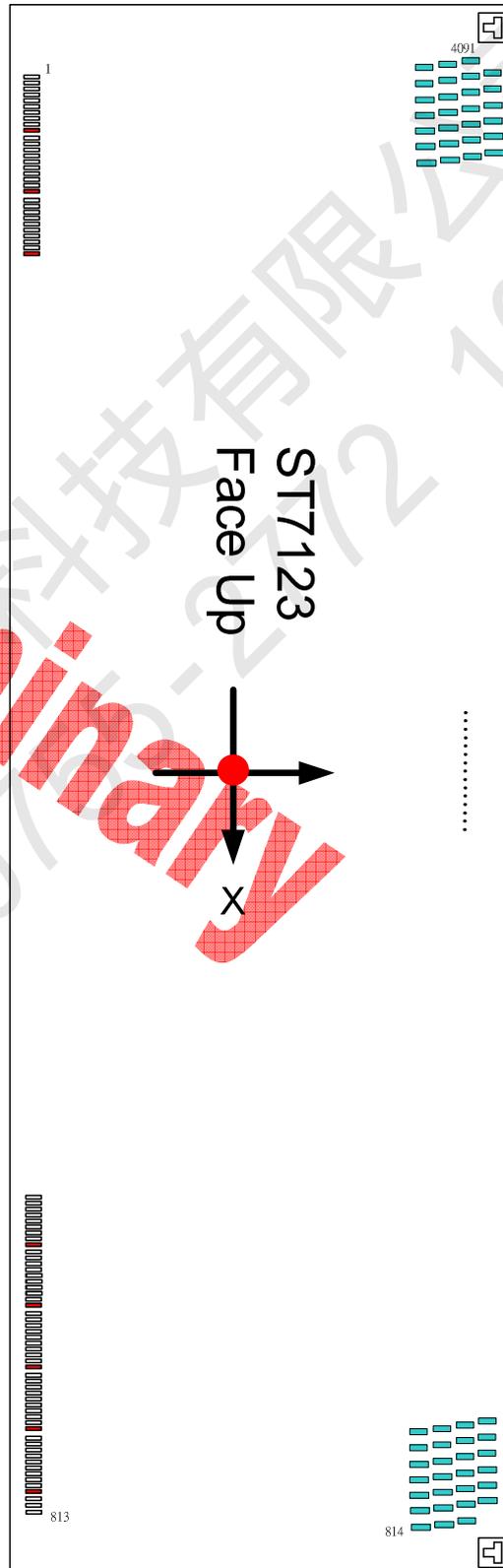
4.1.2   Bump Dimension

● **Output Pads**

Pad No. 814 ~ 4091
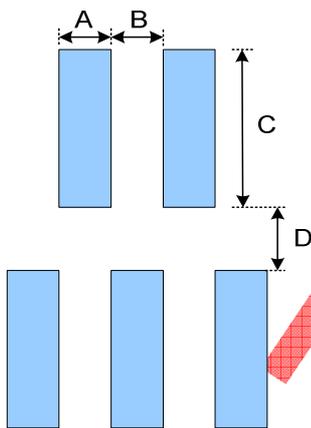
Symbol	Item	Size
A	Bump Width	15 um
B	Bump Gap 1 (Horizontal)	24 um
C	Bump Height	100um
D	Bump Gap 2 (Vertical)	20um

● **Input Pads**

Pad No.1~813
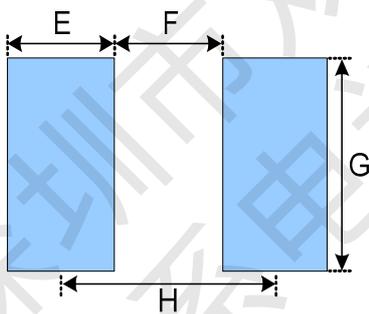
Symbol	Item	Size
E	Bump Width	24 um
F	Bump Gap	16 um
G	Bump Height	90um
H	Bump Pitch	39 um

4.1.3 Alignment Dimension

● **Alignment Mark Left: L(X,Y)=(-15969.4, 440.5),   Unit: um**
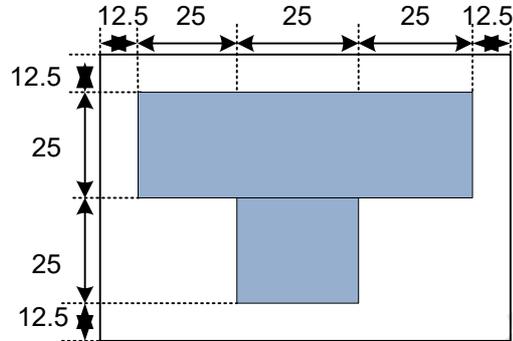
● **Alignment Mark Right: R(X,Y)= (15969.4, 440.5) ,   Unit: um**
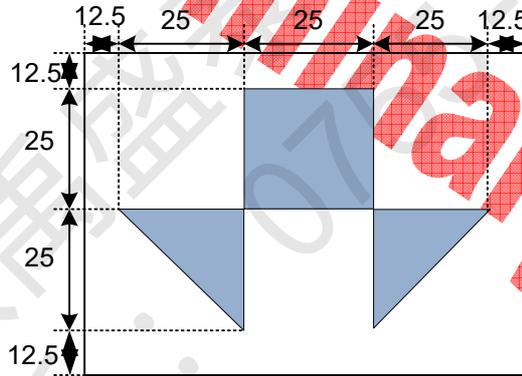
● **Chip Information**

Chip size	32060um x 947um
Chip height & width tolerance	20um
Chip thickness	150um
Pad Location	Pad center
Coordinate Origin	Chip center

4.1.4 Pad Center Coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	CGOUTL[1]	-15839.50	-418	34	DUMMY	-14552.50	-418	67	VDDATEST2_L	-13265.50	-418
2	CGOUTL[2]	-15800.50	-418	35	DUMMY	-14513.50	-418	68	VDDATEST2_L	-13226.50	-418
3	CGOUTL[3]	-15761.50	-418	36	DUMMY	-14474.50	-418	69	VGHO1	-13187.50	-418
4	CGOUTL[4]	-15722.50	-418	37	VGL	-14435.50	-418	70	VGHO1	-13148.50	-418
5	CGOUTL[5]	-15683.50	-418	38	VGL	-14396.50	-418	71	VGHO1	-13109.50	-418
6	CGOUTL[6]	-15644.50	-418	39	VGL	-14357.50	-418	72	DGND	-13070.50	-418
7	CGOUTL[7]	-15605.50	-418	40	VGL	-14318.50	-418	73	DGND	-13031.50	-418
8	CGOUTL[8]	-15566.50	-418	41	VGH	-14279.50	-418	74	DGND	-12992.50	-418
9	CGOUTL[9]	-15527.50	-418	42	VGH	-14240.50	-418	75	DGND	-12953.50	-418
10	CGOUTL[10]	-15488.50	-418	43	VGH	-14201.50	-418	76	TX_0D	-12914.50	-418
11	CGOUTL[11]	-15449.50	-418	44	VGH	-14162.50	-418	77	RX_0D[0]	-12875.50	-418
12	CGOUTL[12]	-15410.50	-418	45	DUMMY	-14123.50	-418	78	RX_0D[1]	-12836.50	-418
13	CGOUTL[13]	-15371.50	-418	46	COGTEST1	-14084.50	-418	79	RX_0D[2]	-12797.50	-418
14	CGOUTL[14]	-15332.50	-418	47	COGTEST2	-14045.50	-418	80	DUMMY	-12758.50	-418
15	CGOUTL[15]	-15293.50	-418	48	DUMMY	-14006.50	-418	81	DUMMY	-12719.50	-418
16	CGOUTL[16]	-15254.50	-418	49	DUMMY	-13967.50	-418	82	DUMMY	-12680.50	-418
17	CGOUTL[17]	-15215.50	-418	50	TEST0	-13928.50	-418	83	AGND	-12641.50	-418
18	CGOUTL[18]	-15176.50	-418	51	TEST1	-13889.50	-418	84	AGND	-12602.50	-418
19	CGOUTL[19]	-15137.50	-418	52	TEST2	-13850.50	-418	85	AGND	-12563.50	-418
20	CGOUTL[20]	-15098.50	-418	53	TEST3	-13811.50	-418	86	AGND	-12524.50	-418
21	CGOUTL[21]	-15059.50	-418	54	TEST4	-13772.50	-418	87	AGND	-12485.50	-418
22	CGOUTL[22]	-15020.50	-418	55	TEST5	-13733.50	-418	88	AGND	-12446.50	-418
23	DUMMY	-14981.50	-418	56	TEST6	-13694.50	-418	89	AGND	-12407.50	-418
24	DUMMY	-14942.50	-418	57	TEST7	-13655.50	-418	90	AGND	-12368.50	-418
25	DUMMY	-14903.50	-418	58	TEST8	-13616.50	-418	91	AVDD	-12329.50	-418
26	DUMMY	-14864.50	-418	59	TEST9	-13577.50	-418	92	AVDD	-12290.50	-418
27	DUMMY	-14825.50	-418	60	TEST10	-13538.50	-418	93	AVDD	-12251.50	-418
28	DUMMY	-14786.50	-418	61	TEST11	-13499.50	-418	94	AVDD	-12212.50	-418
29	DUMMY	-14747.50	-418	62	TEST12	-13460.50	-418	95	AVDD	-12173.50	-418
30	DUMMY	-14708.50	-418	63	VDDATEST0_L	-13421.50	-418	96	AVDD	-12134.50	-418
31	DUMMY	-14669.50	-418	64	VDDATEST0_L	-13382.50	-418	97	AVDD	-12095.50	-418
32	DUMMY	-14630.50	-418	65	VDDATEST1_L	-13343.50	-418	98	TVL	-12056.50	-418
33	DUMMY	-14591.50	-418	66	VDDATEST1_L	-13304.50	-418	99	TVL	-12017.50	-418

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
100	TVL	-11978.50	-418	135	AVEE	-10613.50	-418	170	VGH	-9248.50	-418
101	TVH	-11939.50	-418	136	AGND	-10574.50	-418	171	VGH	-9209.50	-418
102	TVH	-11900.50	-418	137	AGND	-10535.50	-418	172	VGH	-9170.50	-418
103	TVH	-11861.50	-418	138	AGND	-10496.50	-418	173	VGH	-9131.50	-418
104	TVH	-11822.50	-418	139	AGND	-10457.50	-418	174	AGND	-9092.50	-418
105	TVH	-11783.50	-418	140	AGND	-10418.50	-418	175	AGND	-9053.50	-418
106	AVDD	-11744.50	-418	141	AGND	-10379.50	-418	176	AGND	-9014.50	-418
107	AVDD	-11705.50	-418	142	TEST16	-10340.50	-418	177	AGND	-8975.50	-418
108	AVDD	-11666.50	-418	143	TEST16	-10301.50	-418	178	AGND	-8936.50	-418
109	AGND	-11627.50	-418	144	AVDD	-10262.50	-418	179	AGND	-8897.50	-418
110	AGND	-11588.50	-418	145	AVDD	-10223.50	-418	180	AGND	-8858.50	-418
111	AGND	-11549.50	-418	146	AVDD	-10184.50	-418	181	AGND	-8819.50	-418
112	VCOM_PASS_L	-11510.50	-418	147	AVDD	-10145.50	-418	182	AGND	-8780.50	-418
113	VCOM_PASS_L	-11471.50	-418	148	AVDD	-10106.50	-418	183	AGND	-8741.50	-418
114	VCOM_PASS_L	-11432.50	-418	149	AVDD	-10067.50	-418	184	AGND	-8702.50	-418
115	VCOM_PASS_L	-11393.50	-418	150	AVEE	-10028.50	-418	185	AGND	-8663.50	-418
116	IOVCC	-11354.50	-418	151	AVEE	-9989.50	-418	186	AVDD	-8624.50	-418
117	IOVCC	-11315.50	-418	152	AVEE	-9950.50	-418	187	AVDD	-8585.50	-418
118	IOVCC	-11276.50	-418	153	AVEE	-9911.50	-418	188	AVDD	-8546.50	-418
119	IOVCC	-11237.50	-418	154	AVEE	-9872.50	-418	189	AVDD	-8507.50	-418
120	IOVCC	-11198.50	-418	155	AVEE	-9833.50	-418	190	AVDD	-8468.50	-418
121	IOVCC	-11159.50	-418	156	IOVCC	-9794.50	-418	191	AVDD	-8429.50	-418
122	VCOM_OPT_L	-11120.50	-418	157	IOVCC	-9755.50	-418	192	IOVCC	-8390.50	-418
123	VCOM_OPT_L	-11081.50	-418	158	IOVCC	-9716.50	-418	193	IOVCC	-8351.50	-418
124	VCOM_OPT_L	-11042.50	-418	159	IOVCC	-9677.50	-418	194	IOVCC	-8312.50	-418
125	VCOM_OPT_L	-11003.50	-418	160	IOVCC	-9638.50	-418	195	IOVCC	-8273.50	-418
126	VCOM_OPT_L	-10964.50	-418	161	IOVCC	-9599.50	-418	196	IOVCC	-8234.50	-418
127	VCOM_OPT_L	-10925.50	-418	162	VDDD	-9560.50	-418	197	IOVCC	-8195.50	-418
128	VCOM_OPT_L	-10886.50	-418	163	VDDD	-9521.50	-418	198	AGND	-8156.50	-418
129	VCOM_OPT_L	-10847.50	-418	164	VDDD	-9482.50	-418	199	AGND	-8117.50	-418
130	AVEE	-10808.50	-418	165	VDDD	-9443.50	-418	200	AGND	-8078.50	-418
131	AVEE	-10769.50	-418	166	VDDD	-9404.50	-418	201	AGND	-8039.50	-418
132	AVEE	-10730.50	-418	167	VDDD	-9365.50	-418	202	AGND	-8000.50	-418
133	AVEE	-10691.50	-418	168	VGH	-9326.50	-418	203	AGND	-7961.50	-418
134	AVEE	-10652.50	-418	169	VGH	-9287.50	-418	204	AVEE	-7922.50	-418

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
205	AVEE	-7883.50	-418	240	AGND	-6518.50	-418	275	DPHYVCC	-5153.50	-418
206	AVEE	-7844.50	-418	241	AGND	-6479.50	-418	276	DPHYVCC	-5114.50	-418
207	AVEE	-7805.50	-418	242	AGND	-6440.50	-418	277	DPHYVCC	-5075.50	-418
208	AVEE	-7766.50	-418	243	AGND	-6401.50	-418	278	DPHYVCC	-5036.50	-418
209	AVEE	-7727.50	-418	244	IOVCC	-6362.50	-418	279	VDDM	-4997.50	-418
210	AVDD	-7688.50	-418	245	IOVCC	-6323.50	-418	280	VDDM	-4958.50	-418
211	AVDD	-7649.50	-418	246	IOVCC	-6284.50	-418	281	VDDM	-4919.50	-418
212	AVDD	-7610.50	-418	247	IOVCC	-6245.50	-418	282	DPHYGND	-4880.50	-418
213	AVDD	-7571.50	-418	248	IOVCC	-6206.50	-418	283	DPHYGND	-4841.50	-418
214	AVDD	-7532.50	-418	249	IOVCC	-6167.50	-418	284	DPHYGND	-4802.50	-418
215	AVDD	-7493.50	-418	250	IOVCC	-6128.50	-418	285	DATA2P	-4763.50	-418
216	AVDD	-7454.50	-418	251	IOVCC	-6089.50	-418	286	DATA2P	-4724.50	-418
217	AVDD	-7415.50	-418	252	IOVCC	-6050.50	-418	287	DATA2P	-4685.50	-418
218	AVDD	-7376.50	-418	253	IOVCC	-6011.50	-418	288	DATA2P	-4646.50	-418
219	AVDD	-7337.50	-418	254	IOVCC	-5972.50	-418	289	DATA2P	-4607.50	-418
220	AVDD	-7298.50	-418	255	IOVCC	-5933.50	-418	290	DATA2P	-4568.50	-418
221	AVEE	-7259.50	-418	256	IOVCC	-5894.50	-418	291	DATA2N	-4529.50	-418
222	AVEE	-7220.50	-418	257	IOVCC	-5855.50	-418	292	DATA2N	-4490.50	-418
223	AVEE	-7181.50	-418	258	IOVCC	-5816.50	-418	293	DATA2N	-4451.50	-418
224	AVEE	-7142.50	-418	259	IOVCC	-5777.50	-418	294	DATA2N	-4412.50	-418
225	AVEE	-7103.50	-418	260	VDD	-5738.50	-418	295	DATA2N	-4373.50	-418
226	AVEE	-7064.50	-418	261	VDD	-5699.50	-418	296	DATA2N	-4334.50	-418
227	VCOM	-7025.50	-418	262	VDD	-5660.50	-418	297	DPHYGND	-4295.50	-418
228	VCOM	-6986.50	-418	263	VDD	-5621.50	-418	298	DPHYGND	-4256.50	-418
229	VCOM	-6947.50	-418	264	VDD	-5582.50	-418	299	DATA1P	-4217.50	-418
230	VCOM	-6908.50	-418	265	VDD	-5543.50	-418	300	DATA1P	-4178.50	-418
231	VCOM	-6869.50	-418	266	DGND	-5504.50	-418	301	DATA1P	-4139.50	-418
232	VCOM	-6830.50	-418	267	DGND	-5465.50	-418	302	DATA1P	-4100.50	-418
233	AGND	-6791.50	-418	268	DGND	-5426.50	-418	303	DATA1P	-4061.50	-418
234	AGND	-6752.50	-418	269	DGND	-5387.50	-418	304	DATA1P	-4022.50	-418
235	AGND	-6713.50	-418	270	DGND	-5348.50	-418	305	DATA1N	-3983.50	-418
236	AGND	-6674.50	-418	271	DGND	-5309.50	-418	306	DATA1N	-3944.50	-418
237	AGND	-6635.50	-418	272	DPHYVCC	-5270.50	-418	307	DATA1N	-3905.50	-418
238	AGND	-6596.50	-418	273	DPHYVCC	-5231.50	-418	308	DATA1N	-3866.50	-418
239	AGND	-6557.50	-418	274	DPHYVCC	-5192.50	-418	309	DATA1N	-3827.50	-418

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
310	DATA1N	-3788.50	-418	345	DATA3P	-2423.50	-418	380	AVDD	-1058.50	-418
311	DPHYGND	-3749.50	-418	346	DATA3P	-2384.50	-418	381	AGND	-1019.50	-418
312	DPHYGND	-3710.50	-418	347	DATA3N	-2345.50	-418	382	AGND	-980.50	-418
313	CLKP	-3671.50	-418	348	DATA3N	-2306.50	-418	383	AGND	-941.50	-418
314	CLKP	-3632.50	-418	349	DATA3N	-2267.50	-418	384	AGND	-902.50	-418
315	CLKP	-3593.50	-418	350	DATA3N	-2228.50	-418	385	AGND	-863.50	-418
316	CLKP	-3554.50	-418	351	DATA3N	-2189.50	-418	386	AGND	-824.50	-418
317	CLKP	-3515.50	-418	352	DATA3N	-2150.50	-418	387	AVEE	-785.50	-418
318	CLKP	-3476.50	-418	353	DPHYGND	-2111.50	-418	388	AVEE	-746.50	-418
319	CLKN	-3437.50	-418	354	DPHYGND	-2072.50	-418	389	AVEE	-707.50	-418
320	CLKN	-3398.50	-418	355	DPHYGND	-2033.50	-418	390	AVEE	-668.50	-418
321	CLKN	-3359.50	-418	356	IOVCC	-1994.50	-418	391	AVEE	-629.50	-418
322	CLKN	-3320.50	-418	357	IOVCC	-1955.50	-418	392	AVEE	-590.50	-418
323	CLKN	-3281.50	-418	358	IOVCC	-1916.50	-418	393	AGND	-551.50	-418
324	CLKN	-3242.50	-418	359	IOVCC	-1877.50	-418	394	AGND	-512.50	-418
325	DPHYGND	-3203.50	-418	360	IOVCC	-1838.50	-418	395	AGND	-473.50	-418
326	DPHYGND	-3164.50	-418	361	IOVCC	-1799.50	-418	396	AGND	-434.50	-418
327	DATA0P	-3125.50	-418	362	IOVCC	-1760.50	-418	397	AGND	-395.50	-418
328	DATA0P	-3086.50	-418	363	DGND	-1721.50	-418	398	AGND	-356.50	-418
329	DATA0P	-3047.50	-418	364	DGND	-1682.50	-418	399	TP_OPT_2	-317.50	-418
330	DATA0P	-3008.50	-418	365	DGND	-1643.50	-418	400	TP_OPT_3	-278.50	-418
331	DATA0P	-2969.50	-418	366	DGND	-1604.50	-418	401	TP_OPT_4	-239.50	-418
332	DATA0P	-2930.50	-418	367	DGND	-1565.50	-418	402	DUMMY	-200.50	-418
333	DATA0N	-2891.50	-418	368	DGND	-1526.50	-418	403	DUMMY	-161.50	-418
334	DATA0N	-2852.50	-418	369	DGND	-1487.50	-418	404	DUMMY	-122.50	-418
335	DATA0N	-2813.50	-418	370	DGND	-1448.50	-418	405	DUMMY	-83.50	-418
336	DATA0N	-2774.50	-418	371	DGND	-1409.50	-418	406	DUMMY	-44.50	-418
337	DATA0N	-2735.50	-418	372	DGND	-1370.50	-418	407	DUMMY	-5.50	-418
338	DATA0N	-2696.50	-418	373	DGND	-1331.50	-418	408	DUMMY	33.50	-418
339	DPHYGND	-2657.50	-418	374	DGND	-1292.50	-418	409	DUMMY	72.50	-418
340	DPHYGND	-2618.50	-418	375	AVDD	-1253.50	-418	410	DUMMY	111.50	-418
341	DATA3P	-2579.50	-418	376	AVDD	-1214.50	-418	411	DUMMY	150.50	-418
342	DATA3P	-2540.50	-418	377	AVDD	-1175.50	-418	412	DUMMY	189.50	-418
343	DATA3P	-2501.50	-418	378	AVDD	-1136.50	-418	413	DUMMY	228.50	-418
344	DATA3P	-2462.50	-418	379	AVDD	-1097.50	-418	414	DUMMY	267.50	-418

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
415	TP_TEST7	306.50	-418	450	TE	1671.50	-418	485	TP_OPT_1	3036.50	-418
416	TP_TEST8	345.50	-418	451	TE	1710.50	-418	486	TP_TEST9	3075.50	-418
417	TEST36	384.50	-418	452	TE1	1749.50	-418	487	TP_INT	3114.50	-418
418	TEST29	423.50	-418	453	TE1	1788.50	-418	488	TP_I2C_SDA	3153.50	-418
419	TEST30	462.50	-418	454	LEDPWM	1827.50	-418	489	TP_I2C_SCL	3192.50	-418
420	TEST31	501.50	-418	455	LEDPWM	1866.50	-418	490	TP_SPI_CS	3231.50	-418
421	TEST32	540.50	-418	456	PSWAP	1905.50	-418	491	TP_SPI_MISO	3270.50	-418
422	TEST33	579.50	-418	457	PSWAP	1944.50	-418	492	TP_SPI_MOSI	3309.50	-418
423	TEST34	618.50	-418	458	IM[0]	1983.50	-418	493	TP_SPI_SCL	3348.50	-418
424	TEST35	657.50	-418	459	IM[0]	2022.50	-418	494	FLASH_CS	3387.50	-418
425	80TEST0	696.50	-418	460	IM[1]	2061.50	-418	495	FLASH_CS	3426.50	-418
426	80TEST1	735.50	-418	461	IM[1]	2100.50	-418	496	FLASH_MISO	3465.50	-418
427	80TEST2	774.50	-418	462	DSWAP[0]	2139.50	-418	497	FLASH_MISO	3504.50	-418
428	80TEST3	813.50	-418	463	DSWAP[0]	2178.50	-418	498	FLASH_MOSI	3543.50	-418
429	80TEST4	852.50	-418	464	DSWAP[1]	2217.50	-418	499	FLASH_MOSI	3582.50	-418
430	80TEST5	891.50	-418	465	DSWAP[1]	2256.50	-418	500	FLASH_SCL	3621.50	-418
431	80TEST6	930.50	-418	466	FRM	2295.50	-418	501	FLASH_SCL	3660.50	-418
432	80TEST7	969.50	-418	467	RESX	2334.50	-418	502	TP_TEST_EN	3699.50	-418
433	80TEST8	1008.50	-418	468	TP_RESX	2373.50	-418	503	TP_TEST_EN	3738.50	-418
434	80TEST9	1047.50	-418	469	TP_TEST0	2412.50	-418	504	DGND	3777.50	-418
435	DGND	1086.50	-418	470	TP_TEST1	2451.50	-418	505	DGND	3816.50	-418
436	DGND	1125.50	-418	471	TP_TEST2	2490.50	-418	506	DGND	3855.50	-418
437	PWR_TEST3	1164.50	-418	472	TP_TEST3	2529.50	-418	507	DGND	3894.50	-418
438	PWR_TEST3	1203.50	-418	473	TP_TEST4	2568.50	-418	508	DGND	3933.50	-418
439	80TEST10	1242.50	-418	474	TP_TEST5	2607.50	-418	509	DGND	3972.50	-418
440	80TEST11	1281.50	-418	475	TP_TEST6	2646.50	-418	510	VDDD	4011.50	-418
441	TEST20	1320.50	-418	476	PWR_TEST1	2685.50	-418	511	VDDD	4050.50	-418
442	TEST21	1359.50	-418	477	PWR_TEST1	2724.50	-418	512	VDDD	4089.50	-418
443	TEST22	1398.50	-418	478	DGND	2763.50	-418	513	VDDD	4128.50	-418
444	TEST23	1437.50	-418	479	DGND	2802.50	-418	514	VDDD	4167.50	-418
445	TEST24	1476.50	-418	480	PWR_TEST2	2841.50	-418	515	VDDD	4206.50	-418
446	TEST25	1515.50	-418	481	PWR_TEST2	2880.50	-418	516	IOVCC	4245.50	-418
447	TEST26	1554.50	-418	482	TP_UART_TX	2919.50	-418	517	IOVCC	4284.50	-418
448	TEST27	1593.50	-418	483	FLASH_HOLD	2958.50	-418	518	IOVCC	4323.50	-418
449	TEST28	1632.50	-418	484	FLASH_WP	2997.50	-418	519	IOVCC	4362.50	-418

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
520	IOVCC	4401.50	-418	555	AVDD	5766.50	-418	590	AGND	7131.50	-418
521	IOVCC	4440.50	-418	556	AVDD	5805.50	-418	591	TVL	7170.50	-418
522	IOVCC	4479.50	-418	557	AVDD	5844.50	-418	592	TVL	7209.50	-418
523	IOVCC	4518.50	-418	558	AVDD	5883.50	-418	593	TVL	7248.50	-418
524	IOVCC	4557.50	-418	559	IOVCC	5922.50	-418	594	TVL	7287.50	-418
525	IOVCC	4596.50	-418	560	IOVCC	5961.50	-418	595	TVL	7326.50	-418
526	IOVCC	4635.50	-418	561	IOVCC	6000.50	-418	596	TVL	7365.50	-418
527	IOVCC	4674.50	-418	562	IOVCC	6039.50	-418	597	TVH	7404.50	-418
528	IOVCC	4713.50	-418	563	IOVCC	6078.50	-418	598	TVH	7443.50	-418
529	VCOM	4752.50	-418	564	GVDDP	6117.50	-418	599	TVH	7482.50	-418
530	VCOM	4791.50	-418	565	GVDDP	6156.50	-418	600	TVH	7521.50	-418
531	VCOM	4830.50	-418	566	GVDDP	6195.50	-418	601	TVH	7560.50	-418
532	VCOM	4869.50	-418	567	GVDDN	6234.50	-418	602	TVH	7599.50	-418
533	VCOM	4908.50	-418	568	GVDDN	6273.50	-418	603	VAG	7638.50	-418
534	VCOM	4947.50	-418	569	GVDDN	6312.50	-418	604	VAG	7677.50	-418
535	VCOM	4986.50	-418	570	DGND	6351.50	-418	605	VAG	7716.50	-418
536	AGND	5025.50	-418	571	DGND	6390.50	-418	606	VAG	7755.50	-418
537	AGND	5064.50	-418	572	DGND	6429.50	-418	607	VAG	7794.50	-418
538	AGND	5103.50	-418	573	AGND	6468.50	-418	608	VAG	7833.50	-418
539	AGND	5142.50	-418	574	AGND	6507.50	-418	609	AVDD	7872.50	-418
540	AGND	5181.50	-418	575	AGND	6546.50	-418	610	AVDD	7911.50	-418
541	AGND	5220.50	-418	576	AGND	6585.50	-418	611	AVDD	7950.50	-418
542	AVEE	5259.50	-418	577	AGND	6624.50	-418	612	AVDD	7989.50	-418
543	AVEE	5298.50	-418	578	AGND	6663.50	-418	613	AVDD	8028.50	-418
544	AVEE	5337.50	-418	579	AGND	6702.50	-418	614	AVDD	8067.50	-418
545	AVEE	5376.50	-418	580	AGND	6741.50	-418	615	AVEE	8106.50	-418
546	AVEE	5415.50	-418	581	AGND	6780.50	-418	616	AVEE	8145.50	-418
547	AVEE	5454.50	-418	582	AGND	6819.50	-418	617	AVEE	8184.50	-418
548	AVEE	5493.50	-418	583	AGND	6858.50	-418	618	AVEE	8223.50	-418
549	AVDD	5532.50	-418	584	AGND	6897.50	-418	619	AVEE	8262.50	-418
550	AVDD	5571.50	-418	585	AGND	6936.50	-418	620	AVEE	8301.50	-418
551	AVDD	5610.50	-418	586	AGND	6975.50	-418	621	AVEE	8340.50	-418
552	AVDD	5649.50	-418	587	AGND	7014.50	-418	622	AVEE	8379.50	-418
553	AVDD	5688.50	-418	588	AGND	7053.50	-418	623	IOVCC	8418.50	-418
554	AVDD	5727.50	-418	589	AGND	7092.50	-418	624	IOVCC	8457.50	-418

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
625	IOVCC	8496.50	-418	660	AVEE	9861.50	-418	695	IOVCC	11226.50	-418
626	IOVCC	8535.50	-418	661	AVEE	9900.50	-418	696	IOVCC	11265.50	-418
627	IOVCC	8574.50	-418	662	AVEE	9939.50	-418	697	IOVCC	11304.50	-418
628	IOVCC	8613.50	-418	663	AVEE	9978.50	-418	698	IOVCC	11343.50	-418
629	AVDD	8652.50	-418	664	AVEE	10017.50	-418	699	VCOM_PASS_R	11382.50	-418
630	AVDD	8691.50	-418	665	AVDD	10056.50	-418	700	VCOM_PASS_R	11421.50	-418
631	AVDD	8730.50	-418	666	AVDD	10095.50	-418	701	VCOM_PASS_R	11460.50	-418
632	AVDD	8769.50	-418	667	AVDD	10134.50	-418	702	VCOM_PASS_R	11499.50	-418
633	AVDD	8808.50	-418	668	AVDD	10173.50	-418	703	AGND	11538.50	-418
634	AVDD	8847.50	-418	669	AVDD	10212.50	-418	704	AGND	11577.50	-418
635	AGND	8886.50	-418	670	AGND	10251.50	-418	705	AGND	11616.50	-418
636	AGND	8925.50	-418	671	AGND	10290.50	-418	706	AVDD	11655.50	-418
637	AGND	8964.50	-418	672	AGND	10329.50	-418	707	AVDD	11694.50	-418
638	AGND	9003.50	-418	673	AGND	10368.50	-418	708	AVDD	11733.50	-418
639	AGND	9042.50	-418	674	AGND	10407.50	-418	709	TVH	11772.50	-418
640	AGND	9081.50	-418	675	AGND	10446.50	-418	710	TVH	11811.50	-418
641	VGL	9120.50	-418	676	AVEE	10485.50	-418	711	TVH	11850.50	-418
642	VGL	9159.50	-418	677	AVEE	10524.50	-418	712	TVH	11889.50	-418
643	VGL	9198.50	-418	678	AVEE	10563.50	-418	713	TVH	11928.50	-418
644	VGL	9237.50	-418	679	AVEE	10602.50	-418	714	TVL	11967.50	-418
645	VGL	9276.50	-418	680	AVEE	10641.50	-418	715	TVL	12006.50	-418
646	VGL	9315.50	-418	681	AVEEP	10680.50	-418	716	TVL	12045.50	-418
647	AGND	9354.50	-418	682	VCOM_OPT_R	10719.50	-418	717	AVDD	12084.50	-418
648	AGND	9393.50	-418	683	VCOM_OPT_R	10758.50	-418	718	AVDD	12123.50	-418
649	AGND	9432.50	-418	684	VCOM_OPT_R	10797.50	-418	719	AVDD	12162.50	-418
650	AGND	9471.50	-418	685	VCOM_OPT_R	10836.50	-418	720	AVDD	12201.50	-418
651	AGND	9510.50	-418	686	VCOM_OPT_R	10875.50	-418	721	AVDD	12240.50	-418
652	AGND	9549.50	-418	687	VCOM_OPT_R	10914.50	-418	722	AVDD	12279.50	-418
653	VDDD	9588.50	-418	688	VCOM_OPT_R	10953.50	-418	723	AVDD	12318.50	-418
654	VDDD	9627.50	-418	689	VCOM_OPT_R	10992.50	-418	724	AGND	12357.50	-418
655	VDDD	9666.50	-418	690	IOVCC	11031.50	-418	725	AGND	12396.50	-418
656	VDDD	9705.50	-418	691	IOVCC	11070.50	-418	726	AGND	12435.50	-418
657	VDDD	9744.50	-418	692	IOVCC	11109.50	-418	727	AGND	12474.50	-418
658	VDDD	9783.50	-418	693	IOVCC	11148.50	-418	728	AGND	12513.50	-418
659	AVEE	9822.50	-418	694	IOVCC	11187.50	-418	729	AGND	12552.50	-418

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
730	AGND	12591.50	-418	765	DUMMY	13956.50	-418	800	CGOUTR[14]	15321.50	-418
731	AGND	12630.50	-418	766	DUMMY	13995.50	-418	801	CGOUTR[13]	15360.50	-418
732	DUMMY	12669.50	-418	767	COGTEST3	14034.50	-418	802	CGOUTR[12]	15399.50	-418
733	DUMMY	12708.50	-418	768	COGTEST4	14073.50	-418	803	CGOUTR[11]	15438.50	-418
734	DUMMY	12747.50	-418	769	DUMMY	14112.50	-418	804	CGOUTR[10]	15477.50	-418
735	RX_1D[2]	12786.50	-418	770	VGH	14151.50	-418	805	CGOUTR[9]	15516.50	-418
736	RX_1D[1]	12825.50	-418	771	VGH	14190.50	-418	806	CGOUTR[8]	15555.50	-418
737	RX_1D[0]	12864.50	-418	772	VGH	14229.50	-418	807	CGOUTR[7]	15594.50	-418
738	TX_1D	12903.50	-418	773	VGH	14268.50	-418	808	CGOUTR[6]	15633.50	-418
739	DGND	12942.50	-418	774	DUMMY	14307.50	-418	809	CGOUTR[5]	15672.50	-418
740	DGND	12981.50	-418	775	DUMMY	14346.50	-418	810	CGOUTR[4]	15711.50	-418
741	DGND	13020.50	-418	776	DUMMY	14385.50	-418	811	CGOUTR[3]	15750.50	-418
742	DGND	13059.50	-418	777	DUMMY	14424.50	-418	812	CGOUTR[2]	15789.50	-418
743	VGHO1	13098.50	-418	778	DUMMY	14463.50	-418	813	CGOUTR[1]	15828.50	-418
744	VGHO1	13137.50	-418	779	DUMMY	14502.50	-418	814	DUMMY	15893.45	53
745	VGHO1	13176.50	-418	780	DUMMY	14541.50	-418	815	DUMMY	15883.75	173
746	VDDATEST2_R	13215.50	-418	781	DUMMY	14580.50	-418	816	DUMMY	15874.05	293
747	VDDATEST2_R	13254.50	-418	782	DUMMY	14619.50	-418	817	DUMMY	15854.65	53
748	VDDATEST1_R	13293.50	-418	783	DUMMY	14658.50	-418	818	DUMMY	15844.95	173
749	VDDATEST1_R	13332.50	-418	784	DUMMY	14697.50	-418	819	DUMMY	15835.25	293
750	VDDATEST0_R	13371.50	-418	785	DUMMY	14736.50	-418	820	DUMMY	15825.55	413
751	VDDATEST0_R	13410.50	-418	786	DUMMY	14775.50	-418	821	DUMMY	15815.85	53
752	TEST13	13449.50	-418	787	DUMMY	14814.50	-418	822	DUMMY	15806.15	173
753	TEST14	13488.50	-418	788	DUMMY	14853.50	-418	823	DUMMY	15796.45	293
754	TEST15	13527.50	-418	789	DUMMY	14892.50	-418	824	DUMMY	15786.75	413
755	DUMMY	13566.50	-418	790	DUMMY	14931.50	-418	825	VCOM_PASS_R	15777.05	53
756	DUMMY	13605.50	-418	791	DUMMY	14970.50	-418	826	VCOM_PASS_R	15767.35	173
757	DUMMY	13644.50	-418	792	CGOUTR[22]	15009.50	-418	827	VCOM_PASS_R	15757.65	293
758	DUMMY	13683.50	-418	793	CGOUTR[21]	15048.50	-418	828	DUMMY	15747.95	413
759	DUMMY	13722.50	-418	794	CGOUTR[20]	15087.50	-418	829	VCOM_PASS_R	15738.25	53
760	PWR_TEST4	13761.50	-418	795	CGOUTR[19]	15126.50	-418	830	VCOM_PASS_R	15728.55	173
761	PWR_TEST4	13800.50	-418	796	CGOUTR[18]	15165.50	-418	831	VCOM_PASS_R	15718.85	293
762	PWR_TEST4	13839.50	-418	797	CGOUTR[17]	15204.50	-418	832	DUMMY	15709.15	413
763	PWR_TEST4	13878.50	-418	798	CGOUTR[16]	15243.50	-418	833	DUMMY	15699.45	53
764	DUMMY	13917.50	-418	799	CGOUTR[15]	15282.50	-418	834	DUMMY	15689.75	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
835	DUMMY	15680.05	293	870	S23	15340.55	173	905	S49	15001.05	53
836	DUMMY	15670.35	413	871	S24	15330.85	293	906	S50	14991.35	173
837	DUMMY	15660.65	53	872	RX[573]	15321.15	413	907	S51	14981.65	293
838	SDUM0	15650.95	173	873	S25	15311.45	53	908	RX[564]	14971.95	413
839	SDUM1	15641.25	293	874	S26	15301.75	173	909	S52	14962.25	53
840	GRID20	15631.55	413	875	S27	15292.05	293	910	S53	14952.55	173
841	S1	15621.85	53	876	RX[572]	15282.35	413	911	S54	14942.85	293
842	S2	15612.15	173	877	S28	15272.65	53	912	RX[563]	14933.15	413
843	S3	15602.45	293	878	S29	15262.95	173	913	S55	14923.45	53
844	GRID20	15592.75	413	879	S30	15253.25	293	914	S56	14913.75	173
845	S4	15583.05	53	880	RX[571]	15243.55	413	915	S57	14904.05	293
846	S5	15573.35	173	881	S31	15233.85	53	916	RX[562]	14894.35	413
847	S6	15563.65	293	882	S32	15224.15	173	917	S58	14884.65	53
848	GRID20	15553.95	413	883	S33	15214.45	293	918	S59	14874.95	173
849	S7	15544.25	53	884	RX[570]	15204.75	413	919	S60	14865.25	293
850	S8	15534.55	173	885	S34	15195.05	53	920	RX[561]	14855.55	413
851	S9	15524.85	293	886	S35	15185.35	173	921	S61	14845.85	53
852	GRID20	15515.15	413	887	S36	15175.65	293	922	S62	14836.15	173
853	S10	15505.45	53	888	RX[569]	15165.95	413	923	S63	14826.45	293
854	S11	15495.75	173	889	S37	15156.25	53	924	RX[560]	14816.75	413
855	S12	15486.05	293	890	S38	15146.55	173	925	S64	14807.05	53
856	GRID20	15476.35	413	891	S39	15136.85	293	926	S65	14797.35	173
857	S13	15466.65	53	892	RX[568]	15127.15	413	927	S66	14787.65	293
858	S14	15456.95	173	893	S40	15117.45	53	928	RX[559]	14777.95	413
859	S15	15447.25	293	894	S41	15107.75	173	929	S67	14768.25	53
860	RX[576]	15437.55	413	895	S42	15098.05	293	930	S68	14758.55	173
861	S16	15427.85	53	896	RX[567]	15088.35	413	931	S69	14748.85	293
862	S17	15418.15	173	897	S43	15078.65	53	932	RX[558]	14739.15	413
863	S18	15408.45	293	898	S44	15068.95	173	933	S70	14729.45	53
864	RX[575]	15398.75	413	899	S45	15059.25	293	934	S71	14719.75	173
865	S19	15389.05	53	900	RX[566]	15049.55	413	935	S72	14710.05	293
866	S20	15379.35	173	901	S46	15039.85	53	936	RX[557]	14700.35	413
867	S21	15369.65	293	902	S47	15030.15	173	937	S73	14690.65	53
868	RX[574]	15359.95	413	903	S48	15020.45	293	938	S74	14680.95	173
869	S22	15350.25	53	904	RX[565]	15010.75	413	939	S75	14671.25	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
940	RX[556]	14661.55	413	975	S102	14322.05	293	1010	S128	13982.55	173
941	S76	14651.85	53	976	RX[547]	14312.35	413	1011	S129	13972.85	293
942	S77	14642.15	173	977	S103	14302.65	53	1012	GRID19	13963.15	413
943	S78	14632.45	293	978	S104	14292.95	173	1013	S130	13953.45	53
944	RX[555]	14622.75	413	979	S105	14283.25	293	1014	S131	13943.75	173
945	S79	14613.05	53	980	RX[546]	14273.55	413	1015	S132	13934.05	293
946	S80	14603.35	173	981	S106	14263.85	53	1016	RX[544]	13924.35	413
947	S81	14593.65	293	982	S107	14254.15	173	1017	S133	13914.65	53
948	RX[554]	14583.95	413	983	S108	14244.45	293	1018	S134	13904.95	173
949	S82	14574.25	53	984	RX[545]	14234.75	413	1019	S135	13895.25	293
950	S83	14564.55	173	985	S109	14225.05	53	1020	RX[543]	13885.55	413
951	S84	14554.85	293	986	S110	14215.35	173	1021	S136	13875.85	53
952	RX[553]	14545.15	413	987	S111	14205.65	293	1022	S137	13866.15	173
953	S85	14535.45	53	988	GRID19	14195.95	413	1023	S138	13856.45	293
954	S86	14525.75	173	989	S112	14186.25	53	1024	RX[542]	13846.75	413
955	S87	14516.05	293	990	S113	14176.55	173	1025	S139	13837.05	53
956	RX[552]	14506.35	413	991	S114	14166.85	293	1026	S140	13827.35	173
957	S88	14496.65	53	992	GRID19	14157.15	413	1027	S141	13817.65	293
958	S89	14486.95	173	993	S115	14147.45	53	1028	RX[541]	13807.95	413
959	S90	14477.25	293	994	S116	14137.75	173	1029	S142	13798.25	53
960	RX[551]	14467.55	413	995	S117	14128.05	293	1030	S143	13788.55	173
961	S91	14457.85	53	996	GRID19	14118.35	413	1031	S144	13778.85	293
962	S92	14448.15	173	997	S118	14108.65	53	1032	RX[540]	13769.15	413
963	S93	14438.45	293	998	S119	14098.95	173	1033	S145	13759.45	53
964	RX[550]	14428.75	413	999	S120	14089.25	293	1034	S146	13749.75	173
965	S94	14419.05	53	1000	GRID19	14079.55	413	1035	S147	13740.05	293
966	S95	14409.35	173	1001	S121	14069.85	53	1036	RX[539]	13730.35	413
967	S96	14399.65	293	1002	S122	14060.15	173	1037	S148	13720.65	53
968	RX[549]	14389.95	413	1003	S123	14050.45	293	1038	S149	13710.95	173
969	S97	14380.25	53	1004	GRID19	14040.75	413	1039	S150	13701.25	293
970	S98	14370.55	173	1005	S124	14031.05	53	1040	RX[538]	13691.55	413
971	S99	14360.85	293	1006	S125	14021.35	173	1041	S151	13681.85	53
972	RX[548]	14351.15	413	1007	S126	14011.65	293	1042	S152	13672.15	173
973	S100	14341.45	53	1008	GRID19	14001.95	413	1043	S153	13662.45	293
974	S101	14331.75	173	1009	S127	13992.25	53	1044	RX[537]	13652.75	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1045	S154	13643.05	53	1080	RX[528]	13303.55	413	1115	S207	12964.05	293
1046	S155	13633.35	173	1081	S181	13293.85	53	1116	RX[519]	12954.35	413
1047	S156	13623.65	293	1082	S182	13284.15	173	1117	S208	12944.65	53
1048	RX[536]	13613.95	413	1083	S183	13274.45	293	1118	S209	12934.95	173
1049	S157	13604.25	53	1084	RX[527]	13264.75	413	1119	S210	12925.25	293
1050	S158	13594.55	173	1085	S184	13255.05	53	1120	RX[518]	12915.55	413
1051	S159	13584.85	293	1086	S185	13245.35	173	1121	S211	12905.85	53
1052	RX[535]	13575.15	413	1087	S186	13235.65	293	1122	S212	12896.15	173
1053	S160	13565.45	53	1088	RX[526]	13225.95	413	1123	S213	12886.45	293
1054	S161	13555.75	173	1089	S187	13216.25	53	1124	RX[517]	12876.75	413
1055	S162	13546.05	293	1090	S188	13206.55	173	1125	S214	12867.05	53
1056	RX[534]	13536.35	413	1091	S189	13196.85	293	1126	S215	12857.35	173
1057	S163	13526.65	53	1092	RX[525]	13187.15	413	1127	S216	12847.65	293
1058	S164	13516.95	173	1093	S190	13177.45	53	1128	RX[516]	12837.95	413
1059	S165	13507.25	293	1094	S191	13167.75	173	1129	S217	12828.25	53
1060	RX[533]	13497.55	413	1095	S192	13158.05	293	1130	S218	12818.55	173
1061	S166	13487.85	53	1096	RX[524]	13148.35	413	1131	S219	12808.85	293
1062	S167	13478.15	173	1097	S193	13138.65	53	1132	RX[515]	12799.15	413
1063	S168	13468.45	293	1098	S194	13128.95	173	1133	S220	12789.45	53
1064	RX[532]	13458.75	413	1099	S195	13119.25	293	1134	S221	12779.75	173
1065	S169	13449.05	53	1100	RX[523]	13109.55	413	1135	S222	12770.05	293
1066	S170	13439.35	173	1101	S196	13099.85	53	1136	RX[514]	12760.35	413
1067	S171	13429.65	293	1102	S197	13090.15	173	1137	S223	12750.65	53
1068	RX[531]	13419.95	413	1103	S198	13080.45	293	1138	S224	12740.95	173
1069	S172	13410.25	53	1104	RX[522]	13070.75	413	1139	S225	12731.25	293
1070	S173	13400.55	173	1105	S199	13061.05	53	1140	RX[513]	12721.55	413
1071	S174	13390.85	293	1106	S200	13051.35	173	1141	S226	12711.85	53
1072	RX[530]	13381.15	413	1107	S201	13041.65	293	1142	S227	12702.15	173
1073	S175	13371.45	53	1108	RX[521]	13031.95	413	1143	S228	12692.45	293
1074	S176	13361.75	173	1109	S202	13022.25	53	1144	GRID18	12682.75	413
1075	S177	13352.05	293	1110	S203	13012.55	173	1145	S229	12673.05	53
1076	RX[529]	13342.35	413	1111	S204	13002.85	293	1146	S230	12663.35	173
1077	S178	13332.65	53	1112	RX[520]	12993.15	413	1147	S231	12653.65	293
1078	S179	13322.95	173	1113	S205	12983.45	53	1148	GRID18	12643.95	413
1079	S180	13313.25	293	1114	S206	12973.75	173	1149	S232	12634.25	53

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1150	S233	12624.55	173	1185	S259	12285.05	53	1220	RX[500]	11945.55	413
1151	S234	12614.85	293	1186	S260	12275.35	173	1221	S286	11935.85	53
1152	GRID18	12605.15	413	1187	S261	12265.65	293	1222	S287	11926.15	173
1153	S235	12595.45	53	1188	RX[508]	12255.95	413	1223	S288	11916.45	293
1154	S236	12585.75	173	1189	S262	12246.25	53	1224	RX[499]	11906.75	413
1155	S237	12576.05	293	1190	S263	12236.55	173	1225	S289	11897.05	53
1156	GRID18	12566.35	413	1191	S264	12226.85	293	1226	S290	11887.35	173
1157	S238	12556.65	53	1192	RX[507]	12217.15	413	1227	S291	11877.65	293
1158	S239	12546.95	173	1193	S265	12207.45	53	1228	RX[498]	11867.95	413
1159	S240	12537.25	293	1194	S266	12197.75	173	1229	S292	11858.25	53
1160	GRID18	12527.55	413	1195	S267	12188.05	293	1230	S293	11848.55	173
1161	S241	12517.85	53	1196	RX[506]	12178.35	413	1231	S294	11838.85	293
1162	S242	12508.15	173	1197	S268	12168.65	53	1232	RX[497]	11829.15	413
1163	S243	12498.45	293	1198	S269	12158.95	173	1233	S295	11819.45	53
1164	GRID18	12488.75	413	1199	S270	12149.25	293	1234	S296	11809.75	173
1165	S244	12479.05	53	1200	RX[505]	12139.55	413	1235	S297	11800.05	293
1166	S245	12469.35	173	1201	S271	12129.85	53	1236	RX[496]	11790.35	413
1167	S246	12459.65	293	1202	S272	12120.15	173	1237	S298	11780.65	53
1168	GRID18	12449.95	413	1203	S273	12110.45	293	1238	S299	11770.95	173
1169	S247	12440.25	53	1204	RX[504]	12100.75	413	1239	S300	11761.25	293
1170	S248	12430.55	173	1205	S274	12091.05	53	1240	RX[495]	11751.55	413
1171	S249	12420.85	293	1206	S275	12081.35	173	1241	S301	11741.85	53
1172	RX[512]	12411.15	413	1207	S276	12071.65	293	1242	S302	11732.15	173
1173	S250	12401.45	53	1208	RX[503]	12061.95	413	1243	S303	11722.45	293
1174	S251	12391.75	173	1209	S277	12052.25	53	1244	RX[494]	11712.75	413
1175	S252	12382.05	293	1210	S278	12042.55	173	1245	S304	11703.05	53
1176	RX[511]	12372.35	413	1211	S279	12032.85	293	1246	S305	11693.35	173
1177	S253	12362.65	53	1212	RX[502]	12023.15	413	1247	S306	11683.65	293
1178	S254	12352.95	173	1213	S280	12013.45	53	1248	RX[493]	11673.95	413
1179	S255	12343.25	293	1214	S281	12003.75	173	1249	S307	11664.25	53
1180	RX[510]	12333.55	413	1215	S282	11994.05	293	1250	S308	11654.55	173
1181	S256	12323.85	53	1216	RX[501]	11984.35	413	1251	S309	11644.85	293
1182	S257	12314.15	173	1217	S283	11974.65	53	1252	RX[492]	11635.15	413
1183	S258	12304.45	293	1218	S284	11964.95	173	1253	S310	11625.45	53
1184	RX[509]	12294.75	413	1219	S285	11955.25	293	1254	S311	11615.75	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1255	S312	11606.05	293	1290	S338	11266.55	173	1325	S364	10927.05	53
1256	RX[491]	11596.35	413	1291	S339	11256.85	293	1326	S365	10917.35	173
1257	S313	11586.65	53	1292	RX[482]	11247.15	413	1327	S366	10907.65	293
1258	S314	11576.95	173	1293	S340	11237.45	53	1328	GRID17	10897.95	413
1259	S315	11567.25	293	1294	S341	11227.75	173	1329	S367	10888.25	53
1260	RX[490]	11557.55	413	1295	S342	11218.05	293	1330	S368	10878.55	173
1261	S316	11547.85	53	1296	RX[481]	11208.35	413	1331	S369	10868.85	293
1262	S317	11538.15	173	1297	S343	11198.65	53	1332	GRID17	10859.15	413
1263	S318	11528.45	293	1298	S344	11188.95	173	1333	S370	10849.45	53
1264	RX[489]	11518.75	413	1299	S345	11179.25	293	1334	S371	10839.75	173
1265	S319	11509.05	53	1300	GRID17	11169.55	413	1335	S372	10830.05	293
1266	S320	11499.35	173	1301	S346	11159.85	53	1336	GRID17	10820.35	413
1267	S321	11489.65	293	1302	S347	11150.15	173	1337	S373	10810.65	53
1268	RX[488]	11479.95	413	1303	S348	11140.45	293	1338	S374	10800.95	173
1269	S322	11470.25	53	1304	GRID17	11130.75	413	1339	S375	10791.25	293
1270	S323	11460.55	173	1305	S349	11121.05	53	1340	RX[480]	10781.55	413
1271	S324	11450.85	293	1306	S350	11111.35	173	1341	S376	10771.85	53
1272	RX[487]	11441.15	413	1307	S351	11101.65	293	1342	S377	10762.15	173
1273	S325	11431.45	53	1308	GRID17	11091.95	413	1343	S378	10752.45	293
1274	S326	11421.75	173	1309	S352	11082.25	53	1344	RX[479]	10742.75	413
1275	S327	11412.05	293	1310	S353	11072.55	173	1345	S379	10733.05	53
1276	RX[486]	11402.35	413	1311	S354	11062.85	293	1346	S380	10723.35	173
1277	S328	11392.65	53	1312	GRID17	11053.15	413	1347	S381	10713.65	293
1278	S329	11382.95	173	1313	S355	11043.45	53	1348	RX[478]	10703.95	413
1279	S330	11373.25	293	1314	S356	11033.75	173	1349	S382	10694.25	53
1280	RX[485]	11363.55	413	1315	S357	11024.05	293	1350	S383	10684.55	173
1281	S331	11353.85	53	1316	GRID17	11014.35	413	1351	S384	10674.85	293
1282	S332	11344.15	173	1317	S358	11004.65	53	1352	RX[477]	10665.15	413
1283	S333	11334.45	293	1318	S359	10994.95	173	1353	S385	10655.45	53
1284	RX[484]	11324.75	413	1319	S360	10985.25	293	1354	S386	10645.75	173
1285	S334	11315.05	53	1320	GRID17	10975.55	413	1355	S387	10636.05	293
1286	S335	11305.35	173	1321	S361	10965.85	53	1356	RX[476]	10626.35	413
1287	S336	11295.65	293	1322	S362	10956.15	173	1357	S388	10616.65	53
1288	RX[483]	11285.95	413	1323	S363	10946.45	293	1358	S389	10606.95	173
1289	S337	11276.25	53	1324	GRID17	10936.75	413	1359	S390	10597.25	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1360	RX[475]	10587.55	413	1395	S417	10248.05	293	1430	S443	9908.55	173
1361	S391	10577.85	53	1396	RX[466]	10238.35	413	1431	S444	9898.85	293
1362	S392	10568.15	173	1397	S418	10228.65	53	1432	RX[457]	9889.15	413
1363	S393	10558.45	293	1398	S419	10218.95	173	1433	S445	9879.45	53
1364	RX[474]	10548.75	413	1399	S420	10209.25	293	1434	S446	9869.75	173
1365	S394	10539.05	53	1400	RX[465]	10199.55	413	1435	S447	9860.05	293
1366	S395	10529.35	173	1401	S421	10189.85	53	1436	RX[456]	9850.35	413
1367	S396	10519.65	293	1402	S422	10180.15	173	1437	S448	9840.65	53
1368	RX[473]	10509.95	413	1403	S423	10170.45	293	1438	S449	9830.95	173
1369	S397	10500.25	53	1404	RX[464]	10160.75	413	1439	S450	9821.25	293
1370	S398	10490.55	173	1405	S424	10151.05	53	1440	RX[455]	9811.55	413
1371	S399	10480.85	293	1406	S425	10141.35	173	1441	S451	9801.85	53
1372	RX[472]	10471.15	413	1407	S426	10131.65	293	1442	S452	9792.15	173
1373	S400	10461.45	53	1408	RX[463]	10121.95	413	1443	S453	9782.45	293
1374	S401	10451.75	173	1409	S427	10112.25	53	1444	RX[454]	9772.75	413
1375	S402	10442.05	293	1410	S428	10102.55	173	1445	S454	9763.05	53
1376	RX[471]	10432.35	413	1411	S429	10092.85	293	1446	S455	9753.35	173
1377	S403	10422.65	53	1412	RX[462]	10083.15	413	1447	S456	9743.65	293
1378	S404	10412.95	173	1413	S430	10073.45	53	1448	RX[453]	9733.95	413
1379	S405	10403.25	293	1414	S431	10063.75	173	1449	S457	9724.25	53
1380	RX[470]	10393.55	413	1415	S432	10054.05	293	1450	S458	9714.55	173
1381	S406	10383.85	53	1416	RX[461]	10044.35	413	1451	S459	9704.85	293
1382	S407	10374.15	173	1417	S433	10034.65	53	1452	RX[452]	9695.15	413
1383	S408	10364.45	293	1418	S434	10024.95	173	1453	S460	9685.45	53
1384	RX[469]	10354.75	413	1419	S435	10015.25	293	1454	S461	9675.75	173
1385	S409	10345.05	53	1420	RX[460]	10005.55	413	1455	S462	9666.05	293
1386	S410	10335.35	173	1421	S436	9995.85	53	1456	RX[451]	9656.35	413
1387	S411	10325.65	293	1422	S437	9986.15	173	1457	S463	9646.65	53
1388	RX[468]	10315.95	413	1423	S438	9976.45	293	1458	S464	9636.95	173
1389	S412	10306.25	53	1424	RX[459]	9966.75	413	1459	S465	9627.25	293
1390	S413	10296.55	173	1425	S439	9957.05	53	1460	RX[450]	9617.55	413
1391	S414	10286.85	293	1426	S440	9947.35	173	1461	S466	9607.85	53
1392	RX[467]	10277.15	413	1427	S441	9937.65	293	1462	S467	9598.15	173
1393	S415	10267.45	53	1428	RX[458]	9927.95	413	1463	S468	9588.45	293
1394	S416	10257.75	173	1429	S442	9918.25	53	1464	RX[449]	9578.75	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1465	S469	9569.05	53	1500	RX[447]	9229.55	413	1535	S522	8890.05	293
1466	S470	9559.35	173	1501	S496	9219.85	53	1536	RX[438]	8880.35	413
1467	S471	9549.65	293	1502	S497	9210.15	173	1537	S523	8870.65	53
1468	GRID16	9539.95	413	1503	S498	9200.45	293	1538	S524	8860.95	173
1469	S472	9530.25	53	1504	RX[446]	9190.75	413	1539	S525	8851.25	293
1470	S473	9520.55	173	1505	S499	9181.05	53	1540	RX[437]	8841.55	413
1471	S474	9510.85	293	1506	S500	9171.35	173	1541	S526	8831.85	53
1472	GRID16	9501.15	413	1507	S501	9161.65	293	1542	S527	8822.15	173
1473	S475	9491.45	53	1508	RX[445]	9151.95	413	1543	S528	8812.45	293
1474	S476	9481.75	173	1509	S502	9142.25	53	1544	RX[436]	8802.75	413
1475	S477	9472.05	293	1510	S503	9132.55	173	1545	S529	8793.05	53
1476	GRID16	9462.35	413	1511	S504	9122.85	293	1546	S530	8783.35	173
1477	S478	9452.65	53	1512	RX[444]	9113.15	413	1547	S531	8773.65	293
1478	S479	9442.95	173	1513	S505	9103.45	53	1548	RX[435]	8763.95	413
1479	S480	9433.25	293	1514	S506	9093.75	173	1549	S532	8754.25	53
1480	GRID16	9423.55	413	1515	S507	9084.05	293	1550	S533	8744.55	173
1481	S481	9413.85	53	1516	RX[443]	9074.35	413	1551	S534	8734.85	293
1482	S482	9404.15	173	1517	S508	9064.65	53	1552	RX[434]	8725.15	413
1483	S483	9394.45	293	1518	S509	9054.95	173	1553	S535	8715.45	53
1484	GRID16	9384.75	413	1519	S510	9045.25	293	1554	S536	8705.75	173
1485	S484	9375.05	53	1520	RX[442]	9035.55	413	1555	S537	8696.05	293
1486	S485	9365.35	173	1521	S511	9025.85	53	1556	RX[433]	8686.35	413
1487	S486	9355.65	293	1522	S512	9016.15	173	1557	S538	8676.65	53
1488	GRID16	9345.95	413	1523	S513	9006.45	293	1558	S539	8666.95	173
1489	S487	9336.25	53	1524	RX[441]	8996.75	413	1559	S540	8657.25	293
1490	S488	9326.55	173	1525	S514	8987.05	53	1560	RX[432]	8647.55	413
1491	S489	9316.85	293	1526	S515	8977.35	173	1561	S541	8637.85	53
1492	GRID16	9307.15	413	1527	S516	8967.65	293	1562	S542	8628.15	173
1493	S490	9297.45	53	1528	RX[440]	8957.95	413	1563	S543	8618.45	293
1494	S491	9287.75	173	1529	S517	8948.25	53	1564	RX[431]	8608.75	413
1495	S492	9278.05	293	1530	S518	8938.55	173	1565	S544	8599.05	53
1496	RX[448]	9268.35	413	1531	S519	8928.85	293	1566	S545	8589.35	173
1497	S493	9258.65	53	1532	RX[439]	8919.15	413	1567	S546	8579.65	293
1498	S494	9248.95	173	1533	S520	8909.45	53	1568	RX[430]	8569.95	413
1499	S495	9239.25	293	1534	S521	8899.75	173	1569	S547	8560.25	53

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1570	S548	8550.55	173	1605	S574	8211.05	53	1640	GRID15	7871.55	413
1571	S549	8540.85	293	1606	S575	8201.35	173	1641	S601	7861.85	53
1572	RX[429]	8531.15	413	1607	S576	8191.65	293	1642	S602	7852.15	173
1573	S550	8521.45	53	1608	RX[420]	8181.95	413	1643	S603	7842.45	293
1574	S551	8511.75	173	1609	S577	8172.25	53	1644	GRID15	7832.75	413
1575	S552	8502.05	293	1610	S578	8162.55	173	1645	S604	7823.05	53
1576	RX[428]	8492.35	413	1611	S579	8152.85	293	1646	S605	7813.35	173
1577	S553	8482.65	53	1612	RX[419]	8143.15	413	1647	S606	7803.65	293
1578	S554	8472.95	173	1613	S580	8133.45	53	1648	GRID15	7793.95	413
1579	S555	8463.25	293	1614	S581	8123.75	173	1649	S607	7784.25	53
1580	RX[427]	8453.55	413	1615	S582	8114.05	293	1650	S608	7774.55	173
1581	S556	8443.85	53	1616	RX[418]	8104.35	413	1651	S609	7764.85	293
1582	S557	8434.15	173	1617	S583	8094.65	53	1652	RX[416]	7755.15	413
1583	S558	8424.45	293	1618	S584	8084.95	173	1653	S610	7745.45	53
1584	RX[426]	8414.75	413	1619	S585	8075.25	293	1654	S611	7735.75	173
1585	S559	8405.05	53	1620	RX[417]	8065.55	413	1655	S612	7726.05	293
1586	S560	8395.35	173	1621	S586	8055.85	53	1656	RX[415]	7716.35	413
1587	S561	8385.65	293	1622	S587	8046.15	173	1657	S613	7706.65	53
1588	RX[425]	8375.95	413	1623	S588	8036.45	293	1658	S614	7696.95	173
1589	S562	8366.25	53	1624	GRID15	8026.75	413	1659	S615	7687.25	293
1590	S563	8356.55	173	1625	S589	8017.05	53	1660	RX[414]	7677.55	413
1591	S564	8346.85	293	1626	S590	8007.35	173	1661	S616	7667.85	53
1592	RX[424]	8337.15	413	1627	S591	7997.65	293	1662	S617	7658.15	173
1593	S565	8327.45	53	1628	GRID15	7987.95	413	1663	S618	7648.45	293
1594	S566	8317.75	173	1629	S592	7978.25	53	1664	RX[413]	7638.75	413
1595	S567	8308.05	293	1630	S593	7968.55	173	1665	S619	7629.05	53
1596	RX[423]	8298.35	413	1631	S594	7958.85	293	1666	S620	7619.35	173
1597	S568	8288.65	53	1632	GRID15	7949.15	413	1667	S621	7609.65	293
1598	S569	8278.95	173	1633	S595	7939.45	53	1668	RX[412]	7599.95	413
1599	S570	8269.25	293	1634	S596	7929.75	173	1669	S622	7590.25	53
1600	RX[422]	8259.55	413	1635	S597	7920.05	293	1670	S623	7580.55	173
1601	S571	8249.85	53	1636	GRID15	7910.35	413	1671	S624	7570.85	293
1602	S572	8240.15	173	1637	S598	7900.65	53	1672	RX[411]	7561.15	413
1603	S573	8230.45	293	1638	S599	7890.95	173	1673	S625	7551.45	53
1604	RX[421]	8220.75	413	1639	S600	7881.25	293	1674	S626	7541.75	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1675	S627	7532.05	293	1710	S653	7192.55	173	1745	S679	6853.05	53
1676	RX[410]	7522.35	413	1711	S654	7182.85	293	1746	S680	6843.35	173
1677	S628	7512.65	53	1712	RX[401]	7173.15	413	1747	S681	6833.65	293
1678	S629	7502.95	173	1713	S655	7163.45	53	1748	RX[392]	6823.95	413
1679	S630	7493.25	293	1714	S656	7153.75	173	1749	S682	6814.25	53
1680	RX[409]	7483.55	413	1715	S657	7144.05	293	1750	S683	6804.55	173
1681	S631	7473.85	53	1716	RX[400]	7134.35	413	1751	S684	6794.85	293
1682	S632	7464.15	173	1717	S658	7124.65	53	1752	RX[391]	6785.15	413
1683	S633	7454.45	293	1718	S659	7114.95	173	1753	S685	6775.45	53
1684	RX[408]	7444.75	413	1719	S660	7105.25	293	1754	S686	6765.75	173
1685	S634	7435.05	53	1720	RX[399]	7095.55	413	1755	S687	6756.05	293
1686	S635	7425.35	173	1721	S661	7085.85	53	1756	RX[390]	6746.35	413
1687	S636	7415.65	293	1722	S662	7076.15	173	1757	S688	6736.65	53
1688	RX[407]	7405.95	413	1723	S663	7066.45	293	1758	S689	6726.95	173
1689	S637	7396.25	53	1724	RX[398]	7056.75	413	1759	S690	6717.25	293
1690	S638	7386.55	173	1725	S664	7047.05	53	1760	RX[389]	6707.55	413
1691	S639	7376.85	293	1726	S665	7037.35	173	1761	S691	6697.85	53
1692	RX[406]	7367.15	413	1727	S666	7027.65	293	1762	S692	6688.15	173
1693	S640	7357.45	53	1728	RX[397]	7017.95	413	1763	S693	6678.45	293
1694	S641	7347.75	173	1729	S667	7008.25	53	1764	RX[388]	6668.75	413
1695	S642	7338.05	293	1730	S668	6998.55	173	1765	S694	6659.05	53
1696	RX[405]	7328.35	413	1731	S669	6988.85	293	1766	S695	6649.35	173
1697	S643	7318.65	53	1732	RX[396]	6979.15	413	1767	S696	6639.65	293
1698	S644	7308.95	173	1733	S670	6969.45	53	1768	RX[387]	6629.95	413
1699	S645	7299.25	293	1734	S671	6959.75	173	1769	S697	6620.25	53
1700	RX[404]	7289.55	413	1735	S672	6950.05	293	1770	S698	6610.55	173
1701	S646	7279.85	53	1736	RX[395]	6940.35	413	1771	S699	6600.85	293
1702	S647	7270.15	173	1737	S673	6930.65	53	1772	RX[386]	6591.15	413
1703	S648	7260.45	293	1738	S674	6920.95	173	1773	S700	6581.45	53
1704	RX[403]	7250.75	413	1739	S675	6911.25	293	1774	S701	6571.75	173
1705	S649	7241.05	53	1740	RX[394]	6901.55	413	1775	S702	6562.05	293
1706	S650	7231.35	173	1741	S676	6891.85	53	1776	RX[385]	6552.35	413
1707	S651	7221.65	293	1742	S677	6882.15	173	1777	S703	6542.65	53
1708	RX[402]	7211.95	413	1743	S678	6872.45	293	1778	S704	6532.95	173
1709	S652	7202.25	53	1744	RX[393]	6862.75	413	1779	S705	6523.25	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1780	GRID14	6513.55	413	1815	S732	6174.05	293	1850	S758	5834.55	173
1781	S706	6503.85	53	1816	GRID14	6164.35	413	1851	S759	5824.85	293
1782	S707	6494.15	173	1817	S733	6154.65	53	1852	RX[376]	5815.15	413
1783	S708	6484.45	293	1818	S734	6144.95	173	1853	S760	5805.45	53
1784	GRID14	6474.75	413	1819	S735	6135.25	293	1854	S761	5795.75	173
1785	S709	6465.05	53	1820	RX[384]	6125.55	413	1855	S762	5786.05	293
1786	S710	6455.35	173	1821	S736	6115.85	53	1856	RX[375]	5776.35	413
1787	S711	6445.65	293	1822	S737	6106.15	173	1857	S763	5766.65	53
1788	GRID14	6435.95	413	1823	S738	6096.45	293	1858	S764	5756.95	173
1789	S712	6426.25	53	1824	RX[383]	6086.75	413	1859	S765	5747.25	293
1790	S713	6416.55	173	1825	S739	6077.05	53	1860	RX[374]	5737.55	413
1791	S714	6406.85	293	1826	S740	6067.35	173	1861	S766	5727.85	53
1792	GRID14	6397.15	413	1827	S741	6057.65	293	1862	S767	5718.15	173
1793	S715	6387.45	53	1828	RX[382]	6047.95	413	1863	S768	5708.45	293
1794	S716	6377.75	173	1829	S742	6038.25	53	1864	RX[373]	5698.75	413
1795	S717	6368.05	293	1830	S743	6028.55	173	1865	S769	5689.05	53
1796	GRID14	6358.35	413	1831	S744	6018.85	293	1866	S770	5679.35	173
1797	S718	6348.65	53	1832	RX[381]	6009.15	413	1867	S771	5669.65	293
1798	S719	6338.95	173	1833	S745	5999.45	53	1868	RX[372]	5659.95	413
1799	S720	6329.25	293	1834	S746	5989.75	173	1869	S772	5650.25	53
1800	GRID14	6319.55	413	1835	S747	5980.05	293	1870	S773	5640.55	173
1801	S721	6309.85	53	1836	RX[380]	5970.35	413	1871	S774	5630.85	293
1802	S722	6300.15	173	1837	S748	5960.65	53	1872	RX[371]	5621.15	413
1803	S723	6290.45	293	1838	S749	5950.95	173	1873	S775	5611.45	53
1804	GRID14	6280.75	413	1839	S750	5941.25	293	1874	S776	5601.75	173
1805	S724	6271.05	53	1840	RX[379]	5931.55	413	1875	S777	5592.05	293
1806	S725	6261.35	173	1841	S751	5921.85	53	1876	RX[370]	5582.35	413
1807	S726	6251.65	293	1842	S752	5912.15	173	1877	S778	5572.65	53
1808	GRID14	6241.95	413	1843	S753	5902.45	293	1878	S779	5562.95	173
1809	S727	6232.25	53	1844	RX[378]	5892.75	413	1879	S780	5553.25	293
1810	S728	6222.55	173	1845	S754	5883.05	53	1880	RX[369]	5543.55	413
1811	S729	6212.85	293	1846	S755	5873.35	173	1881	S781	5533.85	53
1812	GRID14	6203.15	413	1847	S756	5863.65	293	1882	S782	5524.15	173
1813	S730	6193.45	53	1848	RX[377]	5853.95	413	1883	S783	5514.45	293
1814	S731	6183.75	173	1849	S757	5844.25	53	1884	RX[368]	5504.75	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1885	S784	5495.05	53	1920	RX[359]	5155.55	413	1955	S837	4816.05	293
1886	S785	5485.35	173	1921	S811	5145.85	53	1956	GRID13	4806.35	413
1887	S786	5475.65	293	1922	S812	5136.15	173	1957	S838	4796.65	53
1888	RX[367]	5465.95	413	1923	S813	5126.45	293	1958	S839	4786.95	173
1889	S787	5456.25	53	1924	RX[358]	5116.75	413	1959	S840	4777.25	293
1890	S788	5446.55	173	1925	S814	5107.05	53	1960	GRID13	4767.55	413
1891	S789	5436.85	293	1926	S815	5097.35	173	1961	S841	4757.85	53
1892	RX[366]	5427.15	413	1927	S816	5087.65	293	1962	S842	4748.15	173
1893	S790	5417.45	53	1928	RX[357]	5077.95	413	1963	S843	4738.45	293
1894	S791	5407.75	173	1929	S817	5068.25	53	1964	GRID13	4728.75	413
1895	S792	5398.05	293	1930	S818	5058.55	173	1965	S844	4719.05	53
1896	RX[365]	5388.35	413	1931	S819	5048.85	293	1966	S845	4709.35	173
1897	S793	5378.65	53	1932	RX[356]	5039.15	413	1967	S846	4699.65	293
1898	S794	5368.95	173	1933	S820	5029.45	53	1968	GRID13	4689.95	413
1899	S795	5359.25	293	1934	S821	5019.75	173	1969	S847	4680.25	53
1900	RX[364]	5349.55	413	1935	S822	5010.05	293	1970	S848	4670.55	173
1901	S796	5339.85	53	1936	RX[355]	5000.35	413	1971	S849	4660.85	293
1902	S797	5330.15	173	1937	S823	4990.65	53	1972	GRID13	4651.15	413
1903	S798	5320.45	293	1938	S824	4980.95	173	1973	S850	4641.45	53
1904	RX[363]	5310.75	413	1939	S825	4971.25	293	1974	S851	4631.75	173
1905	S799	5301.05	53	1940	RX[354]	4961.55	413	1975	S852	4622.05	293
1906	S800	5291.35	173	1941	S826	4951.85	53	1976	RX[352]	4612.35	413
1907	S801	5281.65	293	1942	S827	4942.15	173	1977	S853	4602.65	53
1908	RX[362]	5271.95	413	1943	S828	4932.45	293	1978	S854	4592.95	173
1909	S802	5262.25	53	1944	RX[353]	4922.75	413	1979	S855	4583.25	293
1910	S803	5252.55	173	1945	S829	4913.05	53	1980	RX[351]	4573.55	413
1911	S804	5242.85	293	1946	S830	4903.35	173	1981	S856	4563.85	53
1912	RX[361]	5233.15	413	1947	S831	4893.65	293	1982	S857	4554.15	173
1913	S805	5223.45	53	1948	GRID13	4883.95	413	1983	S858	4544.45	293
1914	S806	5213.75	173	1949	S832	4874.25	53	1984	RX[350]	4534.75	413
1915	S807	5204.05	293	1950	S833	4864.55	173	1985	S859	4525.05	53
1916	RX[360]	5194.35	413	1951	S834	4854.85	293	1986	S860	4515.35	173
1917	S808	5184.65	53	1952	GRID13	4845.15	413	1987	S861	4505.65	293
1918	S809	5174.95	173	1953	S835	4835.45	53	1988	RX[349]	4495.95	413
1919	S810	5165.25	293	1954	S836	4825.75	173	1989	S862	4486.25	53

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1990	S863	4476.55	173	2025	S889	4137.05	53	2060	RX[331]	3797.55	413
1991	S864	4466.85	293	2026	S890	4127.35	173	2061	S916	3787.85	53
1992	RX[348]	4457.15	413	2027	S891	4117.65	293	2062	S917	3778.15	173
1993	S865	4447.45	53	2028	RX[339]	4107.95	413	2063	S918	3768.45	293
1994	S866	4437.75	173	2029	S892	4098.25	53	2064	RX[330]	3758.75	413
1995	S867	4428.05	293	2030	S893	4088.55	173	2065	S919	3749.05	53
1996	RX[347]	4418.35	413	2031	S894	4078.85	293	2066	S920	3739.35	173
1997	S868	4408.65	53	2032	RX[338]	4069.15	413	2067	S921	3729.65	293
1998	S869	4398.95	173	2033	S895	4059.45	53	2068	RX[329]	3719.95	413
1999	S870	4389.25	293	2034	S896	4049.75	173	2069	S922	3710.25	53
2000	RX[346]	4379.55	413	2035	S897	4040.05	293	2070	S923	3700.55	173
2001	S871	4369.85	53	2036	RX[337]	4030.35	413	2071	S924	3690.85	293
2002	S872	4360.15	173	2037	S898	4020.65	53	2072	RX[328]	3681.15	413
2003	S873	4350.45	293	2038	S899	4010.95	173	2073	S925	3671.45	53
2004	RX[345]	4340.75	413	2039	S900	4001.25	293	2074	S926	3661.75	173
2005	S874	4331.05	53	2040	RX[336]	3991.55	413	2075	S927	3652.05	293
2006	S875	4321.35	173	2041	S901	3981.85	53	2076	RX[327]	3642.35	413
2007	S876	4311.65	293	2042	S902	3972.15	173	2077	S928	3632.65	53
2008	RX[344]	4301.95	413	2043	S903	3962.45	293	2078	S929	3622.95	173
2009	S877	4292.25	53	2044	RX[335]	3952.75	413	2079	S930	3613.25	293
2010	S878	4282.55	173	2045	S904	3943.05	53	2080	RX[326]	3603.55	413
2011	S879	4272.85	293	2046	S905	3933.35	173	2081	S931	3593.85	53
2012	RX[343]	4263.15	413	2047	S906	3923.65	293	2082	S932	3584.15	173
2013	S880	4253.45	53	2048	RX[334]	3913.95	413	2083	S933	3574.45	293
2014	S881	4243.75	173	2049	S907	3904.25	53	2084	RX[325]	3564.75	413
2015	S882	4234.05	293	2050	S908	3894.55	173	2085	S934	3555.05	53
2016	RX[342]	4224.35	413	2051	S909	3884.85	293	2086	S935	3545.35	173
2017	S883	4214.65	53	2052	RX[333]	3875.15	413	2087	S936	3535.65	293
2018	S884	4204.95	173	2053	S910	3865.45	53	2088	RX[324]	3525.95	413
2019	S885	4195.25	293	2054	S911	3855.75	173	2089	S937	3516.25	53
2020	RX[341]	4185.55	413	2055	S912	3846.05	293	2090	S938	3506.55	173
2021	S886	4175.85	53	2056	RX[332]	3836.35	413	2091	S939	3496.85	293
2022	S887	4166.15	173	2057	S913	3826.65	53	2092	RX[323]	3487.15	413
2023	S888	4156.45	293	2058	S914	3816.95	173	2093	S940	3477.45	53
2024	RX[340]	4146.75	413	2059	S915	3807.25	293	2094	S941	3467.75	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2095	S942	3458.05	293	2130	S968	3118.55	173	2165	S994	2779.05	53
2096	RX[322]	3448.35	413	2131	S969	3108.85	293	2166	S995	2769.35	173
2097	S943	3438.65	53	2132	RX[320]	3099.15	413	2167	S996	2759.65	293
2098	S944	3428.95	173	2133	S970	3089.45	53	2168	RX[311]	2749.95	413
2099	S945	3419.25	293	2134	S971	3079.75	173	2169	S997	2740.25	53
2100	RX[321]	3409.55	413	2135	S972	3070.05	293	2170	S998	2730.55	173
2101	S946	3399.85	53	2136	RX[319]	3060.35	413	2171	S999	2720.85	293
2102	S947	3390.15	173	2137	S973	3050.65	53	2172	RX[310]	2711.15	413
2103	S948	3380.45	293	2138	S974	3040.95	173	2173	S1000	2701.45	53
2104	GRID12	3370.75	413	2139	S975	3031.25	293	2174	S1001	2691.75	173
2105	S949	3361.05	53	2140	RX[318]	3021.55	413	2175	S1002	2682.05	293
2106	S950	3351.35	173	2141	S976	3011.85	53	2176	RX[309]	2672.35	413
2107	S951	3341.65	293	2142	S977	3002.15	173	2177	S1003	2662.65	53
2108	GRID12	3331.95	413	2143	S978	2992.45	293	2178	S1004	2652.95	173
2109	S952	3322.25	53	2144	RX[317]	2982.75	413	2179	S1005	2643.25	293
2110	S953	3312.55	173	2145	S979	2973.05	53	2180	RX[308]	2633.55	413
2111	S954	3302.85	293	2146	S980	2963.35	173	2181	S1006	2623.85	53
2112	GRID12	3293.15	413	2147	S981	2953.65	293	2182	S1007	2614.15	173
2113	S955	3283.45	53	2148	RX[316]	2943.95	413	2183	S1008	2604.45	293
2114	S956	3273.75	173	2149	S982	2934.25	53	2184	RX[307]	2594.75	413
2115	S957	3264.05	293	2150	S983	2924.55	173	2185	S1009	2585.05	53
2116	GRID12	3254.35	413	2151	S984	2914.85	293	2186	S1010	2575.35	173
2117	S958	3244.65	53	2152	RX[315]	2905.15	413	2187	S1011	2565.65	293
2118	S959	3234.95	173	2153	S985	2895.45	53	2188	RX[306]	2555.95	413
2119	S960	3225.25	293	2154	S986	2885.75	173	2189	S1012	2546.25	53
2120	GRID12	3215.55	413	2155	S987	2876.05	293	2190	S1013	2536.55	173
2121	S961	3205.85	53	2156	RX[314]	2866.35	413	2191	S1014	2526.85	293
2122	S962	3196.15	173	2157	S988	2856.65	53	2192	RX[305]	2517.15	413
2123	S963	3186.45	293	2158	S989	2846.95	173	2193	S1015	2507.45	53
2124	GRID12	3176.75	413	2159	S990	2837.25	293	2194	S1016	2497.75	173
2125	S964	3167.05	53	2160	RX[313]	2827.55	413	2195	S1017	2488.05	293
2126	S965	3157.35	173	2161	S991	2817.85	53	2196	RX[304]	2478.35	413
2127	S966	3147.65	293	2162	S992	2808.15	173	2197	S1018	2468.65	53
2128	GRID12	3137.95	413	2163	S993	2798.45	293	2198	S1019	2458.95	173
2129	S967	3128.25	53	2164	RX[312]	2788.75	413	2199	S1020	2449.25	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2200	RX[303]	2439.55	413	2235	S1047	2100.05	293	2270	S1073	1760.55	173
2201	S1021	2429.85	53	2236	RX[294]	2090.35	413	2271	S1074	1750.85	293
2202	S1022	2420.15	173	2237	S1048	2080.65	53	2272	GRID11	1741.15	413
2203	S1023	2410.45	293	2238	S1049	2070.95	173	2273	S1075	1731.45	53
2204	RX[302]	2400.75	413	2239	S1050	2061.25	293	2274	S1076	1721.75	173
2205	S1024	2391.05	53	2240	RX[293]	2051.55	413	2275	S1077	1712.05	293
2206	S1025	2381.35	173	2241	S1051	2041.85	53	2276	GRID11	1702.35	413
2207	S1026	2371.65	293	2242	S1052	2032.15	173	2277	S1078	1692.65	53
2208	RX[301]	2361.95	413	2243	S1053	2022.45	293	2278	S1079	1682.95	173
2209	S1027	2352.25	53	2244	RX[292]	2012.75	413	2279	S1080	1673.25	293
2210	S1028	2342.55	173	2245	S1054	2003.05	53	2280	GRID11	1663.55	413
2211	S1029	2332.85	293	2246	S1055	1993.35	173	2281	DUMMY	1653.85	53
2212	RX[300]	2323.15	413	2247	S1056	1983.65	293	2282	DUMMY	1644.15	173
2213	S1030	2313.45	53	2248	RX[291]	1973.95	413	2283	DUMMY	1634.45	293
2214	S1031	2303.75	173	2249	S1057	1964.25	53	2284	DUMMY	1624.75	413
2215	S1032	2294.05	293	2250	S1058	1954.55	173	2285	DUMMY	1615.05	53
2216	RX[299]	2284.35	413	2251	S1059	1944.85	293	2286	DUMMY	1605.35	173
2217	S1033	2274.65	53	2252	RX[290]	1935.15	413	2287	DUMMY	1595.65	293
2218	S1034	2264.95	173	2253	S1060	1925.45	53	2288	DUMMY	1585.95	413
2219	S1035	2255.25	293	2254	S1061	1915.75	173	2289	DUMMY	1576.25	53
2220	RX[298]	2245.55	413	2255	S1062	1906.05	293	2290	DUMMY	1566.55	173
2221	S1036	2235.85	53	2256	RX[289]	1896.35	413	2291	DUMMY	1556.85	293
2222	S1037	2226.15	173	2257	S1063	1886.65	53	2292	DUMMY	1547.15	413
2223	S1038	2216.45	293	2258	S1064	1876.95	173	2293	DUMMY	1537.45	53
2224	RX[297]	2206.75	413	2259	S1065	1867.25	293	2294	DUMMY	1527.75	173
2225	S1039	2197.05	53	2260	GRID11	1857.55	413	2295	DUMMY	1518.05	293
2226	S1040	2187.35	173	2261	S1066	1847.85	53	2296	DUMMY	1508.35	413
2227	S1041	2177.65	293	2262	S1067	1838.15	173	2297	DUMMY	1498.65	53
2228	RX[296]	2167.95	413	2263	S1068	1828.45	293	2298	DUMMY	1488.95	173
2229	S1042	2158.25	53	2264	GRID11	1818.75	413	2299	DUMMY	1479.25	293
2230	S1043	2148.55	173	2265	S1069	1809.05	53	2300	DUMMY	1469.55	413
2231	S1044	2138.85	293	2266	S1070	1799.35	173	2301	DUMMY	1459.85	53
2232	RX[295]	2129.15	413	2267	S1071	1789.65	293	2302	DUMMY	1450.15	173
2233	S1045	2119.45	53	2268	GRID11	1779.95	413	2303	DUMMY	1440.45	293
2234	S1046	2109.75	173	2269	S1072	1770.25	53	2304	DUMMY	1430.75	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2305	DUMMY	1421.05	53	2340	DUMMY	1081.55	413	2375	DUMMY	742.05	293
2306	DUMMY	1411.35	173	2341	DUMMY	1071.85	53	2376	DUMMY	732.35	413
2307	DUMMY	1401.65	293	2342	DUMMY	1062.15	173	2377	DUMMY	722.65	53
2308	DUMMY	1391.95	413	2343	DUMMY	1052.45	293	2378	DUMMY	712.95	173
2309	DUMMY	1382.25	53	2344	DUMMY	1042.75	413	2379	DUMMY	703.25	293
2310	DUMMY	1372.55	173	2345	DUMMY	1033.05	53	2380	DUMMY	693.55	413
2311	DUMMY	1362.85	293	2346	DUMMY	1023.35	173	2381	DUMMY	683.85	53
2312	DUMMY	1353.15	413	2347	DUMMY	1013.65	293	2382	DUMMY	674.15	173
2313	DUMMY	1343.45	53	2348	DUMMY	1003.95	413	2383	DUMMY	664.45	293
2314	DUMMY	1333.75	173	2349	DUMMY	994.25	53	2384	DUMMY	654.75	413
2315	DUMMY	1324.05	293	2350	DUMMY	984.55	173	2385	DUMMY	645.05	53
2316	DUMMY	1314.35	413	2351	DUMMY	974.85	293	2386	DUMMY	635.35	173
2317	DUMMY	1304.65	53	2352	DUMMY	965.15	413	2387	DUMMY	625.65	293
2318	DUMMY	1294.95	173	2353	DUMMY	955.45	53	2388	DUMMY	615.95	413
2319	DUMMY	1285.25	293	2354	DUMMY	945.75	173	2389	DUMMY	606.25	53
2320	DUMMY	1275.55	413	2355	DUMMY	936.05	293	2390	DUMMY	596.55	173
2321	DUMMY	1265.85	53	2356	DUMMY	926.35	413	2391	DUMMY	586.85	293
2322	DUMMY	1256.15	173	2357	DUMMY	916.65	53	2392	DUMMY	577.15	413
2323	DUMMY	1246.45	293	2358	DUMMY	906.95	173	2393	DUMMY	567.45	53
2324	DUMMY	1236.75	413	2359	DUMMY	897.25	293	2394	DUMMY	557.75	173
2325	DUMMY	1227.05	53	2360	DUMMY	887.55	413	2395	DUMMY	548.05	293
2326	DUMMY	1217.35	173	2361	DUMMY	877.85	53	2396	DUMMY	538.35	413
2327	DUMMY	1207.65	293	2362	DUMMY	868.15	173	2397	DUMMY	528.65	53
2328	DUMMY	1197.95	413	2363	DUMMY	858.45	293	2398	DUMMY	518.95	173
2329	DUMMY	1188.25	53	2364	DUMMY	848.75	413	2399	DUMMY	509.25	293
2330	DUMMY	1178.55	173	2365	DUMMY	839.05	53	2400	DUMMY	499.55	413
2331	DUMMY	1168.85	293	2366	DUMMY	829.35	173	2401	DUMMY	489.85	53
2332	DUMMY	1159.15	413	2367	DUMMY	819.65	293	2402	DUMMY	480.15	173
2333	DUMMY	1149.45	53	2368	DUMMY	809.95	413	2403	DUMMY	470.45	293
2334	DUMMY	1139.75	173	2369	DUMMY	800.25	53	2404	DUMMY	460.75	413
2335	DUMMY	1130.05	293	2370	DUMMY	790.55	173	2405	DUMMY	451.05	53
2336	DUMMY	1120.35	413	2371	DUMMY	780.85	293	2406	DUMMY	441.35	173
2337	DUMMY	1110.65	53	2372	DUMMY	771.15	413	2407	DUMMY	431.65	293
2338	DUMMY	1100.95	173	2373	DUMMY	761.45	53	2408	DUMMY	421.95	413
2339	DUMMY	1091.25	293	2374	DUMMY	751.75	173	2409	DUMMY	412.25	53

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2410	DUMMY	402.55	173	2445	DUMMY	63.05	53	2480	DUMMY	-276.45	413
2411	DUMMY	392.85	293	2446	DUMMY	53.35	173	2481	DUMMY	-286.15	53
2412	DUMMY	383.15	413	2447	DUMMY	43.65	293	2482	DUMMY	-295.85	173
2413	DUMMY	373.45	53	2448	DUMMY	33.95	413	2483	DUMMY	-305.55	293
2414	DUMMY	363.75	173	2449	DUMMY	24.25	53	2484	DUMMY	-315.25	413
2415	DUMMY	354.05	293	2450	DUMMY	14.55	173	2485	DUMMY	-324.95	53
2416	DUMMY	344.35	413	2451	DUMMY	4.85	293	2486	DUMMY	-334.65	173
2417	DUMMY	334.65	53	2452	DUMMY	-4.85	413	2487	DUMMY	-344.35	293
2418	DUMMY	324.95	173	2453	DUMMY	-14.55	53	2488	DUMMY	-354.05	413
2419	DUMMY	315.25	293	2454	DUMMY	-24.25	173	2489	DUMMY	-363.75	53
2420	DUMMY	305.55	413	2455	DUMMY	-33.95	293	2490	DUMMY	-373.45	173
2421	DUMMY	295.85	53	2456	DUMMY	-43.65	413	2491	DUMMY	-383.15	293
2422	DUMMY	286.15	173	2457	DUMMY	-53.35	53	2492	DUMMY	-392.85	413
2423	DUMMY	276.45	293	2458	DUMMY	-63.05	173	2493	DUMMY	-402.55	53
2424	DUMMY	266.75	413	2459	DUMMY	-72.75	293	2494	DUMMY	-412.25	173
2425	DUMMY	257.05	53	2460	DUMMY	-82.45	413	2495	DUMMY	-421.95	293
2426	DUMMY	247.35	173	2461	DUMMY	-92.15	53	2496	DUMMY	-431.65	413
2427	DUMMY	237.65	293	2462	DUMMY	-101.85	173	2497	DUMMY	-441.35	53
2428	DUMMY	227.95	413	2463	DUMMY	-111.55	293	2498	DUMMY	-451.05	173
2429	DUMMY	218.25	53	2464	DUMMY	-121.25	413	2499	DUMMY	-460.75	293
2430	DUMMY	208.55	173	2465	DUMMY	-130.95	53	2500	DUMMY	-470.45	413
2431	DUMMY	198.85	293	2466	DUMMY	-140.65	173	2501	DUMMY	-480.15	53
2432	DUMMY	189.15	413	2467	DUMMY	-150.35	293	2502	DUMMY	-489.85	173
2433	DUMMY	179.45	53	2468	DUMMY	-160.05	413	2503	DUMMY	-499.55	293
2434	DUMMY	169.75	173	2469	DUMMY	-169.75	53	2504	DUMMY	-509.25	413
2435	DUMMY	160.05	293	2470	DUMMY	-179.45	173	2505	DUMMY	-518.95	53
2436	DUMMY	150.35	413	2471	DUMMY	-189.15	293	2506	DUMMY	-528.65	173
2437	DUMMY	140.65	53	2472	DUMMY	-198.85	413	2507	DUMMY	-538.35	293
2438	DUMMY	130.95	173	2473	DUMMY	-208.55	53	2508	DUMMY	-548.05	413
2439	DUMMY	121.25	293	2474	DUMMY	-218.25	173	2509	DUMMY	-557.75	53
2440	DUMMY	111.55	413	2475	DUMMY	-227.95	293	2510	DUMMY	-567.45	173
2441	DUMMY	101.85	53	2476	DUMMY	-237.65	413	2511	DUMMY	-577.15	293
2442	DUMMY	92.15	173	2477	DUMMY	-247.35	53	2512	DUMMY	-586.85	413
2443	DUMMY	82.45	293	2478	DUMMY	-257.05	173	2513	DUMMY	-596.55	53
2444	DUMMY	72.75	413	2479	DUMMY	-266.75	293	2514	DUMMY	-606.25	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2515	DUMMY	-615.95	293	2550	DUMMY	-955.45	173	2585	DUMMY	-1294.95	53
2516	DUMMY	-625.65	413	2551	DUMMY	-965.15	293	2586	DUMMY	-1304.65	173
2517	DUMMY	-635.35	53	2552	DUMMY	-974.85	413	2587	DUMMY	-1314.35	293
2518	DUMMY	-645.05	173	2553	DUMMY	-984.55	53	2588	DUMMY	-1324.05	413
2519	DUMMY	-654.75	293	2554	DUMMY	-994.25	173	2589	DUMMY	-1333.75	53
2520	DUMMY	-664.45	413	2555	DUMMY	-1003.95	293	2590	DUMMY	-1343.45	173
2521	DUMMY	-674.15	53	2556	DUMMY	-1013.65	413	2591	DUMMY	-1353.15	293
2522	DUMMY	-683.85	173	2557	DUMMY	-1023.35	53	2592	DUMMY	-1362.85	413
2523	DUMMY	-693.55	293	2558	DUMMY	-1033.05	173	2593	DUMMY	-1372.55	53
2524	DUMMY	-703.25	413	2559	DUMMY	-1042.75	293	2594	DUMMY	-1382.25	173
2525	DUMMY	-712.95	53	2560	DUMMY	-1052.45	413	2595	DUMMY	-1391.95	293
2526	DUMMY	-722.65	173	2561	DUMMY	-1062.15	53	2596	DUMMY	-1401.65	413
2527	DUMMY	-732.35	293	2562	DUMMY	-1071.85	173	2597	DUMMY	-1411.35	53
2528	DUMMY	-742.05	413	2563	DUMMY	-1081.55	293	2598	DUMMY	-1421.05	173
2529	DUMMY	-751.75	53	2564	DUMMY	-1091.25	413	2599	DUMMY	-1430.75	293
2530	DUMMY	-761.45	173	2565	DUMMY	-1100.95	53	2600	DUMMY	-1440.45	413
2531	DUMMY	-771.15	293	2566	DUMMY	-1110.65	173	2601	DUMMY	-1450.15	53
2532	DUMMY	-780.85	413	2567	DUMMY	-1120.35	293	2602	DUMMY	-1459.85	173
2533	DUMMY	-790.55	53	2568	DUMMY	-1130.05	413	2603	DUMMY	-1469.55	293
2534	DUMMY	-800.25	173	2569	DUMMY	-1139.75	53	2604	DUMMY	-1479.25	413
2535	DUMMY	-809.95	293	2570	DUMMY	-1149.45	173	2605	DUMMY	-1488.95	53
2536	DUMMY	-819.65	413	2571	DUMMY	-1159.15	293	2606	DUMMY	-1498.65	173
2537	DUMMY	-829.35	53	2572	DUMMY	-1168.85	413	2607	DUMMY	-1508.35	293
2538	DUMMY	-839.05	173	2573	DUMMY	-1178.55	53	2608	DUMMY	-1518.05	413
2539	DUMMY	-848.75	293	2574	DUMMY	-1188.25	173	2609	DUMMY	-1527.75	53
2540	DUMMY	-858.45	413	2575	DUMMY	-1197.95	293	2610	DUMMY	-1537.45	173
2541	DUMMY	-868.15	53	2576	DUMMY	-1207.65	413	2611	DUMMY	-1547.15	293
2542	DUMMY	-877.85	173	2577	DUMMY	-1217.35	53	2612	DUMMY	-1556.85	413
2543	DUMMY	-887.55	293	2578	DUMMY	-1227.05	173	2613	DUMMY	-1566.55	53
2544	DUMMY	-897.25	413	2579	DUMMY	-1236.75	293	2614	DUMMY	-1576.25	173
2545	DUMMY	-906.95	53	2580	DUMMY	-1246.45	413	2615	DUMMY	-1585.95	293
2546	DUMMY	-916.65	173	2581	DUMMY	-1256.15	53	2616	DUMMY	-1595.65	413
2547	DUMMY	-926.35	293	2582	DUMMY	-1265.85	173	2617	DUMMY	-1605.35	53
2548	DUMMY	-936.05	413	2583	DUMMY	-1275.55	293	2618	DUMMY	-1615.05	173
2549	DUMMY	-945.75	53	2584	DUMMY	-1285.25	413	2619	DUMMY	-1624.75	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2620	DUMMY	-1634.45	413	2655	S1104	-1973.95	293	2690	S1130	-2313.45	173
2621	DUMMY	-1644.15	53	2656	RX[286]	-1983.65	413	2691	S1131	-2323.15	293
2622	DUMMY	-1653.85	173	2657	S1105	-1993.35	53	2692	RX[277]	-2332.85	413
2623	DUMMY	-1663.55	293	2658	S1106	-2003.05	173	2693	S1132	-2342.55	53
2624	DUMMY	-1673.25	413	2659	S1107	-2012.75	293	2694	S1133	-2352.25	173
2625	S1081	-1682.95	53	2660	RX[285]	-2022.45	413	2695	S1134	-2361.95	293
2626	S1082	-1692.65	173	2661	S1108	-2032.15	53	2696	RX[276]	-2371.65	413
2627	S1083	-1702.35	293	2662	S1109	-2041.85	173	2697	S1135	-2381.35	53
2628	GRID10	-1712.05	413	2663	S1110	-2051.55	293	2698	S1136	-2391.05	173
2629	S1084	-1721.75	53	2664	RX[284]	-2061.25	413	2699	S1137	-2400.75	293
2630	S1085	-1731.45	173	2665	S1111	-2070.95	53	2700	RX[275]	-2410.45	413
2631	S1086	-1741.15	293	2666	S1112	-2080.65	173	2701	S1138	-2420.15	53
2632	GRID10	-1750.85	413	2667	S1113	-2090.35	293	2702	S1139	-2429.85	173
2633	S1087	-1760.55	53	2668	RX[283]	-2100.05	413	2703	S1140	-2439.55	293
2634	S1088	-1770.25	173	2669	S1114	-2109.75	53	2704	RX[274]	-2449.25	413
2635	S1089	-1779.95	293	2670	S1115	-2119.45	173	2705	S1141	-2458.95	53
2636	GRID10	-1789.65	413	2671	S1116	-2129.15	293	2706	S1142	-2468.65	173
2637	S1090	-1799.35	53	2672	RX[282]	-2138.85	413	2707	S1143	-2478.35	293
2638	S1091	-1809.05	173	2673	S1117	-2148.55	53	2708	RX[273]	-2488.05	413
2639	S1092	-1818.75	293	2674	S1118	-2158.25	173	2709	S1144	-2497.75	53
2640	GRID10	-1828.45	413	2675	S1119	-2167.95	293	2710	S1145	-2507.45	173
2641	S1093	-1838.15	53	2676	RX[281]	-2177.65	413	2711	S1146	-2517.15	293
2642	S1094	-1847.85	173	2677	S1120	-2187.35	53	2712	RX[272]	-2526.85	413
2643	S1095	-1857.55	293	2678	S1121	-2197.05	173	2713	S1147	-2536.55	53
2644	GRID10	-1867.25	413	2679	S1122	-2206.75	293	2714	S1148	-2546.25	173
2645	S1096	-1876.95	53	2680	RX[280]	-2216.45	413	2715	S1149	-2555.95	293
2646	S1097	-1886.65	173	2681	S1123	-2226.15	53	2716	RX[271]	-2565.65	413
2647	S1098	-1896.35	293	2682	S1124	-2235.85	173	2717	S1150	-2575.35	53
2648	RX[288]	-1906.05	413	2683	S1125	-2245.55	293	2718	S1151	-2585.05	173
2649	S1099	-1915.75	53	2684	RX[279]	-2255.25	413	2719	S1152	-2594.75	293
2650	S1100	-1925.45	173	2685	S1126	-2264.95	53	2720	RX[270]	-2604.45	413
2651	S1101	-1935.15	293	2686	S1127	-2274.65	173	2721	S1153	-2614.15	53
2652	RX[287]	-1944.85	413	2687	S1128	-2284.35	293	2722	S1154	-2623.85	173
2653	S1102	-1954.55	53	2688	RX[278]	-2294.05	413	2723	S1155	-2633.55	293
2654	S1103	-1964.25	173	2689	S1129	-2303.75	53	2724	RX[269]	-2643.25	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2725	S1156	-2652.95	53	2760	RX[260]	-2992.45	413	2795	S1209	-3331.95	293
2726	S1157	-2662.65	173	2761	S1183	-3002.15	53	2796	GRID9	-3341.65	413
2727	S1158	-2672.35	293	2762	S1184	-3011.85	173	2797	S1210	-3351.35	53
2728	RX[268]	-2682.05	413	2763	S1185	-3021.55	293	2798	S1211	-3361.05	173
2729	S1159	-2691.75	53	2764	RX[259]	-3031.25	413	2799	S1212	-3370.75	293
2730	S1160	-2701.45	173	2765	S1186	-3040.95	53	2800	GRID9	-3380.45	413
2731	S1161	-2711.15	293	2766	S1187	-3050.65	173	2801	S1213	-3390.15	53
2732	RX[267]	-2720.85	413	2767	S1188	-3060.35	293	2802	S1214	-3399.85	173
2733	S1162	-2730.55	53	2768	RX[258]	-3070.05	413	2803	S1215	-3409.55	293
2734	S1163	-2740.25	173	2769	S1189	-3079.75	53	2804	RX[256]	-3419.25	413
2735	S1164	-2749.95	293	2770	S1190	-3089.45	173	2805	S1216	-3428.95	53
2736	RX[266]	-2759.65	413	2771	S1191	-3099.15	293	2806	S1217	-3438.65	173
2737	S1165	-2769.35	53	2772	RX[257]	-3108.85	413	2807	S1218	-3448.35	293
2738	S1166	-2779.05	173	2773	S1192	-3118.55	53	2808	RX[255]	-3458.05	413
2739	S1167	-2788.75	293	2774	S1193	-3128.25	173	2809	S1219	-3467.75	53
2740	RX[265]	-2798.45	413	2775	S1194	-3137.95	293	2810	S1220	-3477.45	173
2741	S1168	-2808.15	53	2776	GRID9	-3147.65	413	2811	S1221	-3487.15	293
2742	S1169	-2817.85	173	2777	S1195	-3157.35	53	2812	RX[254]	-3496.85	413
2743	S1170	-2827.55	293	2778	S1196	-3167.05	173	2813	S1222	-3506.55	53
2744	RX[264]	-2837.25	413	2779	S1197	-3176.75	293	2814	S1223	-3516.25	173
2745	S1171	-2846.95	53	2780	GRID9	-3186.45	413	2815	S1224	-3525.95	293
2746	S1172	-2856.65	173	2781	S1198	-3196.15	53	2816	RX[253]	-3535.65	413
2747	S1173	-2866.35	293	2782	S1199	-3205.85	173	2817	S1225	-3545.35	53
2748	RX[263]	-2876.05	413	2783	S1200	-3215.55	293	2818	S1226	-3555.05	173
2749	S1174	-2885.75	53	2784	GRID9	-3225.25	413	2819	S1227	-3564.75	293
2750	S1175	-2895.45	173	2785	S1201	-3234.95	53	2820	RX[252]	-3574.45	413
2751	S1176	-2905.15	293	2786	S1202	-3244.65	173	2821	S1228	-3584.15	53
2752	RX[262]	-2914.85	413	2787	S1203	-3254.35	293	2822	S1229	-3593.85	173
2753	S1177	-2924.55	53	2788	GRID9	-3264.05	413	2823	S1230	-3603.55	293
2754	S1178	-2934.25	173	2789	S1204	-3273.75	53	2824	RX[251]	-3613.25	413
2755	S1179	-2943.95	293	2790	S1205	-3283.45	173	2825	S1231	-3622.95	53
2756	RX[261]	-2953.65	413	2791	S1206	-3293.15	293	2826	S1232	-3632.65	173
2757	S1180	-2963.35	53	2792	GRID9	-3302.85	413	2827	S1233	-3642.35	293
2758	S1181	-2973.05	173	2793	S1207	-3312.55	53	2828	RX[250]	-3652.05	413
2759	S1182	-2982.75	293	2794	S1208	-3322.25	173	2829	S1234	-3661.75	53

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2830	S1235	-3671.45	173	2865	S1261	-4010.95	53	2900	RX[232]	-4350.45	413
2831	S1236	-3681.15	293	2866	S1262	-4020.65	173	2901	S1288	-4360.15	53
2832	RX[249]	-3690.85	413	2867	S1263	-4030.35	293	2902	S1289	-4369.85	173
2833	S1237	-3700.55	53	2868	RX[240]	-4040.05	413	2903	S1290	-4379.55	293
2834	S1238	-3710.25	173	2869	S1264	-4049.75	53	2904	RX[231]	-4389.25	413
2835	S1239	-3719.95	293	2870	S1265	-4059.45	173	2905	S1291	-4398.95	53
2836	RX[248]	-3729.65	413	2871	S1266	-4069.15	293	2906	S1292	-4408.65	173
2837	S1240	-3739.35	53	2872	RX[239]	-4078.85	413	2907	S1293	-4418.35	293
2838	S1241	-3749.05	173	2873	S1267	-4088.55	53	2908	RX[230]	-4428.05	413
2839	S1242	-3758.75	293	2874	S1268	-4098.25	173	2909	S1294	-4437.75	53
2840	RX[247]	-3768.45	413	2875	S1269	-4107.95	293	2910	S1295	-4447.45	173
2841	S1243	-3778.15	53	2876	RX[238]	-4117.65	413	2911	S1296	-4457.15	293
2842	S1244	-3787.85	173	2877	S1270	-4127.35	53	2912	RX[229]	-4466.85	413
2843	S1245	-3797.55	293	2878	S1271	-4137.05	173	2913	S1297	-4476.55	53
2844	RX[246]	-3807.25	413	2879	S1272	-4146.75	293	2914	S1298	-4486.25	173
2845	S1246	-3816.95	53	2880	RX[237]	-4156.45	413	2915	S1299	-4495.95	293
2846	S1247	-3826.65	173	2881	S1273	-4166.15	53	2916	RX[228]	-4505.65	413
2847	S1248	-3836.35	293	2882	S1274	-4175.85	173	2917	S1300	-4515.35	53
2848	RX[245]	-3846.05	413	2883	S1275	-4185.55	293	2918	S1301	-4525.05	173
2849	S1249	-3855.75	53	2884	RX[236]	-4195.25	413	2919	S1302	-4534.75	293
2850	S1250	-3865.45	173	2885	S1276	-4204.95	53	2920	RX[227]	-4544.45	413
2851	S1251	-3875.15	293	2886	S1277	-4214.65	173	2921	S1303	-4554.15	53
2852	RX[244]	-3884.85	413	2887	S1278	-4224.35	293	2922	S1304	-4563.85	173
2853	S1252	-3894.55	53	2888	RX[235]	-4234.05	413	2923	S1305	-4573.55	293
2854	S1253	-3904.25	173	2889	S1279	-4243.75	53	2924	RX[226]	-4583.25	413
2855	S1254	-3913.95	293	2890	S1280	-4253.45	173	2925	S1306	-4592.95	53
2856	RX[243]	-3923.65	413	2891	S1281	-4263.15	293	2926	S1307	-4602.65	173
2857	S1255	-3933.35	53	2892	RX[234]	-4272.85	413	2927	S1308	-4612.35	293
2858	S1256	-3943.05	173	2893	S1282	-4282.55	53	2928	RX[225]	-4622.05	413
2859	S1257	-3952.75	293	2894	S1283	-4292.25	173	2929	S1309	-4631.75	53
2860	RX[242]	-3962.45	413	2895	S1284	-4301.95	293	2930	S1310	-4641.45	173
2861	S1258	-3972.15	53	2896	RX[233]	-4311.65	413	2931	S1311	-4651.15	293
2862	S1259	-3981.85	173	2897	S1285	-4321.35	53	2932	GRID8	-4660.85	413
2863	S1260	-3991.55	293	2898	S1286	-4331.05	173	2933	S1312	-4670.55	53
2864	RX[241]	-4001.25	413	2899	S1287	-4340.75	293	2934	S1313	-4680.25	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
2935	S1314	-4689.95	293	2970	S1340	-5029.45	173	3005	S1366	-5368.95	53
2936	GRID8	-4699.65	413	2971	S1341	-5039.15	293	3006	S1367	-5378.65	173
2937	S1315	-4709.35	53	2972	RX[221]	-5048.85	413	3007	S1368	-5388.35	293
2938	S1316	-4719.05	173	2973	S1342	-5058.55	53	3008	RX[212]	-5398.05	413
2939	S1317	-4728.75	293	2974	S1343	-5068.25	173	3009	S1369	-5407.75	53
2940	GRID8	-4738.45	413	2975	S1344	-5077.95	293	3010	S1370	-5417.45	173
2941	S1318	-4748.15	53	2976	RX[220]	-5087.65	413	3011	S1371	-5427.15	293
2942	S1319	-4757.85	173	2977	S1345	-5097.35	53	3012	RX[211]	-5436.85	413
2943	S1320	-4767.55	293	2978	S1346	-5107.05	173	3013	S1372	-5446.55	53
2944	GRID8	-4777.25	413	2979	S1347	-5116.75	293	3014	S1373	-5456.25	173
2945	S1321	-4786.95	53	2980	RX[219]	-5126.45	413	3015	S1374	-5465.95	293
2946	S1322	-4796.65	173	2981	S1348	-5136.15	53	3016	RX[210]	-5475.65	413
2947	S1323	-4806.35	293	2982	S1349	-5145.85	173	3017	S1375	-5485.35	53
2948	GRID8	-4816.05	413	2983	S1350	-5155.55	293	3018	S1376	-5495.05	173
2949	S1324	-4825.75	53	2984	RX[218]	-5165.25	413	3019	S1377	-5504.75	293
2950	S1325	-4835.45	173	2985	S1351	-5174.95	53	3020	RX[209]	-5514.45	413
2951	S1326	-4845.15	293	2986	S1352	-5184.65	173	3021	S1378	-5524.15	53
2952	GRID8	-4854.85	413	2987	S1353	-5194.35	293	3022	S1379	-5533.85	173
2953	S1327	-4864.55	53	2988	RX[217]	-5204.05	413	3023	S1380	-5543.55	293
2954	S1328	-4874.25	173	2989	S1354	-5213.75	53	3024	RX[208]	-5553.25	413
2955	S1329	-4883.95	293	2990	S1355	-5223.45	173	3025	S1381	-5562.95	53
2956	GRID8	-4893.65	413	2991	S1356	-5233.15	293	3026	S1382	-5572.65	173
2957	S1330	-4903.35	53	2992	RX[216]	-5242.85	413	3027	S1383	-5582.35	293
2958	S1331	-4913.05	173	2993	S1357	-5252.55	53	3028	RX[207]	-5592.05	413
2959	S1332	-4922.75	293	2994	S1358	-5262.25	173	3029	S1384	-5601.75	53
2960	RX[224]	-4932.45	413	2995	S1359	-5271.95	293	3030	S1385	-5611.45	173
2961	S1333	-4942.15	53	2996	RX[215]	-5281.65	413	3031	S1386	-5621.15	293
2962	S1334	-4951.85	173	2997	S1360	-5291.35	53	3032	RX[206]	-5630.85	413
2963	S1335	-4961.55	293	2998	S1361	-5301.05	173	3033	S1387	-5640.55	53
2964	RX[223]	-4971.25	413	2999	S1362	-5310.75	293	3034	S1388	-5650.25	173
2965	S1336	-4980.95	53	3000	RX[214]	-5320.45	413	3035	S1389	-5659.95	293
2966	S1337	-4990.65	173	3001	S1363	-5330.15	53	3036	RX[205]	-5669.65	413
2967	S1338	-5000.35	293	3002	S1364	-5339.85	173	3037	S1390	-5679.35	53
2968	RX[222]	-5010.05	413	3003	S1365	-5349.55	293	3038	S1391	-5689.05	173
2969	S1339	-5019.75	53	3004	RX[213]	-5359.25	413	3039	S1392	-5698.75	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3040	RX[204]	-5708.45	413	3075	S1419	-6047.95	293	3110	S1445	-6387.45	173
3041	S1393	-5718.15	53	3076	RX[195]	-6057.65	413	3111	S1446	-6397.15	293
3042	S1394	-5727.85	173	3077	S1420	-6067.35	53	3112	GRID7	-6406.85	413
3043	S1395	-5737.55	293	3078	S1421	-6077.05	173	3113	S1447	-6416.55	53
3044	RX[203]	-5747.25	413	3079	S1422	-6086.75	293	3114	S1448	-6426.25	173
3045	S1396	-5756.95	53	3080	RX[194]	-6096.45	413	3115	S1449	-6435.95	293
3046	S1397	-5766.65	173	3081	S1423	-6106.15	53	3116	GRID7	-6445.65	413
3047	S1398	-5776.35	293	3082	S1424	-6115.85	173	3117	S1450	-6455.35	53
3048	RX[202]	-5786.05	413	3083	S1425	-6125.55	293	3118	S1451	-6465.05	173
3049	S1399	-5795.75	53	3084	RX[193]	-6135.25	413	3119	S1452	-6474.75	293
3050	S1400	-5805.45	173	3085	S1426	-6144.95	53	3120	GRID7	-6484.45	413
3051	S1401	-5815.15	293	3086	S1427	-6154.65	173	3121	S1453	-6494.15	53
3052	RX[201]	-5824.85	413	3087	S1428	-6164.35	293	3122	S1454	-6503.85	173
3053	S1402	-5834.55	53	3088	GRID7	-6174.05	413	3123	S1455	-6513.55	293
3054	S1403	-5844.25	173	3089	S1429	-6183.75	53	3124	GRID7	-6523.25	413
3055	S1404	-5853.95	293	3090	S1430	-6193.45	173	3125	S1456	-6532.95	53
3056	RX[200]	-5863.65	413	3091	S1431	-6203.15	293	3126	S1457	-6542.65	173
3057	S1405	-5873.35	53	3092	GRID7	-6212.85	413	3127	S1458	-6552.35	293
3058	S1406	-5883.05	173	3093	S1432	-6222.55	53	3128	RX[192]	-6562.05	413
3059	S1407	-5892.75	293	3094	S1433	-6232.25	173	3129	S1459	-6571.75	53
3060	RX[199]	-5902.45	413	3095	S1434	-6241.95	293	3130	S1460	-6581.45	173
3061	S1408	-5912.15	53	3096	GRID7	-6251.65	413	3131	S1461	-6591.15	293
3062	S1409	-5921.85	173	3097	S1435	-6261.35	53	3132	RX[191]	-6600.85	413
3063	S1410	-5931.55	293	3098	S1436	-6271.05	173	3133	S1462	-6610.55	53
3064	RX[198]	-5941.25	413	3099	S1437	-6280.75	293	3134	S1463	-6620.25	173
3065	S1411	-5950.95	53	3100	GRID7	-6290.45	413	3135	S1464	-6629.95	293
3066	S1412	-5960.65	173	3101	S1438	-6300.15	53	3136	RX[190]	-6639.65	413
3067	S1413	-5970.35	293	3102	S1439	-6309.85	173	3137	S1465	-6649.35	53
3068	RX[197]	-5980.05	413	3103	S1440	-6319.55	293	3138	S1466	-6659.05	173
3069	S1414	-5989.75	53	3104	GRID7	-6329.25	413	3139	S1467	-6668.75	293
3070	S1415	-5999.45	173	3105	S1441	-6338.95	53	3140	RX[189]	-6678.45	413
3071	S1416	-6009.15	293	3106	S1442	-6348.65	173	3141	S1468	-6688.15	53
3072	RX[196]	-6018.85	413	3107	S1443	-6358.35	293	3142	S1469	-6697.85	173
3073	S1417	-6028.55	53	3108	GRID7	-6368.05	413	3143	S1470	-6707.55	293
3074	S1418	-6038.25	173	3109	S1444	-6377.75	53	3144	RX[188]	-6717.25	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3145	S1471	-6726.95	53	3180	RX[179]	-7066.45	413	3215	S1524	-7405.95	293
3146	S1472	-6736.65	173	3181	S1498	-7076.15	53	3216	RX[170]	-7415.65	413
3147	S1473	-6746.35	293	3182	S1499	-7085.85	173	3217	S1525	-7425.35	53
3148	RX[187]	-6756.05	413	3183	S1500	-7095.55	293	3218	S1526	-7435.05	173
3149	S1474	-6765.75	53	3184	RX[178]	-7105.25	413	3219	S1527	-7444.75	293
3150	S1475	-6775.45	173	3185	S1501	-7114.95	53	3220	RX[169]	-7454.45	413
3151	S1476	-6785.15	293	3186	S1502	-7124.65	173	3221	S1528	-7464.15	53
3152	RX[186]	-6794.85	413	3187	S1503	-7134.35	293	3222	S1529	-7473.85	173
3153	S1477	-6804.55	53	3188	RX[177]	-7144.05	413	3223	S1530	-7483.55	293
3154	S1478	-6814.25	173	3189	S1504	-7153.75	53	3224	RX[168]	-7493.25	413
3155	S1479	-6823.95	293	3190	S1505	-7163.45	173	3225	S1531	-7502.95	53
3156	RX[185]	-6833.65	413	3191	S1506	-7173.15	293	3226	S1532	-7512.65	173
3157	S1480	-6843.35	53	3192	RX[176]	-7182.85	413	3227	S1533	-7522.35	293
3158	S1481	-6853.05	173	3193	S1507	-7192.55	53	3228	RX[167]	-7532.05	413
3159	S1482	-6862.75	293	3194	S1508	-7202.25	173	3229	S1534	-7541.75	53
3160	RX[184]	-6872.45	413	3195	S1509	-7211.95	293	3230	S1535	-7551.45	173
3161	S1483	-6882.15	53	3196	RX[175]	-7221.65	413	3231	S1536	-7561.15	293
3162	S1484	-6891.85	173	3197	S1510	-7231.35	53	3232	RX[166]	-7570.85	413
3163	S1485	-6901.55	293	3198	S1511	-7241.05	173	3233	S1537	-7580.55	53
3164	RX[183]	-6911.25	413	3199	S1512	-7250.75	293	3234	S1538	-7590.25	173
3165	S1486	-6920.95	53	3200	RX[174]	-7260.45	413	3235	S1539	-7599.95	293
3166	S1487	-6930.65	173	3201	S1513	-7270.15	53	3236	RX[165]	-7609.65	413
3167	S1488	-6940.35	293	3202	S1514	-7279.85	173	3237	S1540	-7619.35	53
3168	RX[182]	-6950.05	413	3203	S1515	-7289.55	293	3238	S1541	-7629.05	173
3169	S1489	-6959.75	53	3204	RX[173]	-7299.25	413	3239	S1542	-7638.75	293
3170	S1490	-6969.45	173	3205	S1516	-7308.95	53	3240	RX[164]	-7648.45	413
3171	S1491	-6979.15	293	3206	S1517	-7318.65	173	3241	S1543	-7658.15	53
3172	RX[181]	-6988.85	413	3207	S1518	-7328.35	293	3242	S1544	-7667.85	173
3173	S1492	-6998.55	53	3208	RX[172]	-7338.05	413	3243	S1545	-7677.55	293
3174	S1493	-7008.25	173	3209	S1519	-7347.75	53	3244	RX[163]	-7687.25	413
3175	S1494	-7017.95	293	3210	S1520	-7357.45	173	3245	S1546	-7696.95	53
3176	RX[180]	-7027.65	413	3211	S1521	-7367.15	293	3246	S1547	-7706.65	173
3177	S1495	-7037.35	53	3212	RX[171]	-7376.85	413	3247	S1548	-7716.35	293
3178	S1496	-7047.05	173	3213	S1522	-7386.55	53	3248	RX[162]	-7726.05	413
3179	S1497	-7056.75	293	3214	S1523	-7396.25	173	3249	S1549	-7735.75	53

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3250	S1550	-7745.45	173	3285	S1576	-8084.95	53	3320	RX[151]	-8424.45	413
3251	S1551	-7755.15	293	3286	S1577	-8094.65	173	3321	S1603	-8434.15	53
3252	RX[161]	-7764.85	413	3287	S1578	-8104.35	293	3322	S1604	-8443.85	173
3253	S1552	-7774.55	53	3288	RX[159]	-8114.05	413	3323	S1605	-8453.55	293
3254	S1553	-7784.25	173	3289	S1579	-8123.75	53	3324	RX[150]	-8463.25	413
3255	S1554	-7793.95	293	3290	S1580	-8133.45	173	3325	S1606	-8472.95	53
3256	GRID6	-7803.65	413	3291	S1581	-8143.15	293	3326	S1607	-8482.65	173
3257	S1555	-7813.35	53	3292	RX[158]	-8152.85	413	3327	S1608	-8492.35	293
3258	S1556	-7823.05	173	3293	S1582	-8162.55	53	3328	RX[149]	-8502.05	413
3259	S1557	-7832.75	293	3294	S1583	-8172.25	173	3329	S1609	-8511.75	53
3260	GRID6	-7842.45	413	3295	S1584	-8181.95	293	3330	S1610	-8521.45	173
3261	S1558	-7852.15	53	3296	RX[157]	-8191.65	413	3331	S1611	-8531.15	293
3262	S1559	-7861.85	173	3297	S1585	-8201.35	53	3332	RX[148]	-8540.85	413
3263	S1560	-7871.55	293	3298	S1586	-8211.05	173	3333	S1612	-8550.55	53
3264	GRID6	-7881.25	413	3299	S1587	-8220.75	293	3334	S1613	-8560.25	173
3265	S1561	-7890.95	53	3300	RX[156]	-8230.45	413	3335	S1614	-8569.95	293
3266	S1562	-7900.65	173	3301	S1588	-8240.15	53	3336	RX[147]	-8579.65	413
3267	S1563	-7910.35	293	3302	S1589	-8249.85	173	3337	S1615	-8589.35	53
3268	GRID6	-7920.05	413	3303	S1590	-8259.55	293	3338	S1616	-8599.05	173
3269	S1564	-7929.75	53	3304	RX[155]	-8269.25	413	3339	S1617	-8608.75	293
3270	S1565	-7939.45	173	3305	S1591	-8278.95	53	3340	RX[146]	-8618.45	413
3271	S1566	-7949.15	293	3306	S1592	-8288.65	173	3341	S1618	-8628.15	53
3272	GRID6	-7958.85	413	3307	S1593	-8298.35	293	3342	S1619	-8637.85	173
3273	S1567	-7968.55	53	3308	RX[154]	-8308.05	413	3343	S1620	-8647.55	293
3274	S1568	-7978.25	173	3309	S1594	-8317.75	53	3344	RX[145]	-8657.25	413
3275	S1569	-7987.95	293	3310	S1595	-8327.45	173	3345	S1621	-8666.95	53
3276	GRID6	-7997.65	413	3311	S1596	-8337.15	293	3346	S1622	-8676.65	173
3277	S1570	-8007.35	53	3312	RX[153]	-8346.85	413	3347	S1623	-8686.35	293
3278	S1571	-8017.05	173	3313	S1597	-8356.55	53	3348	RX[144]	-8696.05	413
3279	S1572	-8026.75	293	3314	S1598	-8366.25	173	3349	S1624	-8705.75	53
3280	GRID6	-8036.45	413	3315	S1599	-8375.95	293	3350	S1625	-8715.45	173
3281	S1573	-8046.15	53	3316	RX[152]	-8385.65	413	3351	S1626	-8725.15	293
3282	S1574	-8055.85	173	3317	S1600	-8395.35	53	3352	RX[143]	-8734.85	413
3283	S1575	-8065.55	293	3318	S1601	-8405.05	173	3353	S1627	-8744.55	53
3284	RX[160]	-8075.25	413	3319	S1602	-8414.75	293	3354	S1628	-8754.25	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3355	S1629	-8763.95	293	3390	S1655	-9103.45	173	3425	S1681	-9442.95	53
3356	RX[142]	-8773.65	413	3391	S1656	-9113.15	293	3426	S1682	-9452.65	173
3357	S1630	-8783.35	53	3392	RX[133]	-9122.85	413	3427	S1683	-9462.35	293
3358	S1631	-8793.05	173	3393	S1657	-9132.55	53	3428	GRID5	-9472.05	413
3359	S1632	-8802.75	293	3394	S1658	-9142.25	173	3429	S1684	-9481.75	53
3360	RX[141]	-8812.45	413	3395	S1659	-9151.95	293	3430	S1685	-9491.45	173
3361	S1633	-8822.15	53	3396	RX[132]	-9161.65	413	3431	S1686	-9501.15	293
3362	S1634	-8831.85	173	3397	S1660	-9171.35	53	3432	GRID5	-9510.85	413
3363	S1635	-8841.55	293	3398	S1661	-9181.05	173	3433	S1687	-9520.55	53
3364	RX[140]	-8851.25	413	3399	S1662	-9190.75	293	3434	S1688	-9530.25	173
3365	S1636	-8860.95	53	3400	RX[131]	-9200.45	413	3435	S1689	-9539.95	293
3366	S1637	-8870.65	173	3401	S1663	-9210.15	53	3436	GRID5	-9549.65	413
3367	S1638	-8880.35	293	3402	S1664	-9219.85	173	3437	S1690	-9559.35	53
3368	RX[139]	-8890.05	413	3403	S1665	-9229.55	293	3438	S1691	-9569.05	173
3369	S1639	-8899.75	53	3404	RX[130]	-9239.25	413	3439	S1692	-9578.75	293
3370	S1640	-8909.45	173	3405	S1666	-9248.95	53	3440	RX[128]	-9588.45	413
3371	S1641	-8919.15	293	3406	S1667	-9258.65	173	3441	S1693	-9598.15	53
3372	RX[138]	-8928.85	413	3407	S1668	-9268.35	293	3442	S1694	-9607.85	173
3373	S1642	-8938.55	53	3408	RX[129]	-9278.05	413	3443	S1695	-9617.55	293
3374	S1643	-8948.25	173	3409	S1669	-9287.75	53	3444	RX[127]	-9627.25	413
3375	S1644	-8957.95	293	3410	S1670	-9297.45	173	3445	S1696	-9636.95	53
3376	RX[137]	-8967.65	413	3411	S1671	-9307.15	293	3446	S1697	-9646.65	173
3377	S1645	-8977.35	53	3412	GRID5	-9316.85	413	3447	S1698	-9656.35	293
3378	S1646	-8987.05	173	3413	S1672	-9326.55	53	3448	RX[126]	-9666.05	413
3379	S1647	-8996.75	293	3414	S1673	-9336.25	173	3449	S1699	-9675.75	53
3380	RX[136]	-9006.45	413	3415	S1674	-9345.95	293	3450	S1700	-9685.45	173
3381	S1648	-9016.15	53	3416	GRID5	-9355.65	413	3451	S1701	-9695.15	293
3382	S1649	-9025.85	173	3417	S1675	-9365.35	53	3452	RX[125]	-9704.85	413
3383	S1650	-9035.55	293	3418	S1676	-9375.05	173	3453	S1702	-9714.55	53
3384	RX[135]	-9045.25	413	3419	S1677	-9384.75	293	3454	S1703	-9724.25	173
3385	S1651	-9054.95	53	3420	GRID5	-9394.45	413	3455	S1704	-9733.95	293
3386	S1652	-9064.65	173	3421	S1678	-9404.15	53	3456	RX[124]	-9743.65	413
3387	S1653	-9074.35	293	3422	S1679	-9413.85	173	3457	S1705	-9753.35	53
3388	RX[134]	-9084.05	413	3423	S1680	-9423.55	293	3458	S1706	-9763.05	173
3389	S1654	-9093.75	53	3424	GRID5	-9433.25	413	3459	S1707	-9772.75	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3460	RX[123]	-9782.45	413	3495	S1734	-10121.95	293	3530	S1760	-10461.45	173
3461	S1708	-9792.15	53	3496	RX[114]	-10131.65	413	3531	S1761	-10471.15	293
3462	S1709	-9801.85	173	3497	S1735	-10141.35	53	3532	RX[105]	-10480.85	413
3463	S1710	-9811.55	293	3498	S1736	-10151.05	173	3533	S1762	-10490.55	53
3464	RX[122]	-9821.25	413	3499	S1737	-10160.75	293	3534	S1763	-10500.25	173
3465	S1711	-9830.95	53	3500	RX[113]	-10170.45	413	3535	S1764	-10509.95	293
3466	S1712	-9840.65	173	3501	S1738	-10180.15	53	3536	RX[104]	-10519.65	413
3467	S1713	-9850.35	293	3502	S1739	-10189.85	173	3537	S1765	-10529.35	53
3468	RX[121]	-9860.05	413	3503	S1740	-10199.55	293	3538	S1766	-10539.05	173
3469	S1714	-9869.75	53	3504	RX[112]	-10209.25	413	3539	S1767	-10548.75	293
3470	S1715	-9879.45	173	3505	S1741	-10218.95	53	3540	RX[103]	-10558.45	413
3471	S1716	-9889.15	293	3506	S1742	-10228.65	173	3541	S1768	-10568.15	53
3472	RX[120]	-9898.85	413	3507	S1743	-10238.35	293	3542	S1769	-10577.85	173
3473	S1717	-9908.55	53	3508	RX[111]	-10248.05	413	3543	S1770	-10587.55	293
3474	S1718	-9918.25	173	3509	S1744	-10257.75	53	3544	RX[102]	-10597.25	413
3475	S1719	-9927.95	293	3510	S1745	-10267.45	173	3545	S1771	-10606.95	53
3476	RX[119]	-9937.65	413	3511	S1746	-10277.15	293	3546	S1772	-10616.65	173
3477	S1720	-9947.35	53	3512	RX[110]	-10286.85	413	3547	S1773	-10626.35	293
3478	S1721	-9957.05	173	3513	S1747	-10296.55	53	3548	RX[101]	-10636.05	413
3479	S1722	-9966.75	293	3514	S1748	-10306.25	173	3549	S1774	-10645.75	53
3480	RX[118]	-9976.45	413	3515	S1749	-10315.95	293	3550	S1775	-10655.45	173
3481	S1723	-9986.15	53	3516	RX[109]	-10325.65	413	3551	S1776	-10665.15	293
3482	S1724	-9995.85	173	3517	S1750	-10335.35	53	3552	RX[100]	-10674.85	413
3483	S1725	-10005.55	293	3518	S1751	-10345.05	173	3553	S1777	-10684.55	53
3484	RX[117]	-10015.25	413	3519	S1752	-10354.75	293	3554	S1778	-10694.25	173
3485	S1726	-10024.95	53	3520	RX[108]	-10364.45	413	3555	S1779	-10703.95	293
3486	S1727	-10034.65	173	3521	S1753	-10374.15	53	3556	RX[99]	-10713.65	413
3487	S1728	-10044.35	293	3522	S1754	-10383.85	173	3557	S1780	-10723.35	53
3488	RX[116]	-10054.05	413	3523	S1755	-10393.55	293	3558	S1781	-10733.05	173
3489	S1729	-10063.75	53	3524	RX[107]	-10403.25	413	3559	S1782	-10742.75	293
3490	S1730	-10073.45	173	3525	S1756	-10412.95	53	3560	RX[98]	-10752.45	413
3491	S1731	-10083.15	293	3526	S1757	-10422.65	173	3561	S1783	-10762.15	53
3492	RX[115]	-10092.85	413	3527	S1758	-10432.35	293	3562	S1784	-10771.85	173
3493	S1732	-10102.55	53	3528	RX[106]	-10442.05	413	3563	S1785	-10781.55	293
3494	S1733	-10112.25	173	3529	S1759	-10451.75	53	3564	RX[97]	-10791.25	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3565	S1786	-10800.95	53	3600	GRID4	-11140.45	413	3635	S1839	-11479.95	293
3566	S1787	-10810.65	173	3601	S1813	-11150.15	53	3636	RX[89]	-11489.65	413
3567	S1788	-10820.35	293	3602	S1814	-11159.85	173	3637	S1840	-11499.35	53
3568	GRID4	-10830.05	413	3603	S1815	-11169.55	293	3638	S1841	-11509.05	173
3569	S1789	-10839.75	53	3604	GRID4	-11179.25	413	3639	S1842	-11518.75	293
3570	S1790	-10849.45	173	3605	S1816	-11188.95	53	3640	RX[88]	-11528.45	413
3571	S1791	-10859.15	293	3606	S1817	-11198.65	173	3641	S1843	-11538.15	53
3572	GRID4	-10868.85	413	3607	S1818	-11208.35	293	3642	S1844	-11547.85	173
3573	S1792	-10878.55	53	3608	RX[96]	-11218.05	413	3643	S1845	-11557.55	293
3574	S1793	-10888.25	173	3609	S1819	-11227.75	53	3644	RX[87]	-11567.25	413
3575	S1794	-10897.95	293	3610	S1820	-11237.45	173	3645	S1846	-11576.95	53
3576	GRID4	-10907.65	413	3611	S1821	-11247.15	293	3646	S1847	-11586.65	173
3577	S1795	-10917.35	53	3612	RX[95]	-11256.85	413	3647	S1848	-11596.35	293
3578	S1796	-10927.05	173	3613	S1822	-11266.55	53	3648	RX[86]	-11606.05	413
3579	S1797	-10936.75	293	3614	S1823	-11276.25	173	3649	S1849	-11615.75	53
3580	GRID4	-10946.45	413	3615	S1824	-11285.95	293	3650	S1850	-11625.45	173
3581	S1798	-10956.15	53	3616	RX[94]	-11295.65	413	3651	S1851	-11635.15	293
3582	S1799	-10965.85	173	3617	S1825	-11305.35	53	3652	RX[85]	-11644.85	413
3583	S1800	-10975.55	293	3618	S1826	-11315.05	173	3653	S1852	-11654.55	53
3584	GRID4	-10985.25	413	3619	S1827	-11324.75	293	3654	S1853	-11664.25	173
3585	S1801	-10994.95	53	3620	RX[93]	-11334.45	413	3655	S1854	-11673.95	293
3586	S1802	-11004.65	173	3621	S1828	-11344.15	53	3656	RX[84]	-11683.65	413
3587	S1803	-11014.35	293	3622	S1829	-11353.85	173	3657	S1855	-11693.35	53
3588	GRID4	-11024.05	413	3623	S1830	-11363.55	293	3658	S1856	-11703.05	173
3589	S1804	-11033.75	53	3624	RX[92]	-11373.25	413	3659	S1857	-11712.75	293
3590	S1805	-11043.45	173	3625	S1831	-11382.95	53	3660	RX[83]	-11722.45	413
3591	S1806	-11053.15	293	3626	S1832	-11392.65	173	3661	S1858	-11732.15	53
3592	GRID4	-11062.85	413	3627	S1833	-11402.35	293	3662	S1859	-11741.85	173
3593	S1807	-11072.55	53	3628	RX[91]	-11412.05	413	3663	S1860	-11751.55	293
3594	S1808	-11082.25	173	3629	S1834	-11421.75	53	3664	RX[82]	-11761.25	413
3595	S1809	-11091.95	293	3630	S1835	-11431.45	173	3665	S1861	-11770.95	53
3596	GRID4	-11101.65	413	3631	S1836	-11441.15	293	3666	S1862	-11780.65	173
3597	S1810	-11111.35	53	3632	RX[90]	-11450.85	413	3667	S1863	-11790.35	293
3598	S1811	-11121.05	173	3633	S1837	-11460.55	53	3668	RX[81]	-11800.05	413
3599	S1812	-11130.75	293	3634	S1838	-11470.25	173	3669	S1864	-11809.75	53

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3670	S1865	-11819.45	173	3705	S1891	-12158.95	53	3740	GRID3	-12498.45	413
3671	S1866	-11829.15	293	3706	S1892	-12168.65	173	3741	S1918	-12508.15	53
3672	RX[80]	-11838.85	413	3707	S1893	-12178.35	293	3742	S1919	-12517.85	173
3673	S1867	-11848.55	53	3708	RX[71]	-12188.05	413	3743	S1920	-12527.55	293
3674	S1868	-11858.25	173	3709	S1894	-12197.75	53	3744	GRID3	-12537.25	413
3675	S1869	-11867.95	293	3710	S1895	-12207.45	173	3745	S1921	-12546.95	53
3676	RX[79]	-11877.65	413	3711	S1896	-12217.15	293	3746	S1922	-12556.65	173
3677	S1870	-11887.35	53	3712	RX[70]	-12226.85	413	3747	S1923	-12566.35	293
3678	S1871	-11897.05	173	3713	S1897	-12236.55	53	3748	GRID3	-12576.05	413
3679	S1872	-11906.75	293	3714	S1898	-12246.25	173	3749	S1924	-12585.75	53
3680	RX[78]	-11916.45	413	3715	S1899	-12255.95	293	3750	S1925	-12595.45	173
3681	S1873	-11926.15	53	3716	RX[69]	-12265.65	413	3751	S1926	-12605.15	293
3682	S1874	-11935.85	173	3717	S1900	-12275.35	53	3752	GRID3	-12614.85	413
3683	S1875	-11945.55	293	3718	S1901	-12285.05	173	3753	S1927	-12624.55	53
3684	RX[77]	-11955.25	413	3719	S1902	-12294.75	293	3754	S1928	-12634.25	173
3685	S1876	-11964.95	53	3720	RX[68]	-12304.45	413	3755	S1929	-12643.95	293
3686	S1877	-11974.65	173	3721	S1903	-12314.15	53	3756	GRID3	-12653.65	413
3687	S1878	-11984.35	293	3722	S1904	-12323.85	173	3757	S1930	-12663.35	53
3688	RX[76]	-11994.05	413	3723	S1905	-12333.55	293	3758	S1931	-12673.05	173
3689	S1879	-12003.75	53	3724	RX[67]	-12343.25	413	3759	S1932	-12682.75	293
3690	S1880	-12013.45	173	3725	S1906	-12352.95	53	3760	GRID3	-12692.45	413
3691	S1881	-12023.15	293	3726	S1907	-12362.65	173	3761	S1933	-12702.15	53
3692	RX[75]	-12032.85	413	3727	S1908	-12372.35	293	3762	S1934	-12711.85	173
3693	S1882	-12042.55	53	3728	RX[66]	-12382.05	413	3763	S1935	-12721.55	293
3694	S1883	-12052.25	173	3729	S1909	-12391.75	53	3764	RX[64]	-12731.25	413
3695	S1884	-12061.95	293	3730	S1910	-12401.45	173	3765	S1936	-12740.95	53
3696	RX[74]	-12071.65	413	3731	S1911	-12411.15	293	3766	S1937	-12750.65	173
3697	S1885	-12081.35	53	3732	RX[65]	-12420.85	413	3767	S1938	-12760.35	293
3698	S1886	-12091.05	173	3733	S1912	-12430.55	53	3768	RX[63]	-12770.05	413
3699	S1887	-12100.75	293	3734	S1913	-12440.25	173	3769	S1939	-12779.75	53
3700	RX[73]	-12110.45	413	3735	S1914	-12449.95	293	3770	S1940	-12789.45	173
3701	S1888	-12120.15	53	3736	GRID3	-12459.65	413	3771	S1941	-12799.15	293
3702	S1889	-12129.85	173	3737	S1915	-12469.35	53	3772	RX[62]	-12808.85	413
3703	S1890	-12139.55	293	3738	S1916	-12479.05	173	3773	S1942	-12818.55	53
3704	RX[72]	-12149.25	413	3739	S1917	-12488.75	293	3774	S1943	-12828.25	173

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3775	S1944	-12837.95	293	3810	S1970	-13177.45	173	3845	S1996	-13516.95	53
3776	RX[61]	-12847.65	413	3811	S1971	-13187.15	293	3846	S1997	-13526.65	173
3777	S1945	-12857.35	53	3812	RX[52]	-13196.85	413	3847	S1998	-13536.35	293
3778	S1946	-12867.05	173	3813	S1972	-13206.55	53	3848	RX[43]	-13546.05	413
3779	S1947	-12876.75	293	3814	S1973	-13216.25	173	3849	S1999	-13555.75	53
3780	RX[60]	-12886.45	413	3815	S1974	-13225.95	293	3850	S2000	-13565.45	173
3781	S1948	-12896.15	53	3816	RX[51]	-13235.65	413	3851	S2001	-13575.15	293
3782	S1949	-12905.85	173	3817	S1975	-13245.35	53	3852	RX[42]	-13584.85	413
3783	S1950	-12915.55	293	3818	S1976	-13255.05	173	3853	S2002	-13594.55	53
3784	RX[59]	-12925.25	413	3819	S1977	-13264.75	293	3854	S2003	-13604.25	173
3785	S1951	-12934.95	53	3820	RX[50]	-13274.45	413	3855	S2004	-13613.95	293
3786	S1952	-12944.65	173	3821	S1978	-13284.15	53	3856	RX[41]	-13623.65	413
3787	S1953	-12954.35	293	3822	S1979	-13293.85	173	3857	S2005	-13633.35	53
3788	RX[58]	-12964.05	413	3823	S1980	-13303.55	293	3858	S2006	-13643.05	173
3789	S1954	-12973.75	53	3824	RX[49]	-13313.25	413	3859	S2007	-13652.75	293
3790	S1955	-12983.45	173	3825	S1981	-13322.95	53	3860	RX[40]	-13662.45	413
3791	S1956	-12993.15	293	3826	S1982	-13332.65	173	3861	S2008	-13672.15	53
3792	RX[57]	-13002.85	413	3827	S1983	-13342.35	293	3862	S2009	-13681.85	173
3793	S1957	-13012.55	53	3828	RX[48]	-13352.05	413	3863	S2010	-13691.55	293
3794	S1958	-13022.25	173	3829	S1984	-13361.75	53	3864	RX[39]	-13701.25	413
3795	S1959	-13031.95	293	3830	S1985	-13371.45	173	3865	S2011	-13710.95	53
3796	RX[56]	-13041.65	413	3831	S1986	-13381.15	293	3866	S2012	-13720.65	173
3797	S1960	-13051.35	53	3832	RX[47]	-13390.85	413	3867	S2013	-13730.35	293
3798	S1961	-13061.05	173	3833	S1987	-13400.55	53	3868	RX[38]	-13740.05	413
3799	S1962	-13070.75	293	3834	S1988	-13410.25	173	3869	S2014	-13749.75	53
3800	RX[55]	-13080.45	413	3835	S1989	-13419.95	293	3870	S2015	-13759.45	173
3801	S1963	-13090.15	53	3836	RX[46]	-13429.65	413	3871	S2016	-13769.15	293
3802	S1964	-13099.85	173	3837	S1990	-13439.35	53	3872	RX[37]	-13778.85	413
3803	S1965	-13109.55	293	3838	S1991	-13449.05	173	3873	S2017	-13788.55	53
3804	RX[54]	-13119.25	413	3839	S1992	-13458.75	293	3874	S2018	-13798.25	173
3805	S1966	-13128.95	53	3840	RX[45]	-13468.45	413	3875	S2019	-13807.95	293
3806	S1967	-13138.65	173	3841	S1993	-13478.15	53	3876	RX[36]	-13817.65	413
3807	S1968	-13148.35	293	3842	S1994	-13487.85	173	3877	S2020	-13827.35	53
3808	RX[53]	-13158.05	413	3843	S1995	-13497.55	293	3878	S2021	-13837.05	173
3809	S1969	-13167.75	53	3844	RX[44]	-13507.25	413	3879	S2022	-13846.75	293

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3880	RX[35]	-13856.45	413	3915	S2049	-14195.95	293	3950	S2075	-14535.45	173
3881	S2023	-13866.15	53	3916	GRID2	-14205.65	413	3951	S2076	-14545.15	293
3882	S2024	-13875.85	173	3917	S2050	-14215.35	53	3952	RX[24]	-14554.85	413
3883	S2025	-13885.55	293	3918	S2051	-14225.05	173	3953	S2077	-14564.55	53
3884	RX[34]	-13895.25	413	3919	S2052	-14234.75	293	3954	S2078	-14574.25	173
3885	S2026	-13904.95	53	3920	RX[32]	-14244.45	413	3955	S2079	-14583.95	293
3886	S2027	-13914.65	173	3921	S2053	-14254.15	53	3956	RX[23]	-14593.65	413
3887	S2028	-13924.35	293	3922	S2054	-14263.85	173	3957	S2080	-14603.35	53
3888	RX[33]	-13934.05	413	3923	S2055	-14273.55	293	3958	S2081	-14613.05	173
3889	S2029	-13943.75	53	3924	RX[31]	-14283.25	413	3959	S2082	-14622.75	293
3890	S2030	-13953.45	173	3925	S2056	-14292.95	53	3960	RX[22]	-14632.45	413
3891	S2031	-13963.15	293	3926	S2057	-14302.65	173	3961	S2083	-14642.15	53
3892	GRID2	-13972.85	413	3927	S2058	-14312.35	293	3962	S2084	-14651.85	173
3893	S2032	-13982.55	53	3928	RX[30]	-14322.05	413	3963	S2085	-14661.55	293
3894	S2033	-13992.25	173	3929	S2059	-14331.75	53	3964	RX[21]	-14671.25	413
3895	S2034	-14001.95	293	3930	S2060	-14341.45	173	3965	S2086	-14680.95	53
3896	GRID2	-14011.65	413	3931	S2061	-14351.15	293	3966	S2087	-14690.65	173
3897	S2035	-14021.35	53	3932	RX[29]	-14360.85	413	3967	S2088	-14700.35	293
3898	S2036	-14031.05	173	3933	S2062	-14370.55	53	3968	RX[20]	-14710.05	413
3899	S2037	-14040.75	293	3934	S2063	-14380.25	173	3969	S2089	-14719.75	53
3900	GRID2	-14050.45	413	3935	S2064	-14389.95	293	3970	S2090	-14729.45	173
3901	S2038	-14060.15	53	3936	RX[28]	-14399.65	413	3971	S2091	-14739.15	293
3902	S2039	-14069.85	173	3937	S2065	-14409.35	53	3972	RX[19]	-14748.85	413
3903	S2040	-14079.55	293	3938	S2066	-14419.05	173	3973	S2092	-14758.55	53
3904	GRID2	-14089.25	413	3939	S2067	-14428.75	293	3974	S2093	-14768.25	173
3905	S2041	-14098.95	53	3940	RX[27]	-14438.45	413	3975	S2094	-14777.95	293
3906	S2042	-14108.65	173	3941	S2068	-14448.15	53	3976	RX[18]	-14787.65	413
3907	S2043	-14118.35	293	3942	S2069	-14457.85	173	3977	S2095	-14797.35	53
3908	GRID2	-14128.05	413	3943	S2070	-14467.55	293	3978	S2096	-14807.05	173
3909	S2044	-14137.75	53	3944	RX[26]	-14477.25	413	3979	S2097	-14816.75	293
3910	S2045	-14147.45	173	3945	S2071	-14486.95	53	3980	RX[17]	-14826.45	413
3911	S2046	-14157.15	293	3946	S2072	-14496.65	173	3981	S2098	-14836.15	53
3912	GRID2	-14166.85	413	3947	S2073	-14506.35	293	3982	S2099	-14845.85	173
3913	S2047	-14176.55	53	3948	RX[25]	-14516.05	413	3983	S2100	-14855.55	293
3914	S2048	-14186.25	173	3949	S2074	-14525.75	53	3984	RX[16]	-14865.25	413

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
3985	S2101	-14874.95	53	4020	RX[7]	-15214.45	413	4055	S2154	-15553.95	293
3986	S2102	-14884.65	173	4021	S2128	-15224.15	53	4056	GRID1	-15563.65	413
3987	S2103	-14894.35	293	4022	S2129	-15233.85	173	4057	S2155	-15573.35	53
3988	RX[15]	-14904.05	413	4023	S2130	-15243.55	293	4058	S2156	-15583.05	173
3989	S2104	-14913.75	53	4024	RX[6]	-15253.25	413	4059	S2157	-15592.75	293
3990	S2105	-14923.45	173	4025	S2131	-15262.95	53	4060	GRID1	-15602.45	413
3991	S2106	-14933.15	293	4026	S2132	-15272.65	173	4061	S2158	-15612.15	53
3992	RX[14]	-14942.85	413	4027	S2133	-15282.35	293	4062	S2159	-15621.85	173
3993	S2107	-14952.55	53	4028	RX[5]	-15292.05	413	4063	S2160	-15631.55	293
3994	S2108	-14962.25	173	4029	S2134	-15301.75	53	4064	GRID1	-15641.25	413
3995	S2109	-14971.95	293	4030	S2135	-15311.45	173	4065	SDUM2	-15650.95	53
3996	RX[13]	-14981.65	413	4031	S2136	-15321.15	293	4066	SDUM3	-15660.65	173
3997	S2110	-14991.35	53	4032	RX[4]	-15330.85	413	4067	DUMMY	-15670.35	293
3998	S2111	-15001.05	173	4033	S2137	-15340.55	53	4068	GRID1	-15680.05	413
3999	S2112	-15010.75	293	4034	S2138	-15350.25	173	4069	DUMMY	-15689.75	53
4000	RX[12]	-15020.45	413	4035	S2139	-15359.95	293	4070	DUMMY	-15699.45	173
4001	S2113	-15030.15	53	4036	RX[3]	-15369.65	413	4071	DUMMY	-15709.15	293
4002	S2114	-15039.85	173	4037	S2140	-15379.35	53	4072	DUMMY	-15718.85	413
4003	S2115	-15049.55	293	4038	S2141	-15389.05	173	4073	VCOM_PASS_L	-15728.55	53
4004	RX[11]	-15059.25	413	4039	S2142	-15398.75	293	4074	VCOM_PASS_L	-15738.25	173
4005	S2116	-15068.95	53	4040	RX[2]	-15408.45	413	4075	VCOM_PASS_L	-15747.95	293
4006	S2117	-15078.65	173	4041	S2143	-15418.15	53	4076	DUMMY	-15757.65	413
4007	S2118	-15088.35	293	4042	S2144	-15427.85	173	4077	VCOM_PASS_L	-15767.35	53
4008	RX[10]	-15098.05	413	4043	S2145	-15437.55	293	4078	VCOM_PASS_L	-15777.05	173
4009	S2119	-15107.75	53	4044	RX[1]	-15447.25	413	4079	VCOM_PASS_L	-15786.75	293
4010	S2120	-15117.45	173	4045	S2146	-15456.95	53	4080	DUMMY	-15796.45	413
4011	S2121	-15127.15	293	4046	S2147	-15466.65	173	4081	DUMMY	-15806.15	53
4012	RX[9]	-15136.85	413	4047	S2148	-15476.35	293	4082	DUMMY	-15815.85	173
4013	S2122	-15146.55	53	4048	GRID1	-15486.05	413	4083	DUMMY	-15825.55	293
4014	S2123	-15156.25	173	4049	S2149	-15495.75	53	4084	DUMMY	-15835.25	413
4015	S2124	-15165.95	293	4050	S2150	-15505.45	173	4085	DUMMY	-15844.95	53
4016	RX[8]	-15175.65	413	4051	S2151	-15515.15	293	4086	DUMMY	-15854.65	173
4017	S2125	-15185.35	53	4052	GRID1	-15524.85	413	4087	DUMMY	-15864.35	293
4018	S2126	-15195.05	173	4053	S2152	-15534.55	53	4088	DUMMY	-15874.05	413
4019	S2127	-15204.75	293	4054	S2153	-15544.25	173	4089	DUMMY	-15883.75	53

No.	Name	X	Y		No.	Name	X	Y
4090	DUMMY	-15893.45	173		A1	A1	-15969.40	440.5
4091	DUMMY	-15903.15	293		A2	A2	15969.40	440.5

4.2 Pin Definition

4.2.1 Voltage Pins

Name	I/O	PAD Type (Voltage Level)	Description
IOVCC	I	Power Supply	External power supply for internal logic circuit
AVDD	I	Power Supply	External positive power supply for analog circuit
AVEE	I	Power Supply	External negative power supply for analog circuit
AGND	-	GND	Analog ground, need to connect to GND from FPC
DGND	-	GND	Digital ground, need to connect to GND from FPC
DPHYGND	-	GND	Ground for MIPI DPHY circuit, need to connect to GND from FPC
VDD	O	Analog	Regulator output for logic, all pins need to connect together from FPC
VDDD	O	Analog	Internal logic power for Touch logic, all pins need to connect together from FPC
VDDM	O	Analog	Regulator output for MIPI DSI
DPHYVCC	I	Analog	External power supply for MIPI PHY circuit
TVH	O	Analog	Touch output high voltage level, all pins need to connect together from FPC.
TVL	O	Analog	Touch output low voltage level, all pins need to connect together from FPC.
VAG	O	Analog	Active guard signal, all pins need to connect together from FPC.
VGH	O	Analog	Step-up output voltage for panel, all pins need to connect together from FPC.
VGHO1	O	Analog	Step-up output voltage, all pins need to connect together from FPC.
VGL	O	Analog	Step-up output voltage for panel, all pins need to connect together from FPC.
GVDDP	O	Analog	Positive LDO output for gamma circuit. If not used, please keep it open.
GVDDN	O	Analog	Negative LDO output for gamma circuit. If not used, please keep it open.

4.2.2 Control Pins

Name	I/O	PAD Type (Voltage Level)	Description
RESX	I	Digital(IOVCC)	Global reset signal. Low active.
IM[1:0]	I	Digital(IOVCC)	Interface mode select pins | IM1	IM0	Interface Selection
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0	0	DSI video mode
0	1	Reserved
1	0	Reserved
1	1	Reserved	
TE	O	Digital(IOVCC)	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is GND level.
TE1	O	Digital(IOVCC)	This signal is used for noise sensing of TP and generated per scan line.
LEDPWM	O	Digital(IOVCC)	LCD backlight control PWM output pin
FRM	I	--	Test pin, please connect to ground.
PSWAP	I	Digital(IOVCC)	MIPI Lane polarity swap pin.
DSWAP[1:0]	I	Digital(IOVCC)	MIPI data lane swap and polarity swap table.

MIPI data lane swap and polarity swap table.

PSWAP	DSWAP[1:0]	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
0	00	D3N	D3P	D2N	D2P	CLKN	CLKP	D1N	D1P	D0N	D0P
	01	D3N	D3P	D0N	D0P	CLKN	CLKP	D1N	D1P	D2N	D2P
	10	D0N	D0P	D1N	D1P	CLKN	CLKP	D2N	D2P	D3N	D3P
	11	D2N	D2P	D1N	D1P	CLKN	CLKP	D0N	D0P	D3N	D3P
1	00	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
	01	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
	10	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
	11	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N

4.2.3 MIPI Interface Pins

Name	I/O	PAD Type (Voltage Level)	Description
CLKP	I	MIPI	MIPI-DSI clock lane positive-end input pin
CLKN	I	MIPI	MIPI-DSI clock lane negative-end input pin
DATA0P	I/O	MIPI	MIPI-DSI data lane 0 positive-end input/output pin * Please connected to GND if not used
DATA0N	I/O	MIPI	MIPI-DSI data lane 0 negative-end input/output pin * Please connected to GND if not used
DATA1P	I	MIPI	MIPI-DSI data lane 1 positive-end input pin * Please connected to GND if not used
DATA1N	I	MIPI	MIPI-DSI data lane 1 negative-end input pin * Please connected to GND if not used.
DATA 2P	I	MIPI	MIPI-DSI data lane 2 positive-end input pin * Please connected to GND if not used
DATA 2N	I	MIPI	MIPI-DSI data lane 2 negative-end input pin * Please connected to GND if not used
DATA 3P	I	MIPI	MIPI-DSI data lane 3 positive-end input pin * Please connected to GND if not used
DATA 3N	I	MIPI	MIPI-DSI data lane 3 negative-end input pin * Please connected to GND if not used

4.2.4 Driver Panel Related Pins

Name	I/O	PAD Type (Voltage Level)	Description
CGOUTL[22:1]	O	Analog	Panel control signal output pads for left side GIP.
CGOUTR[22:1]	O	Analog	Panel control signal output pads for right side GIP.
S1:S2160	O	Analog	Output source driver signals. The D/A converted 256-gray-scale analog voltage is output.
VCOM	O	Analog	VCOM voltage output
COGTEST12 COGTEST34	O	No level	For ITO resistance trace
VCOM_PASS_R VCOM_PASS_L	-	No level	Pass line for VCOM_OPT
VCOM_OPT_R VCOM_OPT_L	O	Analog	VCOM optional buffer output.

4.2.5 Touch Related Pins

Name	I/O	PAD Type (Voltage Level)	Description
TP_RESX	I	Digital(IOVCC)	External reset for TP
TP_UART_TX	I/O	Digital(IOVCC)	UART TX pad
TP_INT	O	Digital(IOVCC)	Touch screen interrupt
TP_I2C_SDA	I/O	Digital(IOVCC)	I2C interface data pin
TP_I2C_SCL	I	Digital(IOVCC)	I2C interface clock pin
TP_SPI_CS	I	Digital(IOVCC)	Slave chip select pin in SPI interface
TP_SPI_MISO	O	Digital(IOVCC)	Slave input data pin in SPI interface
TP_SPI_MOSI	I	Digital(IOVCC)	Slave output data pin in SPI interface
TP_SPI_SCL	I	Digital(IOVCC)	Slave clock pin in SPI interface
FLASH_HOLD	O	Digital(IOVCC)	Master hold signal in SPI interface
FLASH_WP	O	Digital(IOVCC)	Master write prot. In SPI interface
FLASH_CS	O	Digital(IOVCC)	Master chip select in SPI interface
FLASH_MISO	I	Digital(IOVCC)	Master input data in SPI interface
FLASH_MOSI	I/O	Digital(IOVCC)	Master output data in SPI interface
FLASH_SCL	I	Digital(IOVCC)	Master clock signal in SPI interface
RX[576:1]	O	Analog	Output source driver signals. The D/A converted 256-gray-scale analog voltage is output.
RX0D[0:2], RX1D[0:2], TX0D, TX1D	O	Analog	Touch keys, If not used, please keep it open.

4.2.6 Test/Dummy Pins

Name	I/O	PAD Type (Voltage Level)	Description
SDUM0:3	O	--	Dummy pad
GRID1:20	O	--	Dummy pad
DUMMY	O	--	Dummy pad
TEST0~16 TEST20~36	O	--	TEST pad, please keep these pads open.
VDDATEST0~2_L VDDATEST0~2_R	O	--	TEST pad, please keep these pads open.

TP_OPT_1~4	O	--	TEST pad, please keep these pads open.
TP_TEST0~9	O	--	TEST pad, please keep these pads open.
TP_TEST_EN	I	--	TP TEST enable pin
80TEST0~11	O	--	TEST pad, please keep these pads open.
PWR_TEST1~4	O	--	TEST pad, please keep these pads open.

4.3　Power Supply Configuration

VGH (7 ~ 18 V, 100 mV/step)

AVDD 4.5 ~ 6.3 V

GVDDP (20 mV/step)

IOVCC 1.65 ~ 1.95 V
DPHYVCC

AGND 0 V
DGND

GVDDN (20 mV/step)

AVEE -4.5 ~ -6.3 V

VGL (-7 ~ -18 V, 100 mV/step)
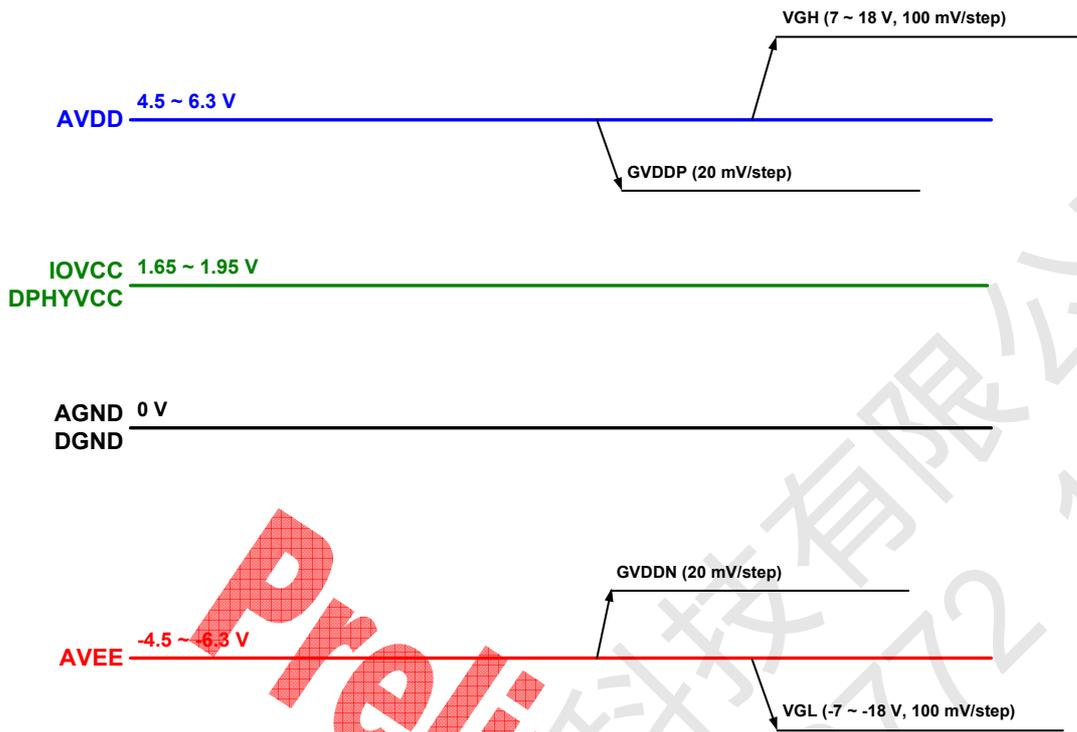
5   FUNCTION DESCRIPTION

5.1   Frame Tearing Effect Interface

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line off & on commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.1.1   Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only (Figure 1):

Figure 1 Mode1

tVDH= The LCD display is not updated from the Partial Memory or Host

tVDL= The LCD display is updated from the Partial Memory or Host

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 1680 H-sync pulses per field. (Figure 2)
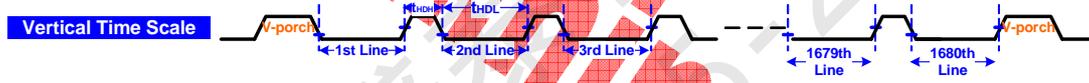
Figure 2 Mode2

tHDH= The LCD display is not updated from the Partial Memory or Host

tHDL= The LCD display is updated from the Partial Memory or Host

Mode3, in this mode, the tearing effect output when the display reaches line N. The output signal length of the high level is one line period. In below figure, it shows the TE pulse that can be select from 1st line to 1920th line by CMD44h.P1 and CMD44.P2 (Figure 3)
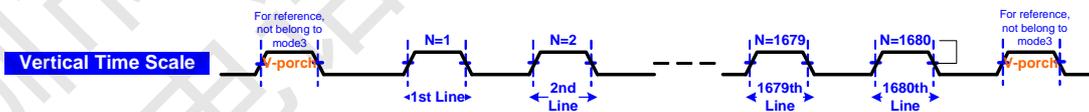
Figure 3 Mode3

CMD 35h	CMD 44h	TE output
TEM	TESN	
0	0	TE high in V-porch region (mode1)
1	0	TE high in all V-porch and H-porch region (mode2)
0	≠0	TE high at N-th line (mode3)

1	≠0	Same as mode2

Where mode1, mode2 and mode3 timing chart is shown in below (Figure 4):
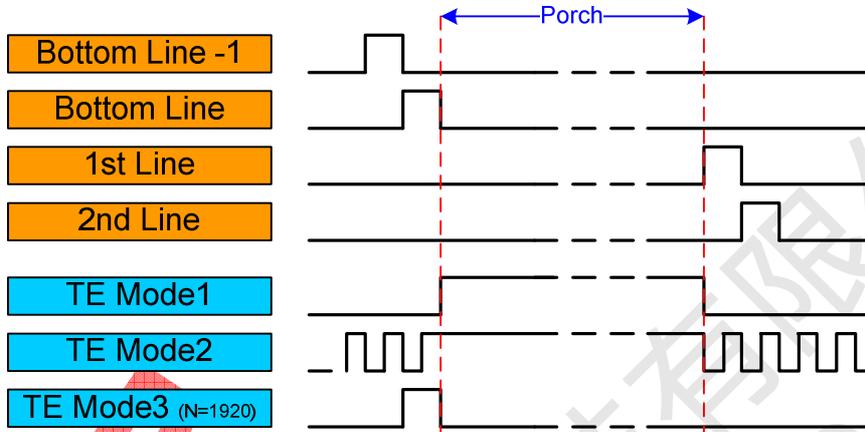
Figure 4 TE Mode

Note: during sleep in mode, the Tearing output pin is active low.

AC characteristics of Tearing Effect Signal (FTE)

FTE's rising-time and falling-time (tr,tf) are stipulated to equal to or less than 15ns when maximum loading is 30pF.
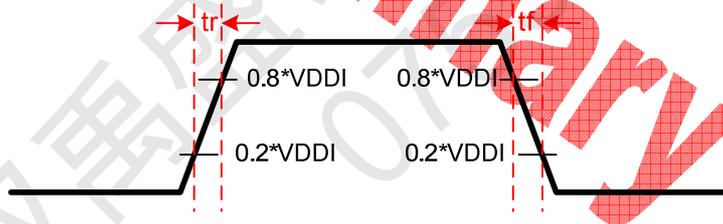
Figure 5 AC characteristics of Tearing Effect Signal

5.2 Content Adaptive Backlight Control (CABC2.0)

5.2.1 Definition of CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus the power consumption reduction

Definition of Modes and target power reduction ratio:

Off mode: Content Adaptive Brightness Control functionality is totally off.

UI [User Interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.

Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.

Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

	Off ode	UI image mode	Still picture mode	Moving image mode
Power Reduction	0%	10% or Less	More than 30%	More than 30%
Image Quality	Best	Approaching Best	Some image degradation	Some image degradation

Note 1: Updating partial area of the image data should be supported by CABC functionality.
Note 2: Processing power consumption of CABC should be minimized.
Note 3: Customer need program NVM GAMMA when using CABC.

The transition time for dimming function is illustrated below.

● Content Adaptive Brightness Control

Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

● Image A: -20% brightness reduction

● Image B: -30% brightness reduction

● Image C: -10% brightness reduction

Transition time from the previous image to the current displayed image is "transition time A".
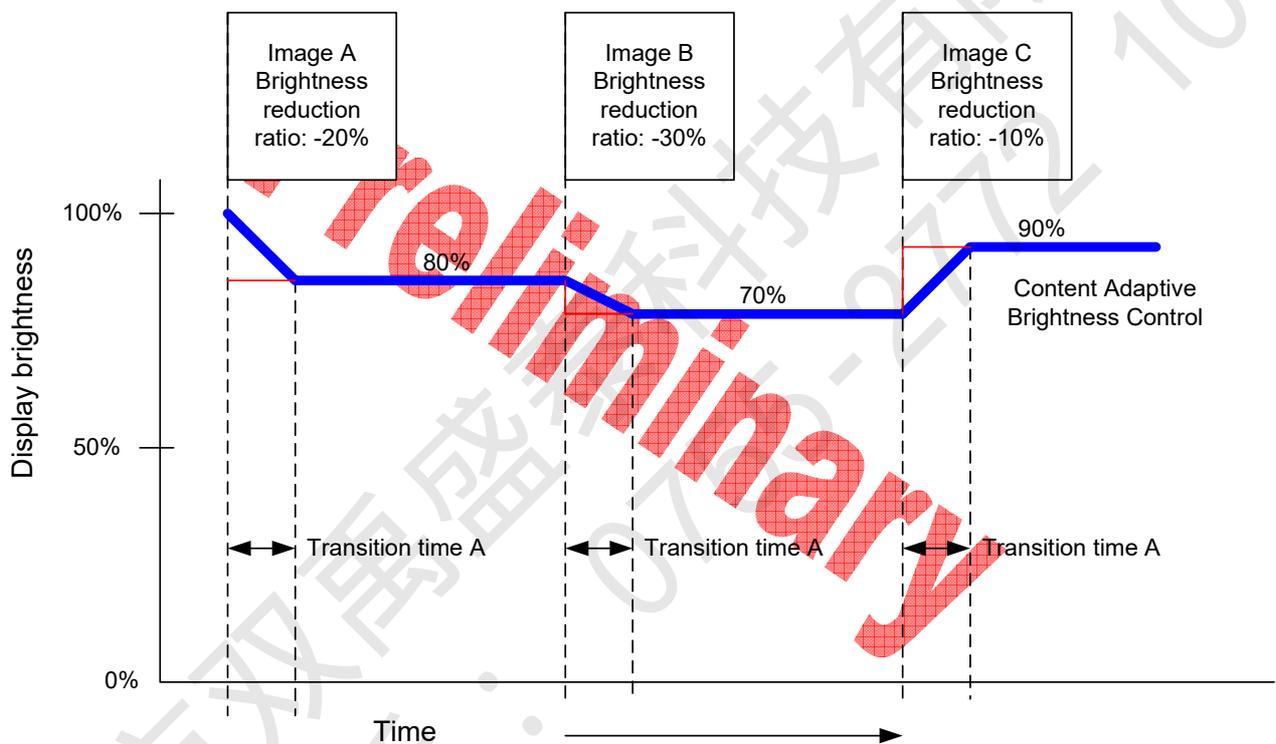
Figure 6 Transition time A

⚠️

● Manual brightness setting and Dimming function

Figure 7   Manual brightness setting and Dimming function

● Manual brightness setting and Dimming function
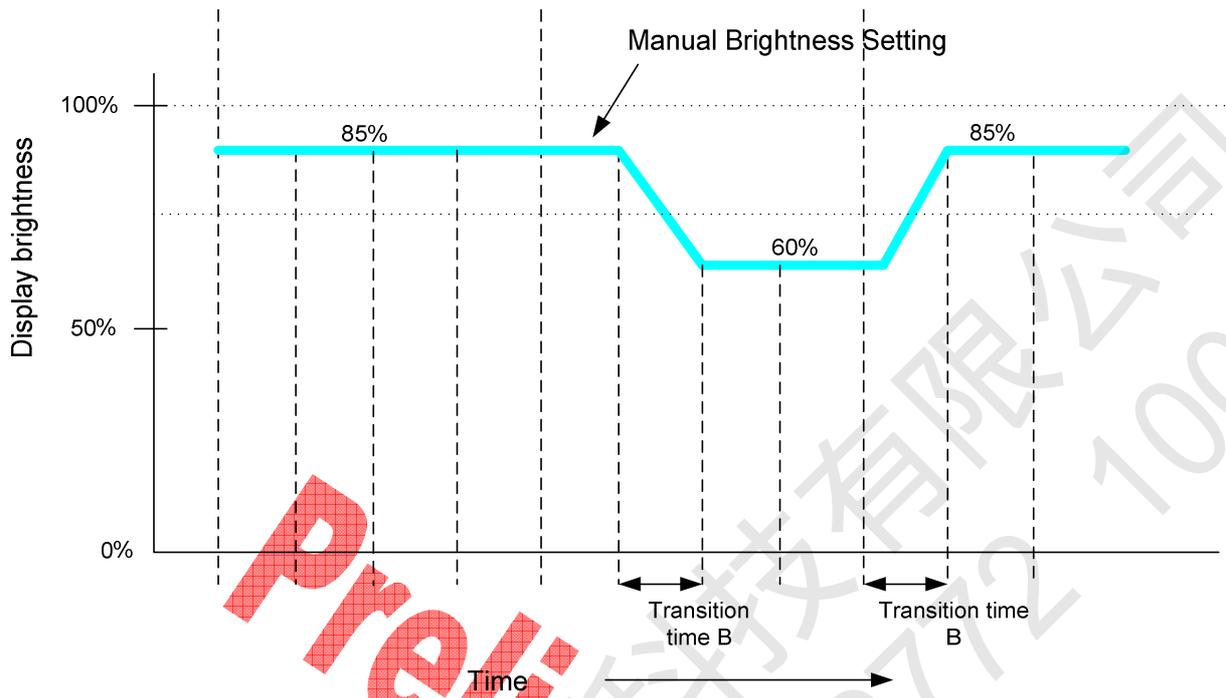
Figure 7   Manual brightness setting and Dimming function

● Combine Display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A+B.
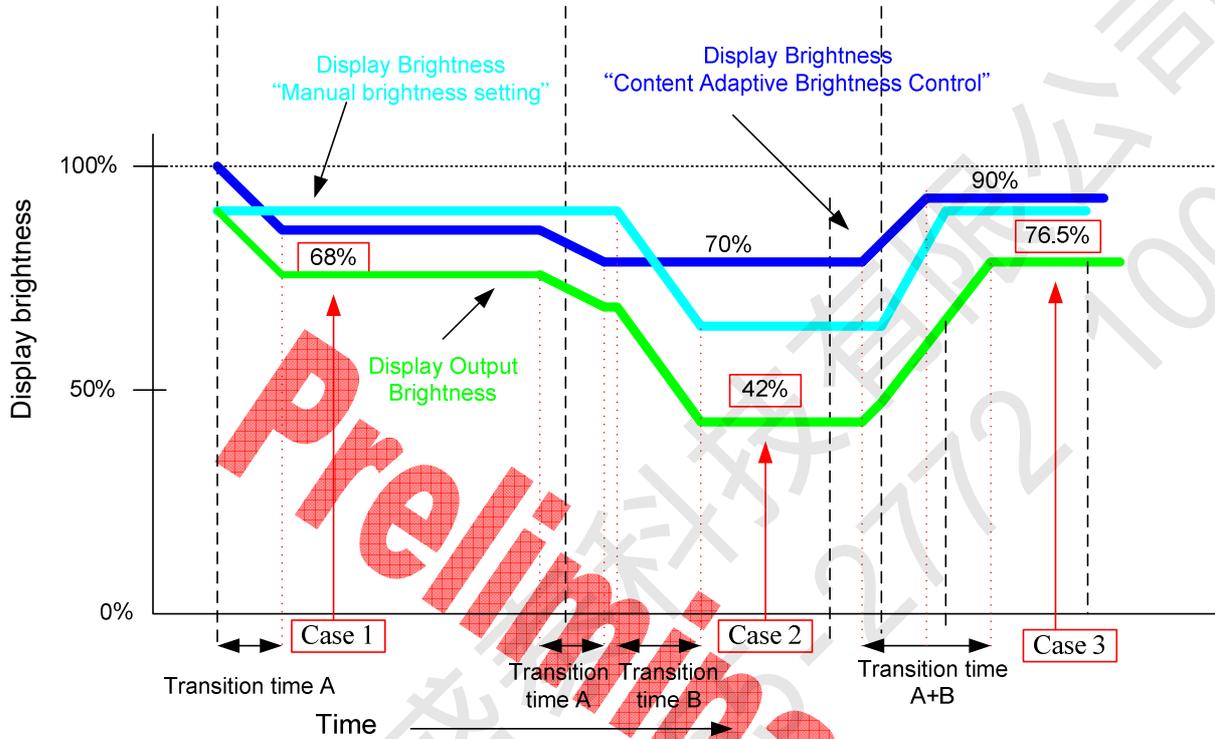
Figure 8   Maximum transition time is transition time A+B

Brightness level calculates with the following formula.

Display Output brightness = Manual Brightness setting * CABC brightness ratio

	Manual Brightness setting	Brightness ratio [CABC]	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Transition time from the current brightness to target brightness is A+B in the worst case.

5.2.2 Minimum Brightness Setting of CABC Function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness cannot be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. "Read CABC minimum brightness (5Fh)" always read the setting value of "Write CABC minimum brightness (5Eh)".

	WRCABC (55h)	**Function**	**RDCABCMB (5Fh)**	**Image**
Sleep-in		NA	WRCABCMB (5Eh)	
CABC off	00b	Disable	WRCABCMB (5Eh)	Original
CABC on	01b/10b/11b	Enable	WRCABCMB (5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.
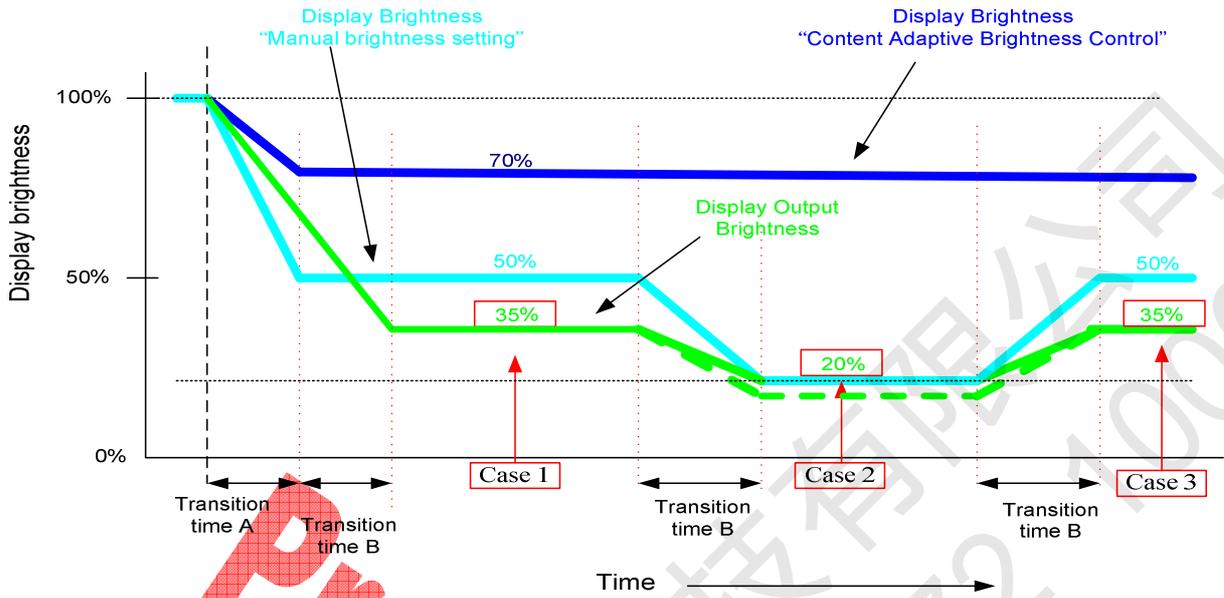
Figure 9 CABC minimum brightness setting

CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	Brightness ratio [CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

5.2.3   Display Dimming

5.2.3.1   General Description

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement. The basic idea is described below.
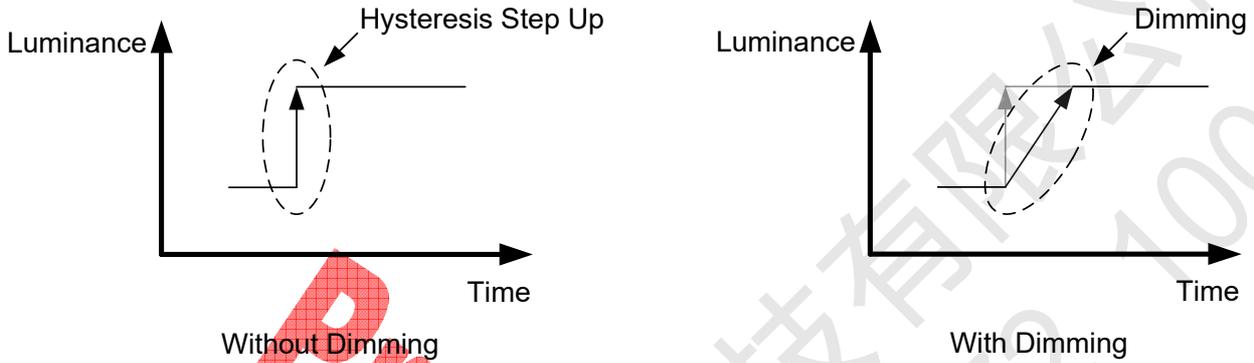
Dimming function can be enable and disable. See "Write CTRL Display (53h)" (bit DD) for more information.

5.2.3.2   Dimming Requirement

Dimming function in the display module should be implemented so that 400-600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

An upward example is illustrating below
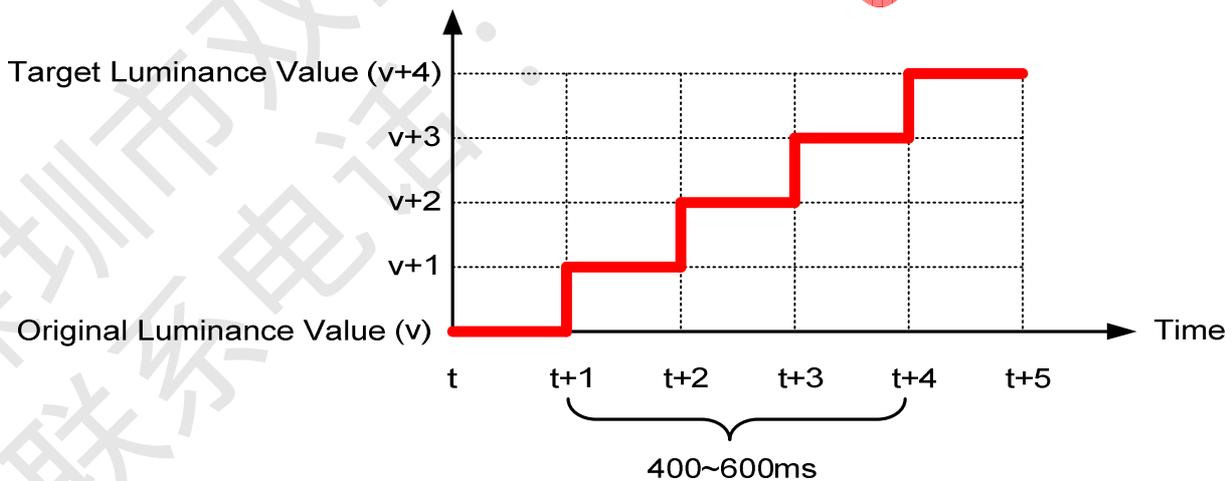
Figure 10 Dimming Requirement

5.2.4   Definition of Brightness Transition Time

● Shorter transition time than 500ms.

There is some stable time between transitions. Below drawing is for transition time: 400ms.
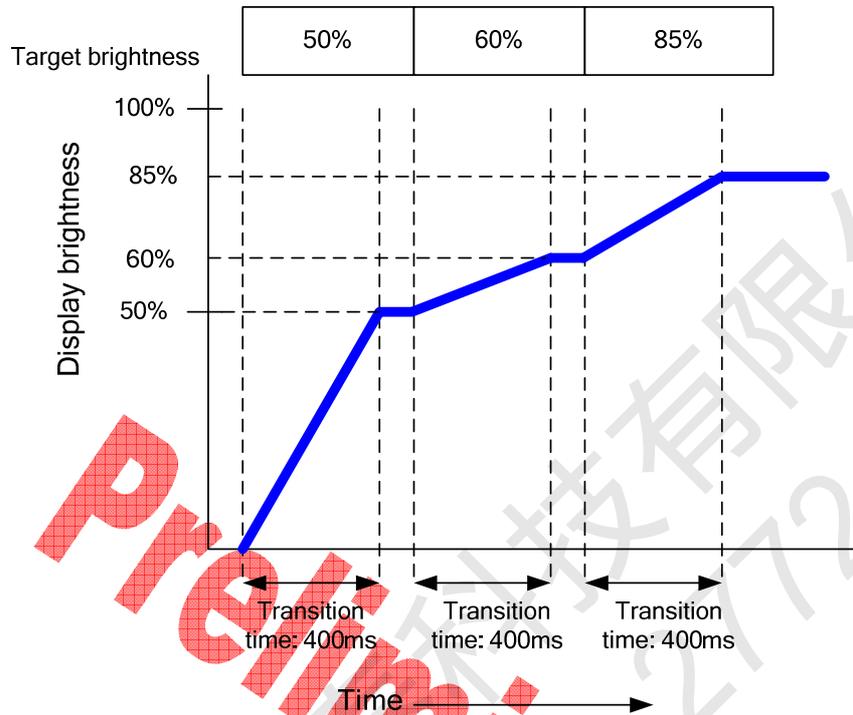
Figure 11 Shorter Transition time than 500ms

● Longer transition time than 500ms

There is no any stable time between transitions. Below drawing is for transition time: 600ms.

It starts 2nd transition when the 2nd brightness target, 60%, is fixed during first transition time. Change point for the new target is at 41.6% brightness.

It starts 3rd transition at 57% brightness
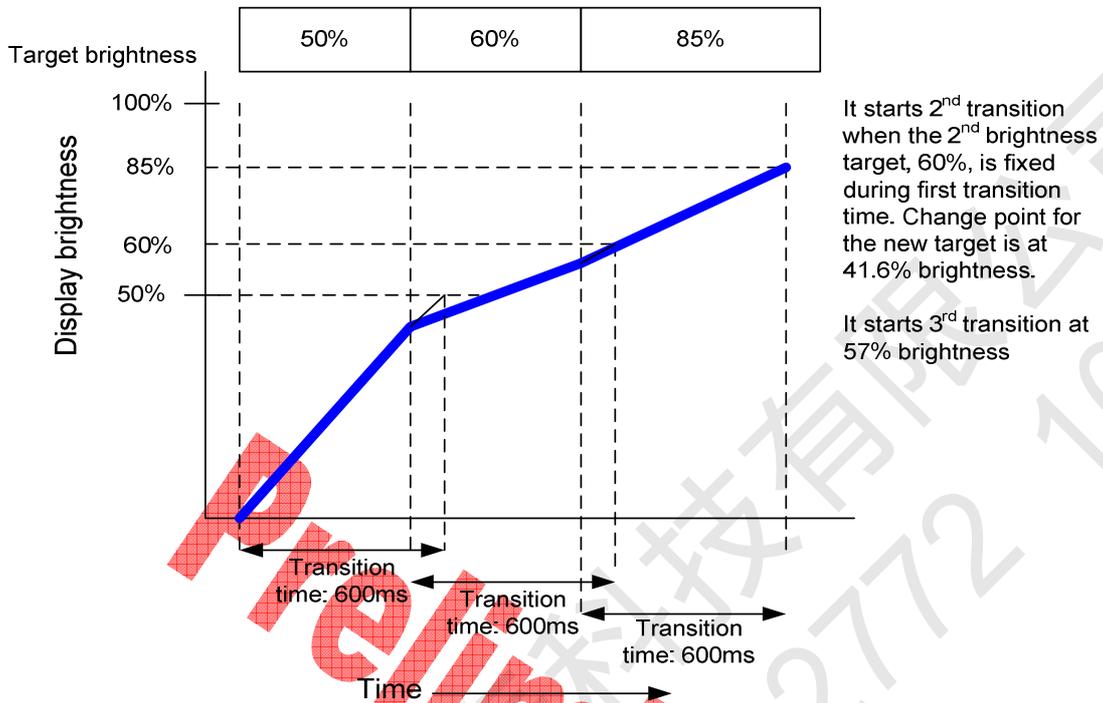
Figure 12 Longer Transition time than 500ms

5.3 Color Enhancement (CE2.0)

Color enhancement function enhances the color saturation by gamut expansion.
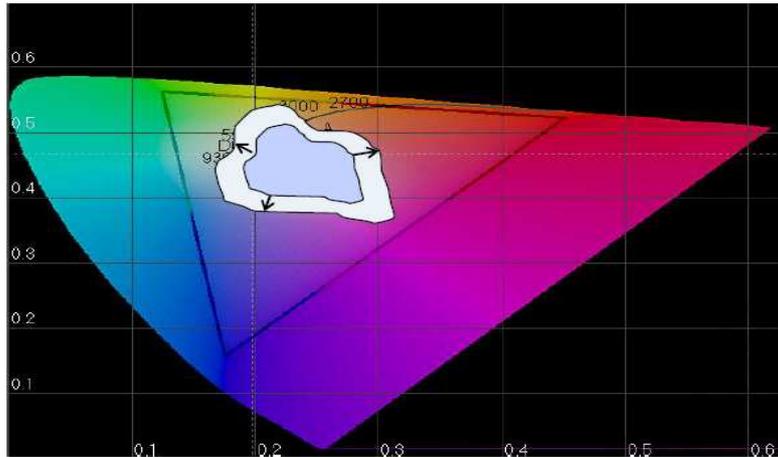
Figure 13 Color Gamut Expansion

An example of the color enhancement function is illustrated below:

Color Enhancement Off	Color Enhancement On
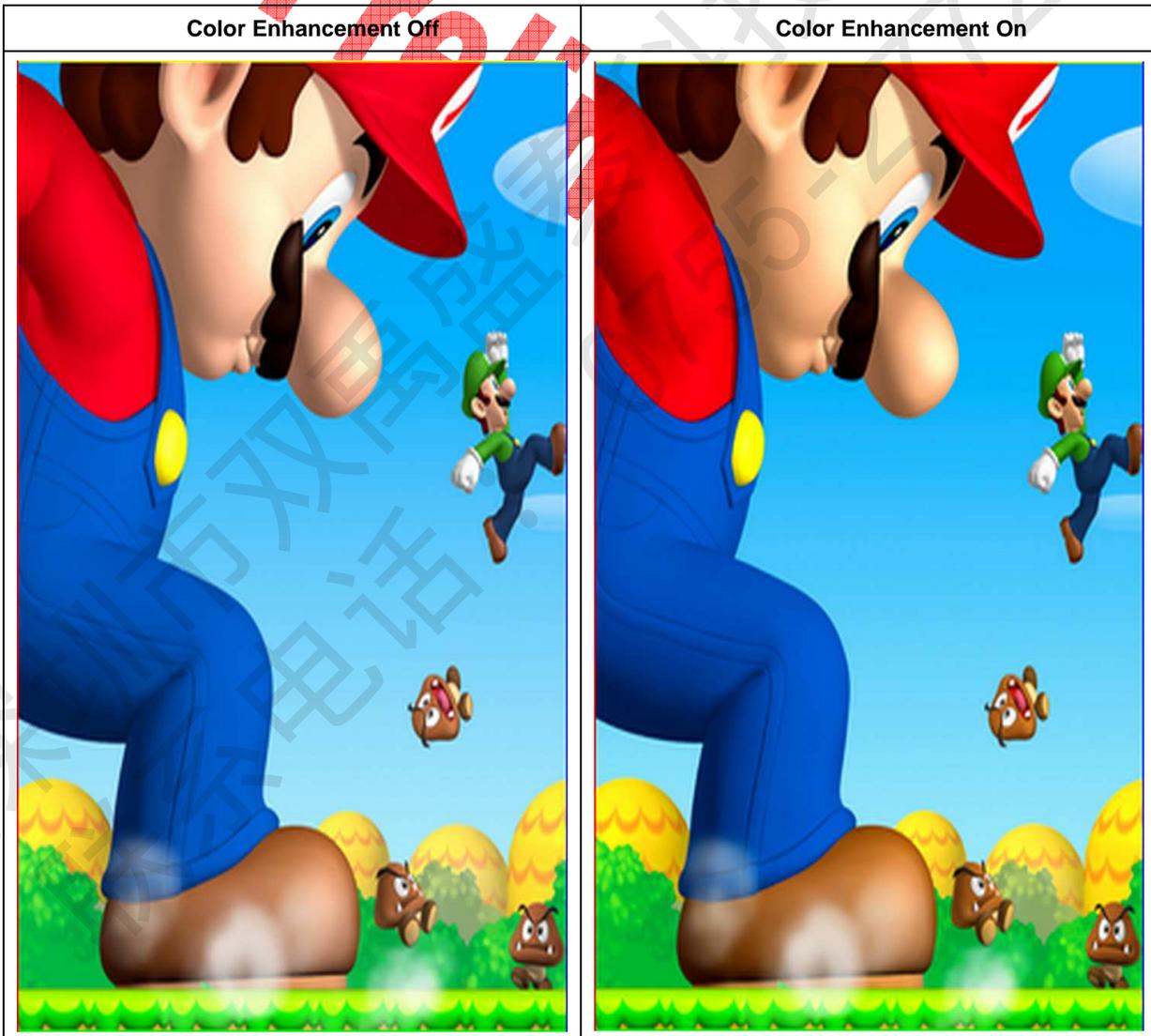
5.4 MIPI-DSI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High-Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low-Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

5.4.1   Display Module Pin Configuration for DSI
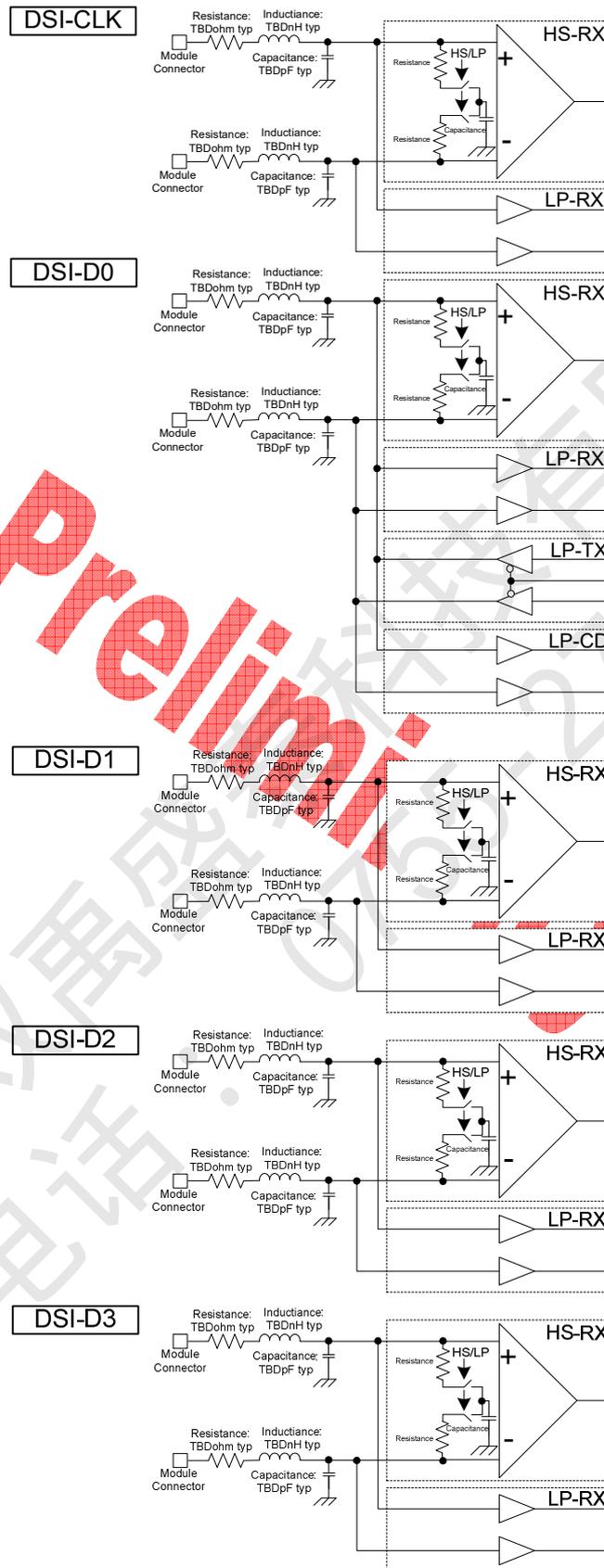
5.4.2   Display Serial Interface (DSI)

5.4.2.1   General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface level : Low level communication

- Packet level : High level communication

5.4.2.2   Interface level communication

5.4.2.2.1   General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven

Low-Power (LP) or High-Speed (HS) mode. Data lane1, data lane2 and data lane3 can be driven High-Speed mode only.

	Lane support mode	
Clock Lane	Unidirectional lane High-Speed Clock only Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane Forward high-speed only Bi-directional Escape Mode Bi-direction LPDT	
Data Lane1/2/3	Unidirectional lane Forward high-speed only Simplified Escape Mode(ULPS Only)	

Figure 14 The Interface Color Lane Types and Support Mode

Low-Power mode means that each line of the differential pair is used in single end mode and a differential receiver is

disable (A termination resistor of the receiver is disable) and it can be driven into a Low-Power mode.

High-Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the

single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU

to the display module and vice versa.

The State Codes of the High-Speed (HS) and Low-Power (LP) lane pair are defined below.

Lane Pair	Line Voltage Levels		High-Speed(HS)	Low-Power(LP)	
State Code	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Request	Mark-0
LP-10	LP High	LP Low	N/A	LP-Request	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note 2

High-Speed and Low-Power Lane Pair State Descriptions

Notes:

1. During High-Speed transmission the Low-Power observe LP-00 on the Lines.

2. If LP-11 occurs during Escape mode the Lane returns to Stop state.

5.4.2.2.2 DSI-CLOCK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low-Power Mode (LPM LP-11), Ultra-Low Power Mode (ULPM) or High-Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low-Power) when there is entering or leaving Low-Power Mode (LPM) or Ultra-Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low-Power) when there is entering in or leaving out High-Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

Figure 15 Clock Lanes Power Modes

5.4.2.2.2.1 Low-Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low-Power Mode (LPM),when DSI-CLK lanes are entering LP-11 State Code , in

three different ways:

After SW Reset, HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP10=>LP-11(LPM).

This sequence is illustrated below.
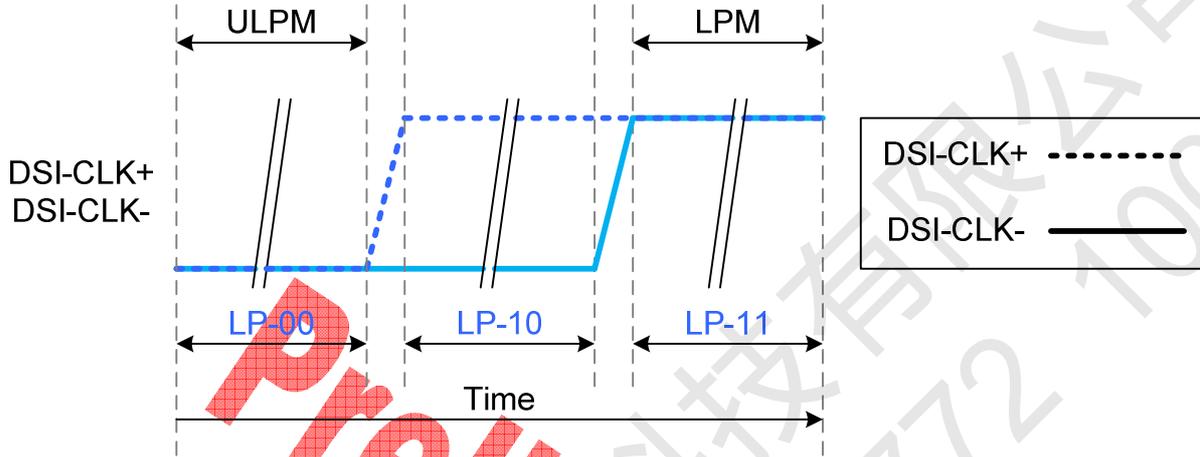
Figure 16 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High-Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.
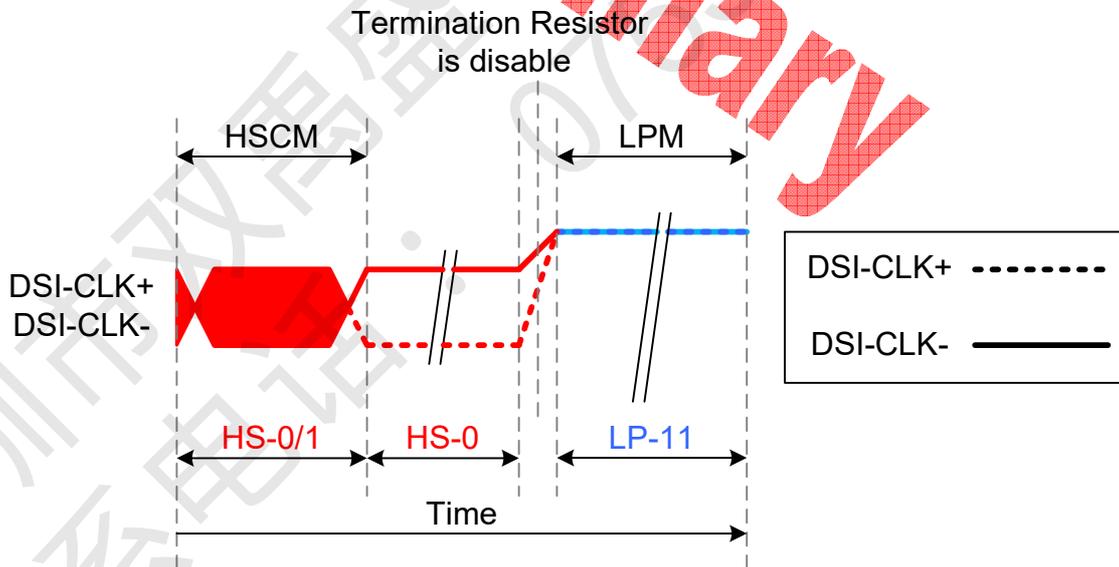
Figure 17 From HSCM to LPM

All three mode changes are illustrated a flow chart below.
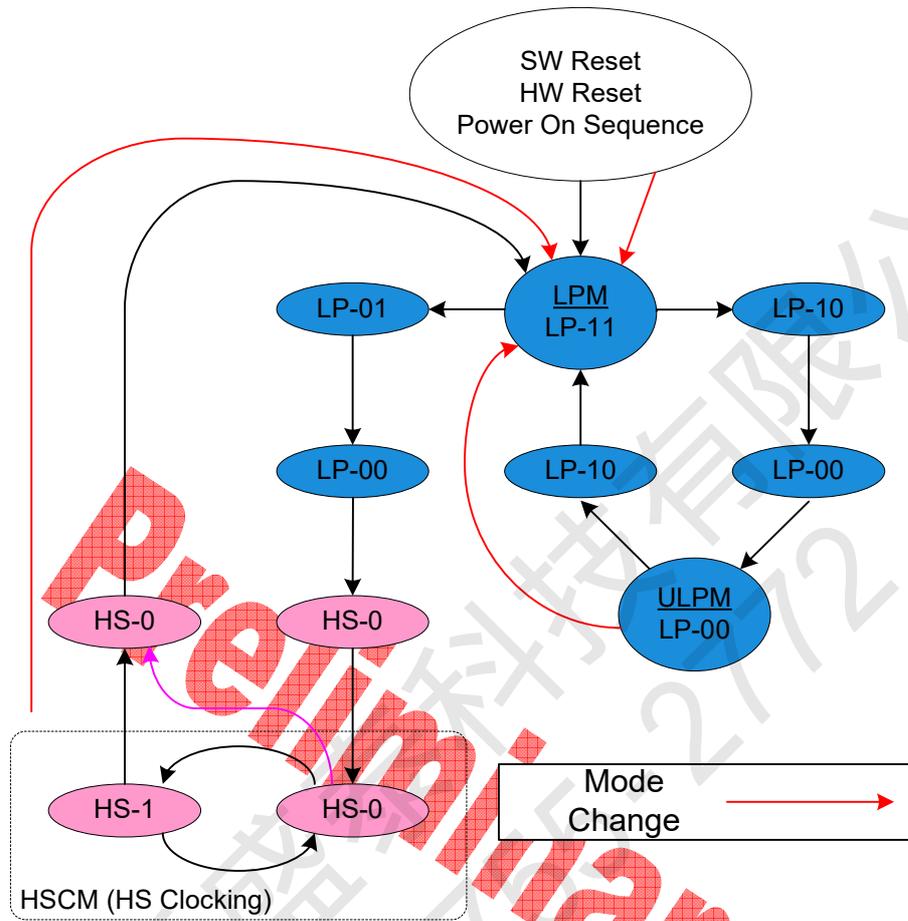
Figure 18 All three mode changes to LPM

5.4.2.2.2.2 Ultra-Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra-Low Power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State

Code. The only entering possibility if from the Low-Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM).

This sequence is illustrated below:
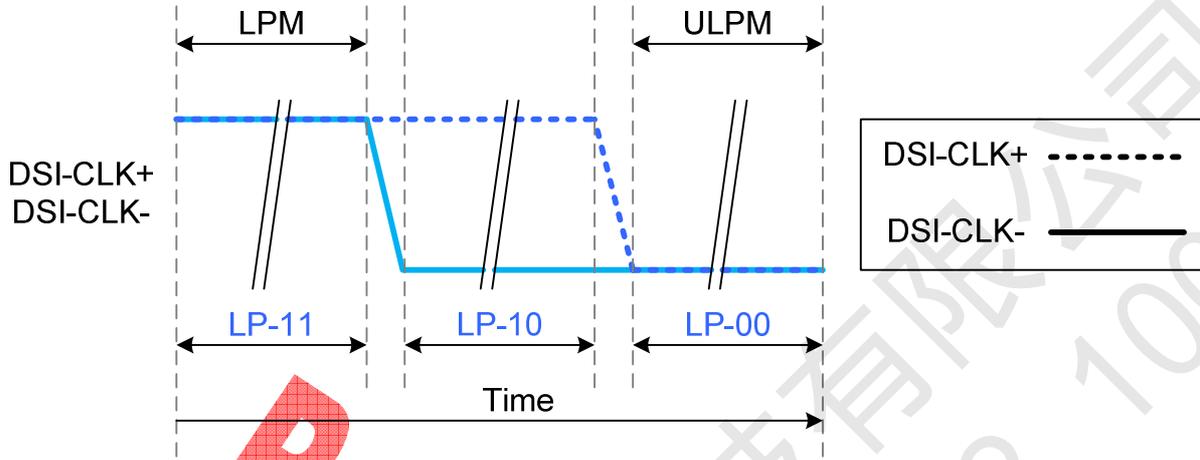
Figure 19 From LPM to UPLM

The mode change is also illustrated below:
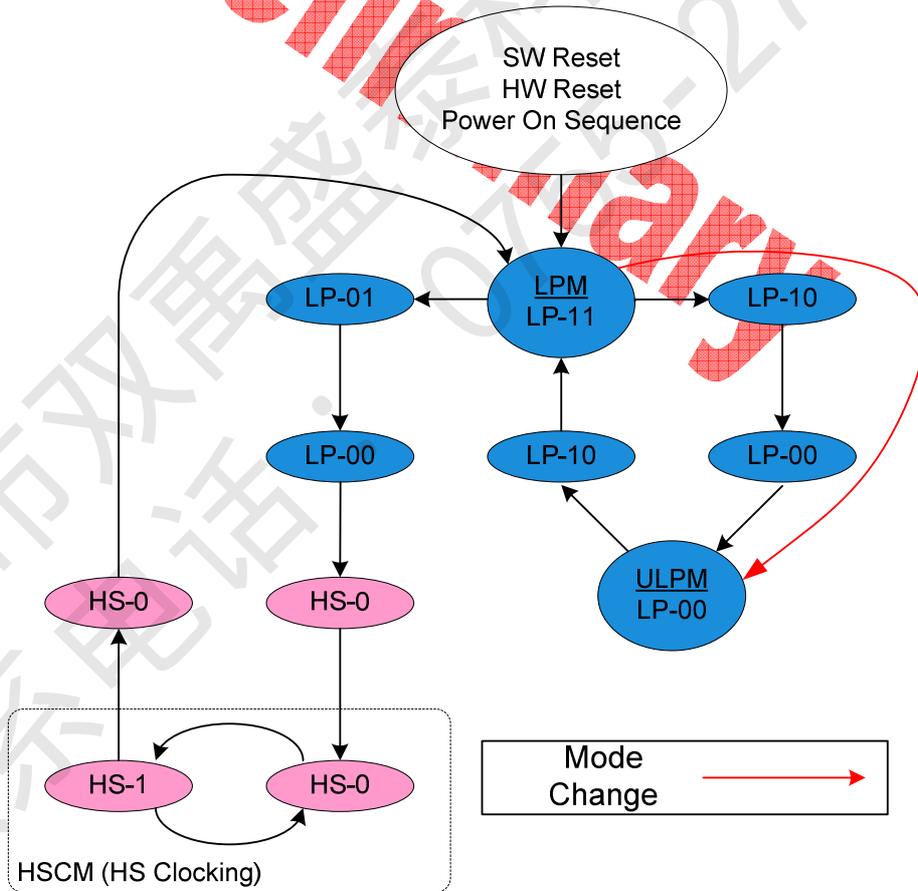
Figure 20 The mode change from LPM to UPLM

5.4.2.2.2.3 High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High-Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work

between HS-0 and HS-1 State Codes. The only entering possibility is from the Low-Power Mode (LPM, LP-11 State Code)

=>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.
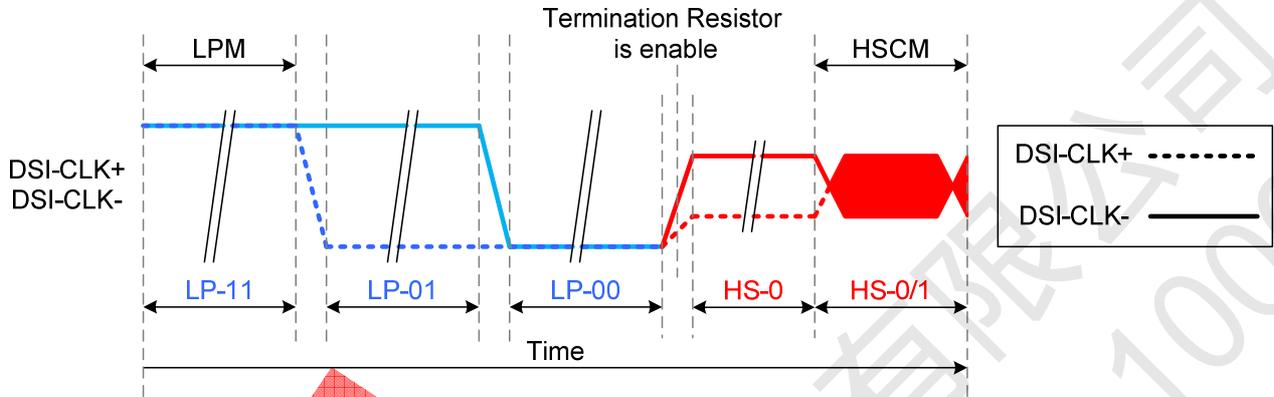
Figure 21 From LPM to HSCM

The mode change is also illustrated below:
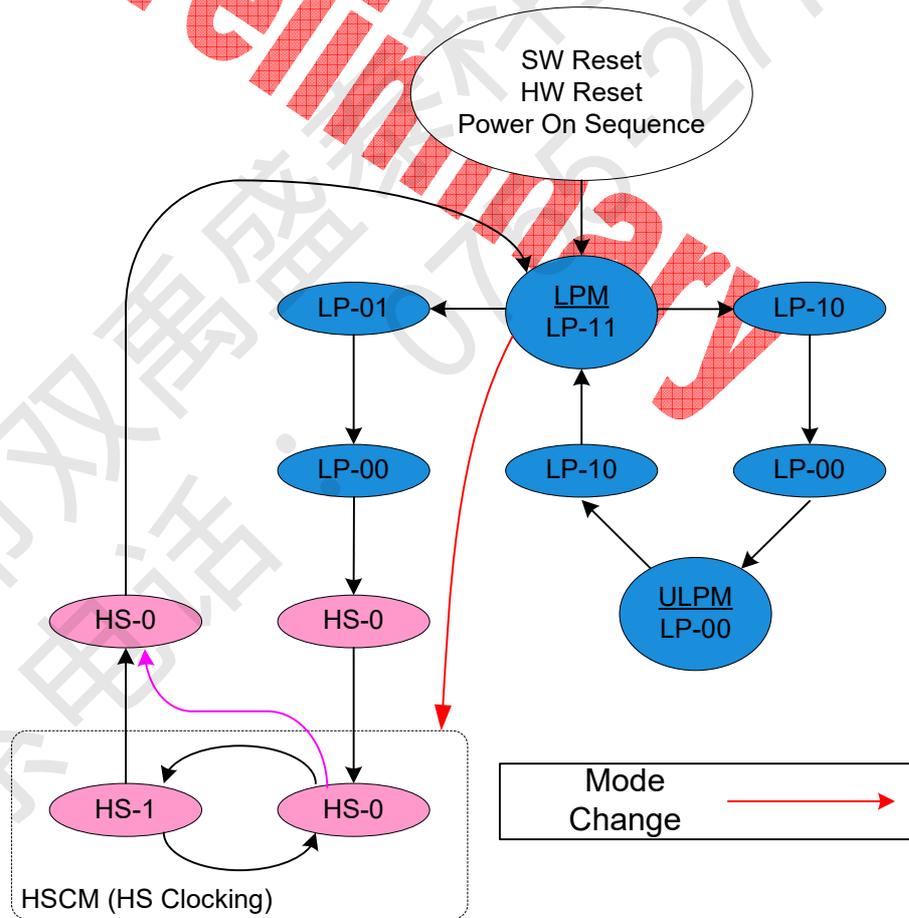
Figure 22 Mode Change from LPM to HSCM on the Flow Chart

The High-Speed clock (DSI-CLK+/-) is started before High-Speed data is sent via DSI-Dn+/- lanes. The High-Speed clock continues clocking after the High-Speed data sending has been stopped.
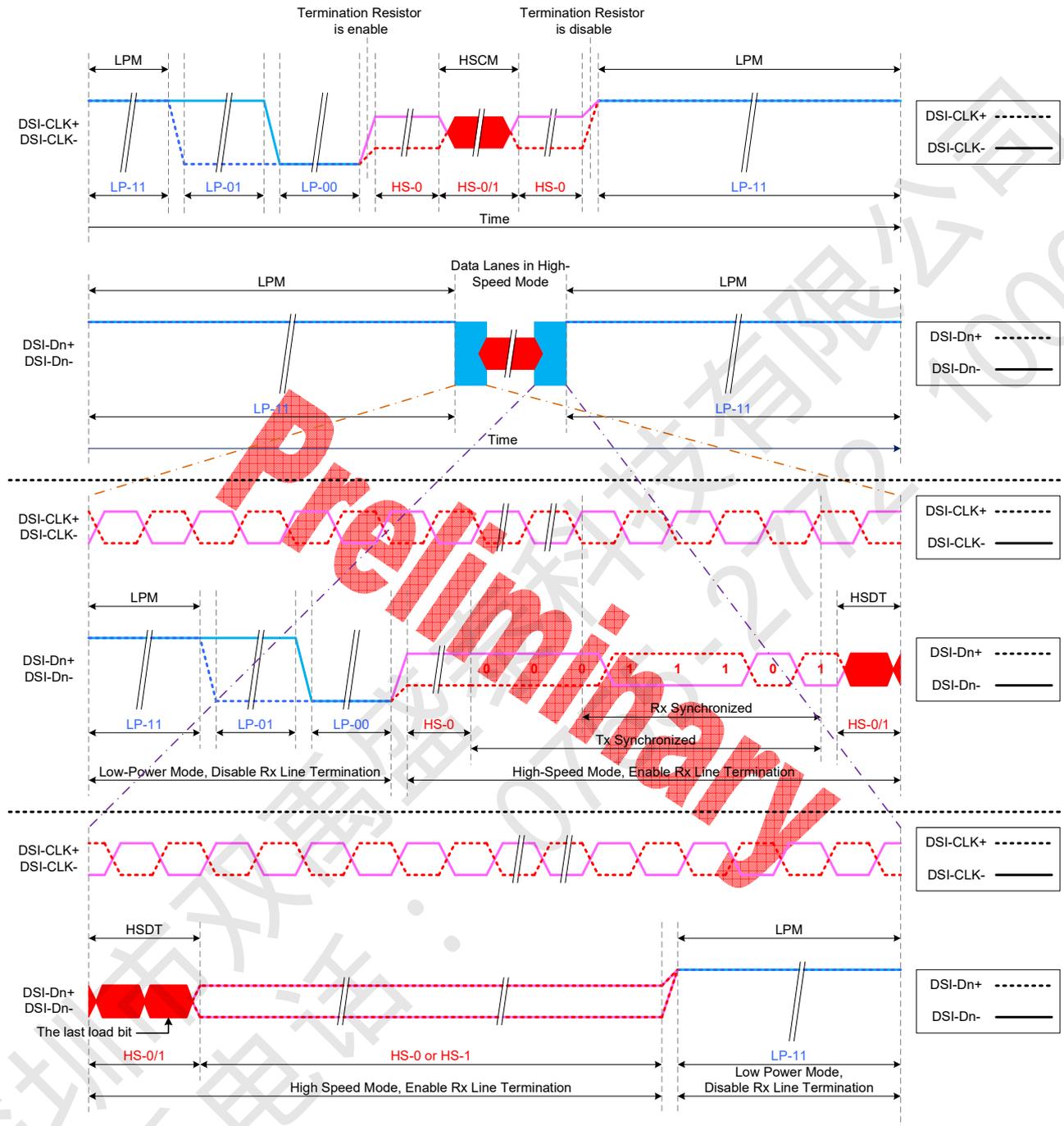
Figure 23 High-Speed Clock Burst

Note:

If the last load bits is HS-0, the transmitter changes form HS-0 to HS-1.

If the last load bits is HS-1, the transmitter changes form HS-1 to HS-0.

5.4.2.2.3 DSI-DATA Lanes

5.4.2.2.3.1 General

DSI-D0+/- data lanes can be driven in different modes which are:

• Escape Mode (Only DSI-D0+/- data lane is used)

• High-Speed Data Transmission (DSI-D0+/-, DSI-D1+/-, DSI-D2+/- and DSI-D3+/- data lanes are used)

• Bus Turnaround Request (Only DSI-D0+/- data lane is used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Entering and leaving sequence

5.4.2.2.3.2 ESCAPE MODE

Data lane0 (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low-Power (LP) mode.

These Escape Modes are used to:

• Send "Low-Power Data Transmission" (LPDT) e.g. from the MCU to the display module

• Drive data lanes to "Ultra-Low Power State" (ULPS)

• Indicate "Remote Application Reset" (RAR), which is reset the display module

• Indicate "Tearing Effect" (TEE), which is used for a TE trigger event from the display module to the MCU

• Indicate "Acknowledge" (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this

changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing

from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this

low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:
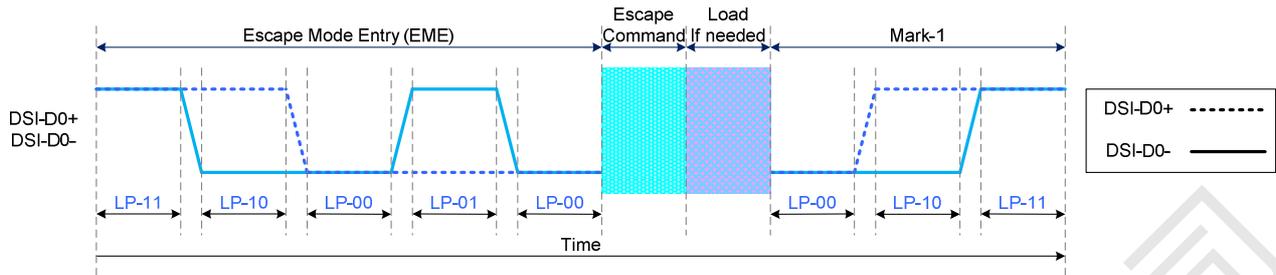
Figure 24 General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the Low-Power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit➜Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 bin	-	○
Ultra-Low Power Mode	Mode	0001 1110 bin	○	○
Underfined-1, Note 1	Mode	1001 1111 bin	-	-
Underfined-2, Note 1	Mode	1101 1110 bin	-	-
Remote Application Reset	Trigger	0110 0010 bin	-	○
Tearing Effect	Trigger	0101 1101 bin	-	-
Acknowledge	Trigger	0010 0001 bin	-	○
Unknow-5, Note 1	Trigger	1010 0000 bin	-	-

Notes:

1. This Escape command support has not been implemented on the display module.

2. n=1.

3. "○"=Supported

4. "-"=Not Supported

5. Tearing Effect Trigger cannot be used in MIPI Video mode.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low-Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

• Load (Data):

  One or more bytes (8 bits)

  Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:
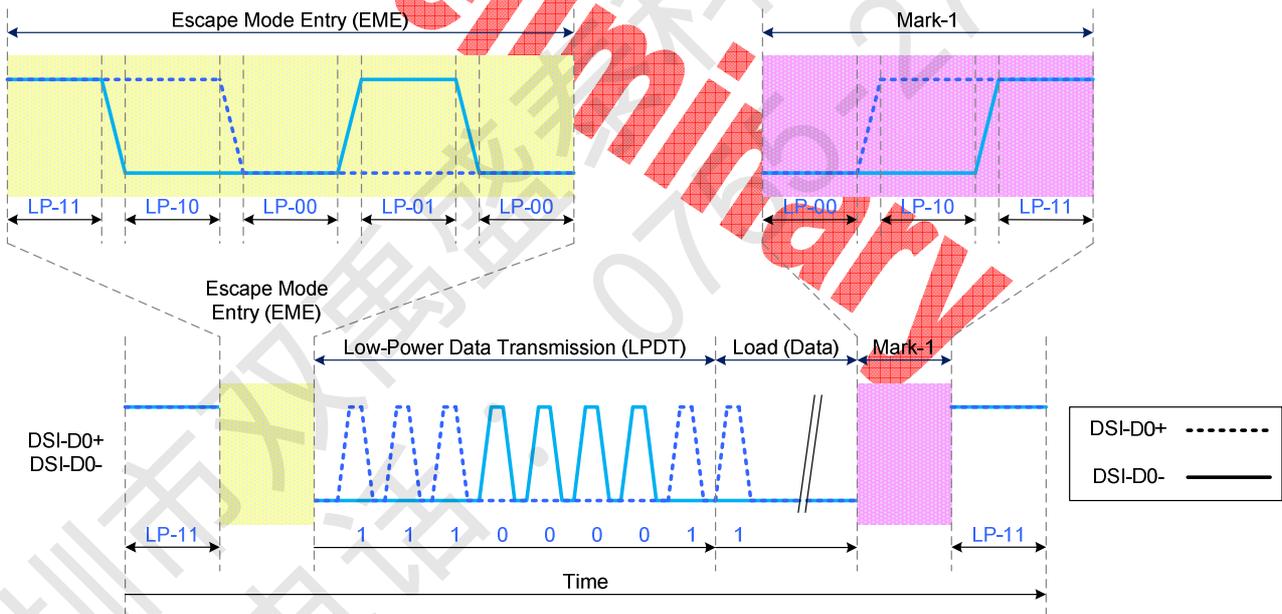
Figure 25 Low-Power Data Transmission (LPDT)

Note:

Load(Data) is presenting that the first bit is logical '1' in this example
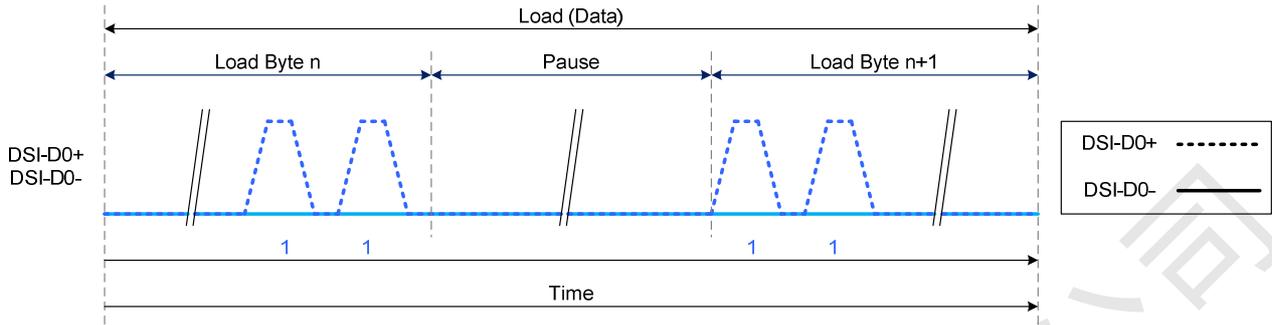
Figure 26 Pause (Example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:
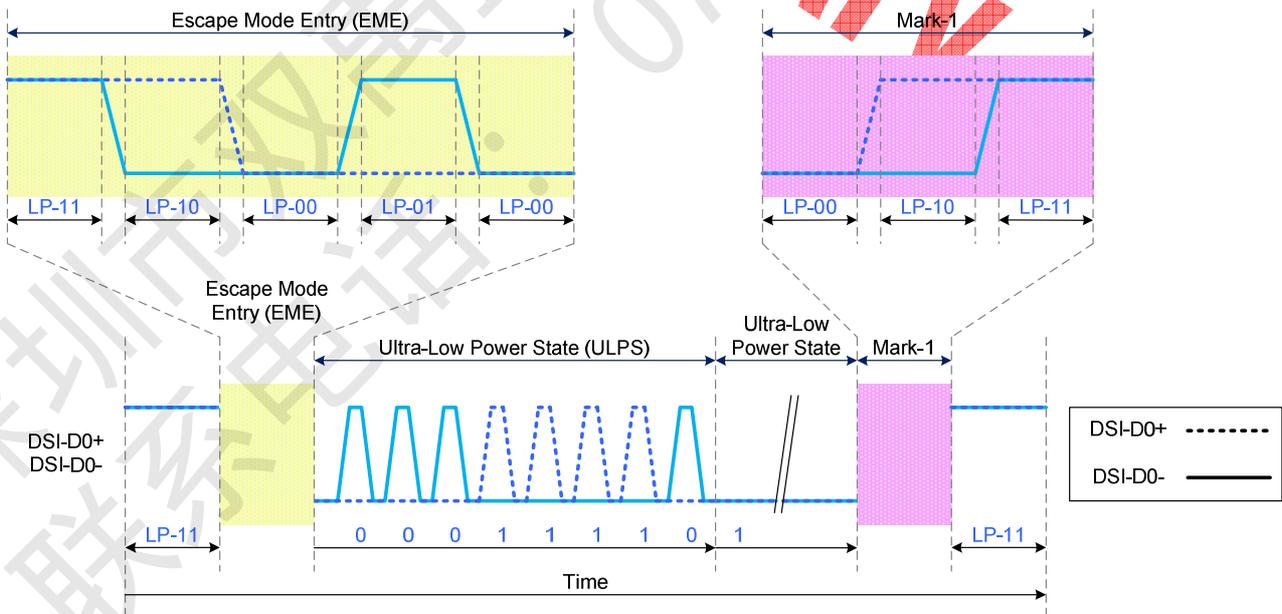
Figure 27 Ultra-Low Power State (ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:
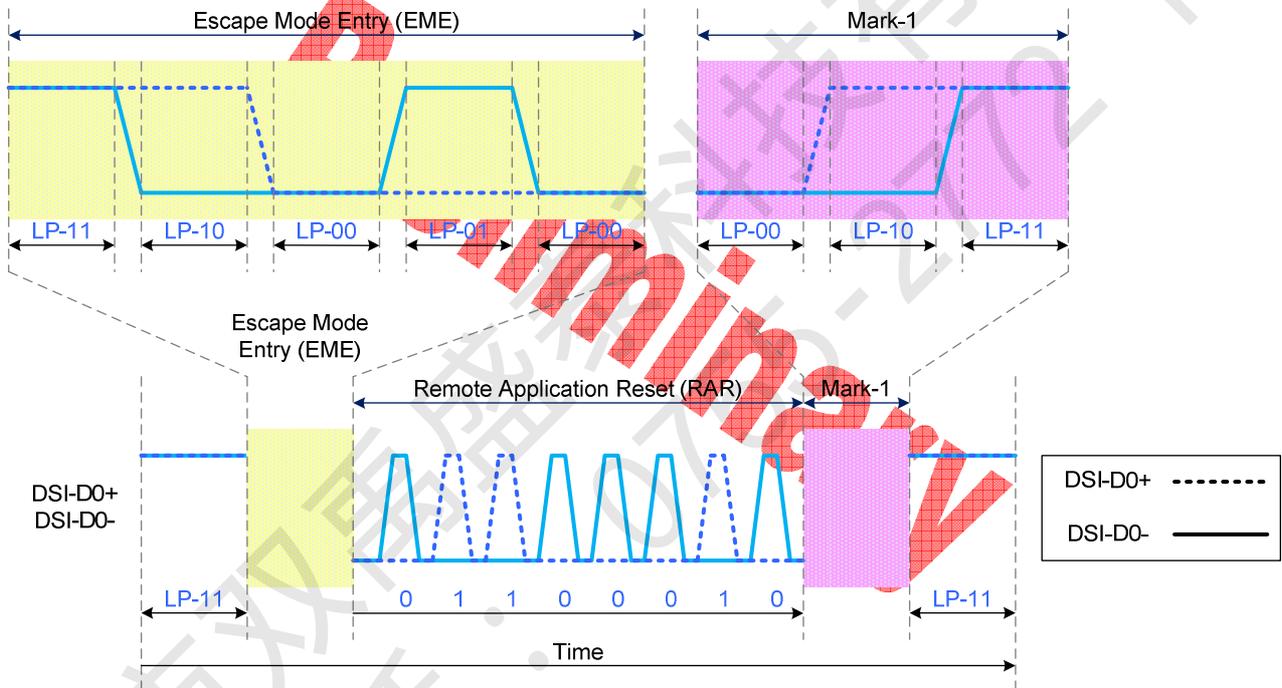
Figure 28 Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:
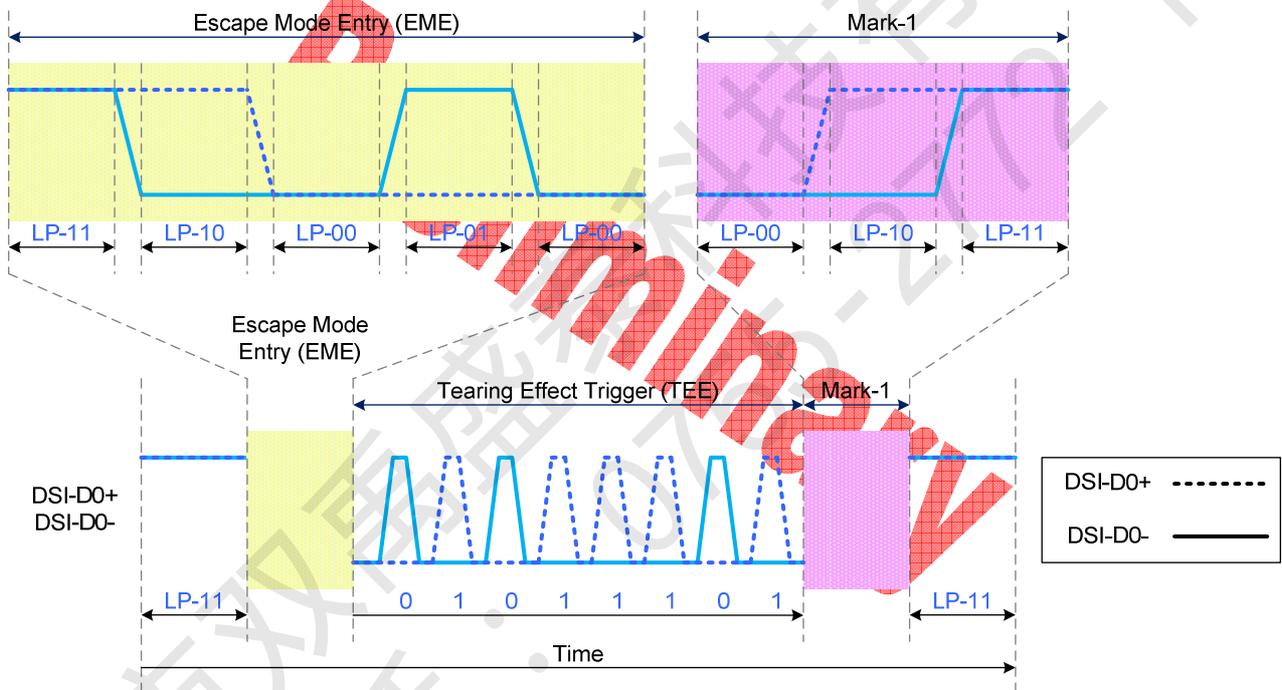
Figure 29 Tearing Effect (TEE)

Note: Tearing Effect (TEE) can not be used in MIPI Video Mode

Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:
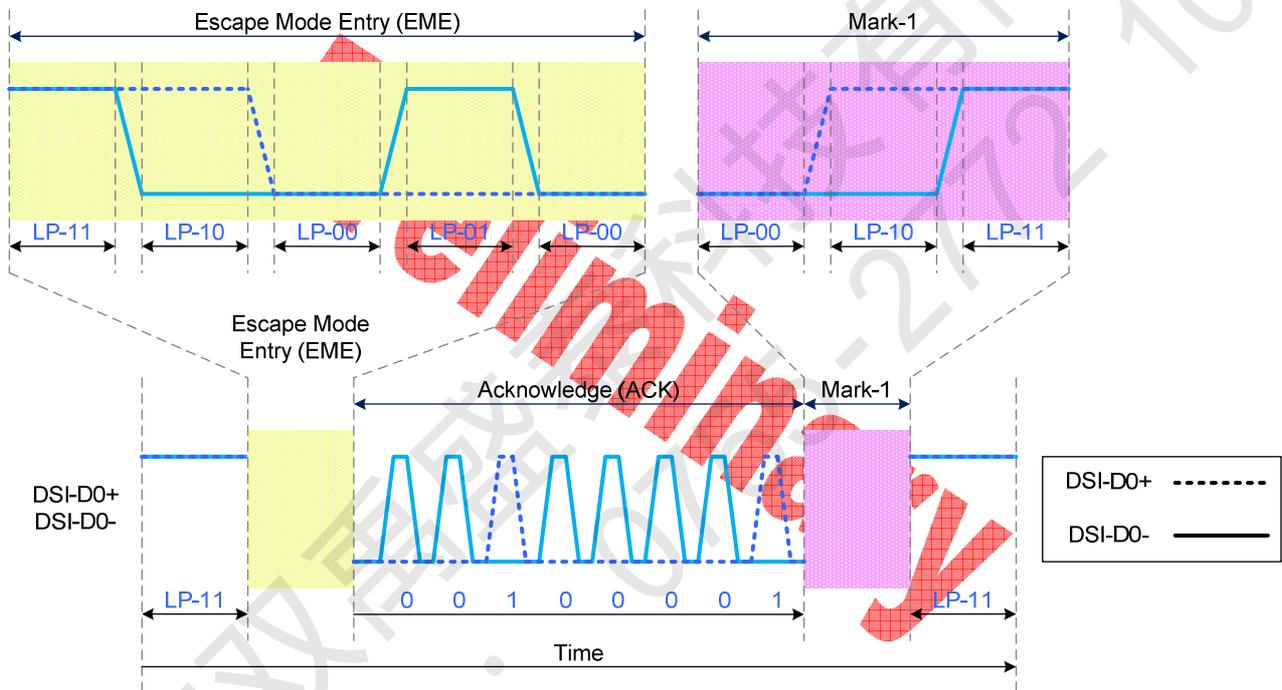
Figure 30 Acknowledge (ACK)

5.4.2.2.3.3 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T$_{SOT}$ of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "High-Speed Clock Mode (HSCM)".

Data lanes of the display module are entering (T$_{SOT}$) in the High-Speed Data Transmission (HSDT) as follows

• Start: LP-11

• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T$_{SOT}$ of HSDT) sequence is illustrated below
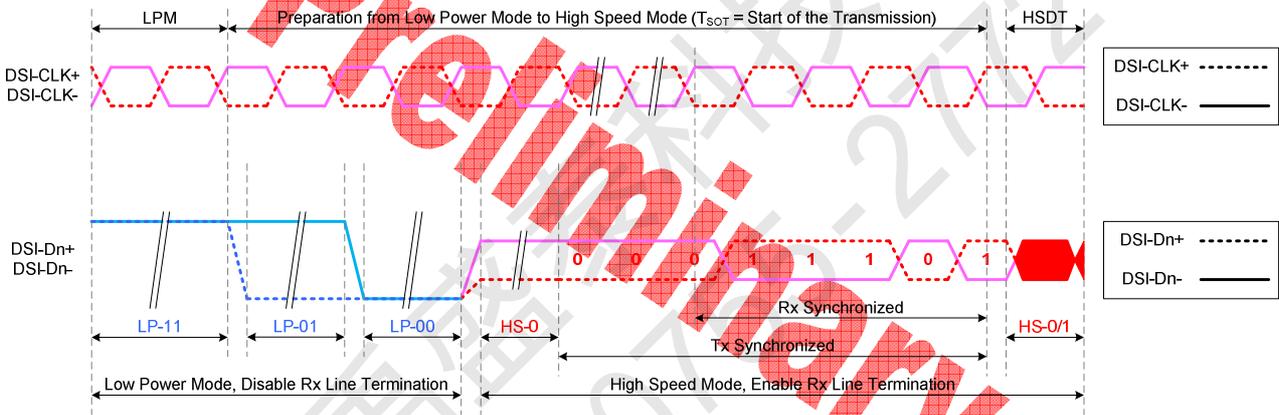
Figure 31 Entering High-Speed Data transmission (T$_{SOT}$ of HSDT)

Leaving High-Speed Data Transmission (T$_{EOT}$ of HSDT)

The display module is leaving the High-Speed Data Transmission (T$_{EOT}$ of HSDT) when Clock lanes DSI-CLK+/- are in the

High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more

information on chapter "High-Speed Clock Mode (HSCM)".

Data lanes of the display module are leaving from the High-Speed Data Transmission (T$_{EOT}$ of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

• Stops High-Speed Data Transmission

MCU changes to HS-1, if the last load bit is HS-0

MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T$_{EOT}$ of HSDT) sequence is illustrated below
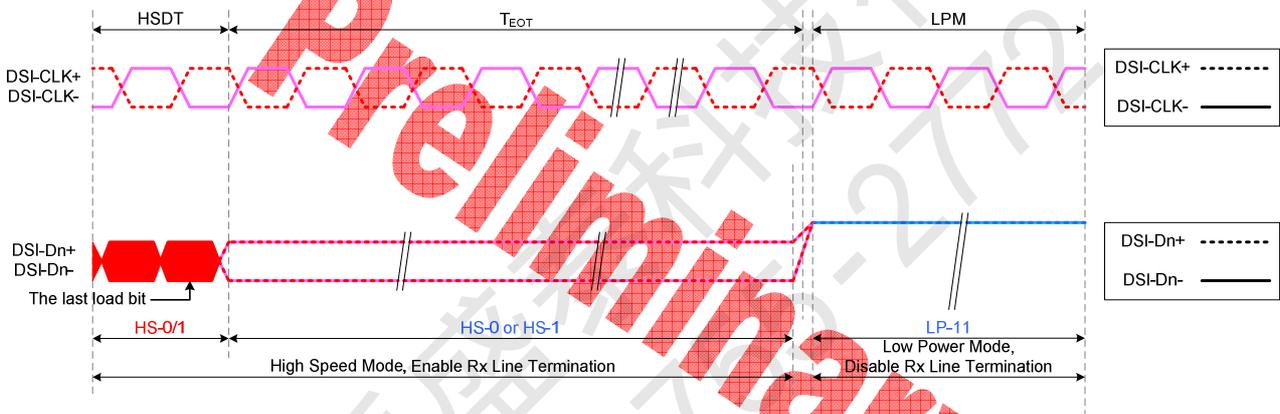
Figure 32 Leaving High-Speed data Transmission (T$_{EOT}$ of HSDT)

Burst of the High-Speed Data Transmission (HSDT)

The burst of the High-Speed Data Transmission (HSDT) can consist of one data packet or several data packets. These

data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.
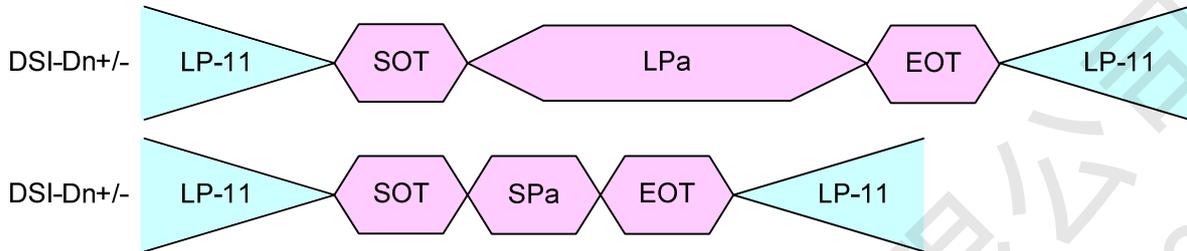
Figure 33 Single Packet in High-Speed Data Transmission with EoT packet disabled
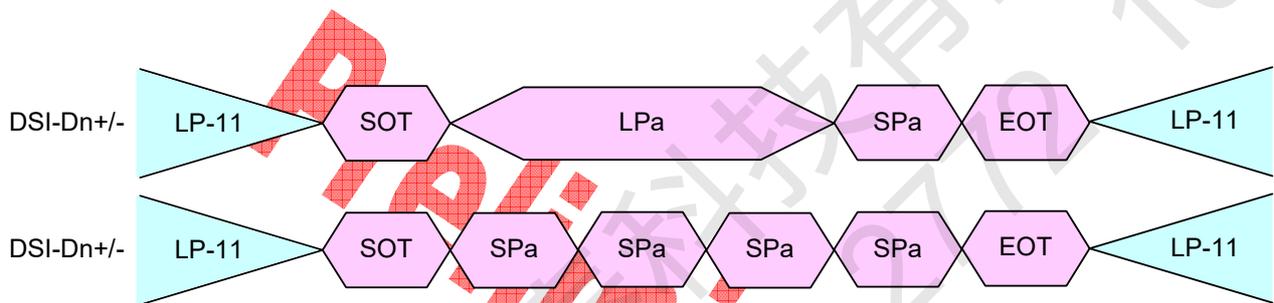
Figure 34 Multiple Packets in High-Speed Data Transmission with EoT packet disabled
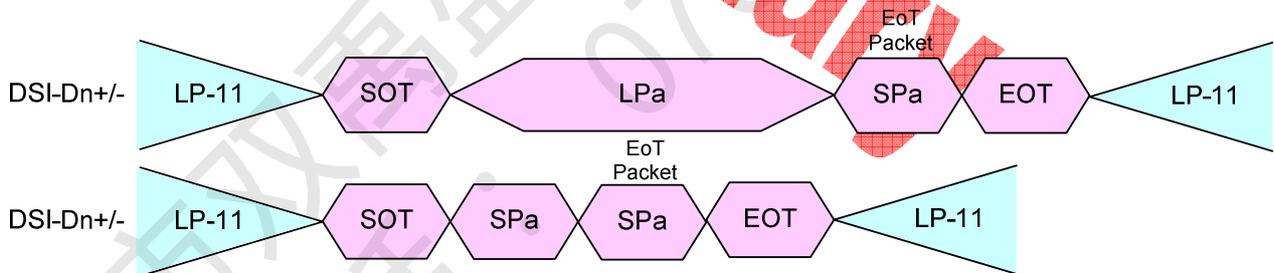
Figure 35 Single Packet in High-Speed Data Transmission with EoT packet enable
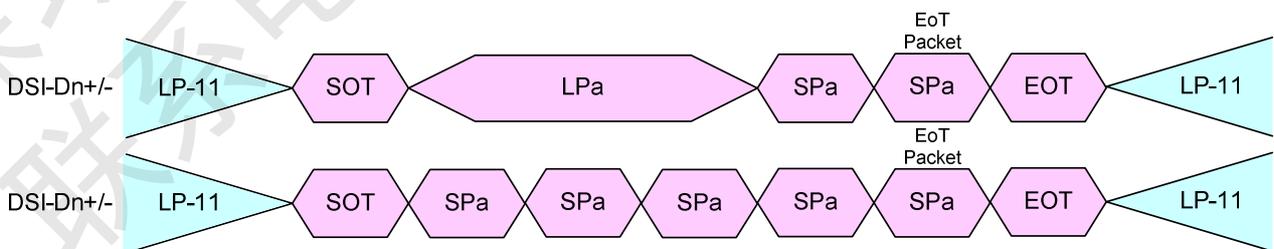
Figure 36 Multiple Packets in High-Speed Data Transmission with EoT packet enable

Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low-Power Mode, Data lanes are'1's (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

5.4.2.2.3.4   Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module is using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.
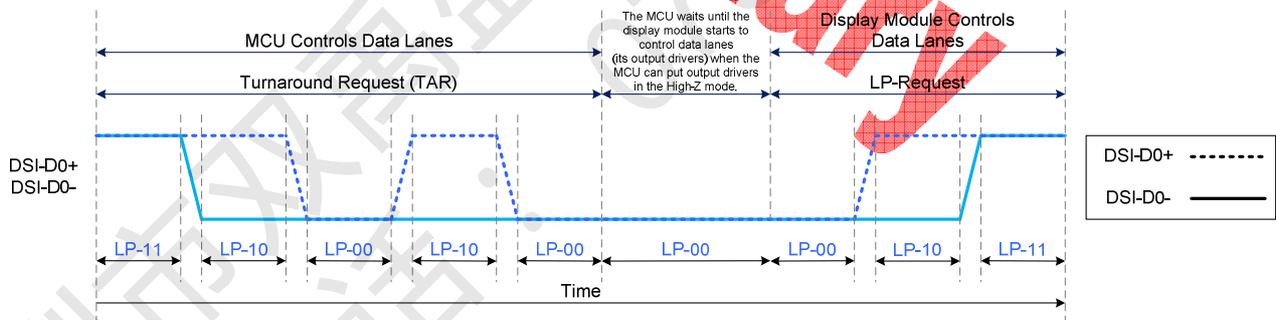
Figure 37 Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

5.4.2.3 Packer Level Communication

5.4.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low-Power Data

Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

• Short Packet (SPa): 4 bytes

• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).
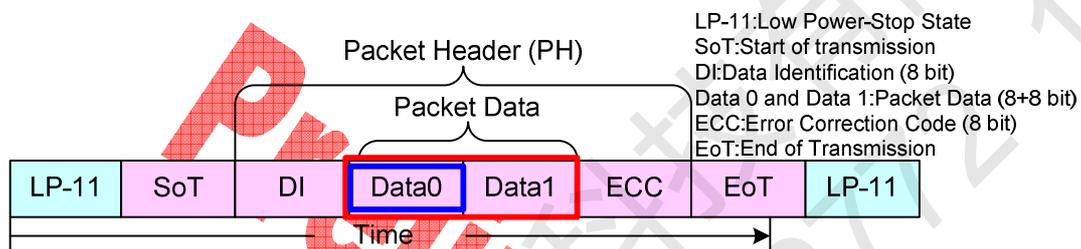
Figure 38 Short Packet (SPa) Structure
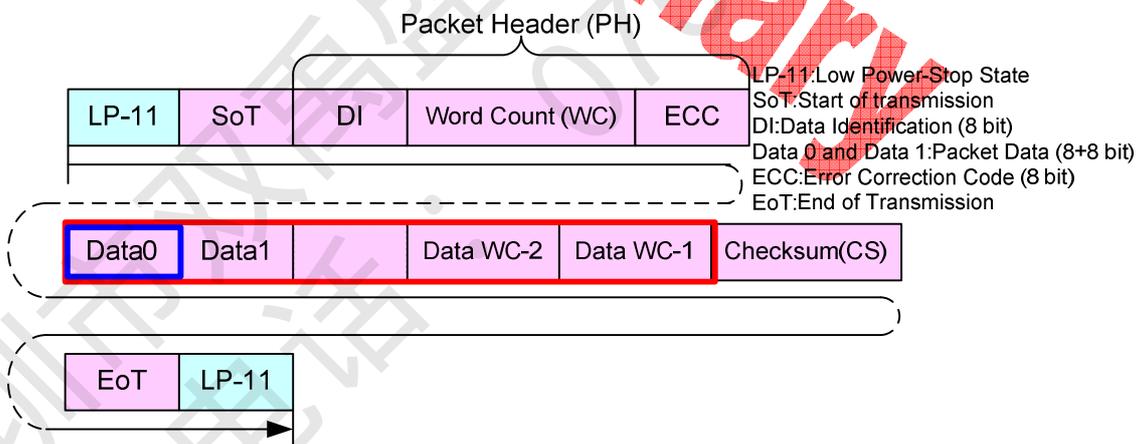
Figure 39 Long Packet (LPa) Structure

Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11,

SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple

packet format e.g.

* LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11

* LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11

* LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.4.2.3.1.1   Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and

the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

DI								WC (LS Byte)								WC (MS Byte)								ECC							
29 hex								01 hex								00 hex								06 hex							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time ⟶
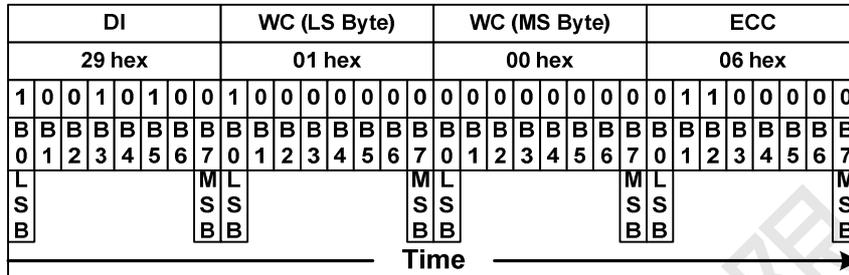
Figure 40 Bit Order of Byte on Packets

5.4.2.3.1.2   Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the

information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC)

consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

WC (LS Byte)								WC (MS Byte)							
01 hex								00 hex							
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB

Time ⟶
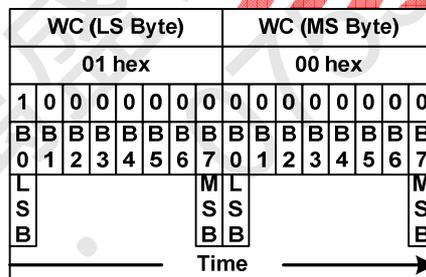
Figure 41 Byte Order of the Multiple Byte on Packets

5.4.2.3.1.3   Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short

Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and Data 1

• 4th byte: Error Correction Code (ECC)
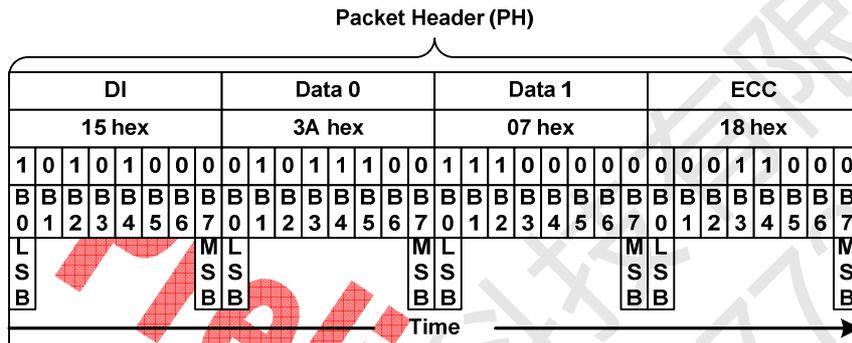
Figure 42 Packet Header (PH) on the Short Packet(SPa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)
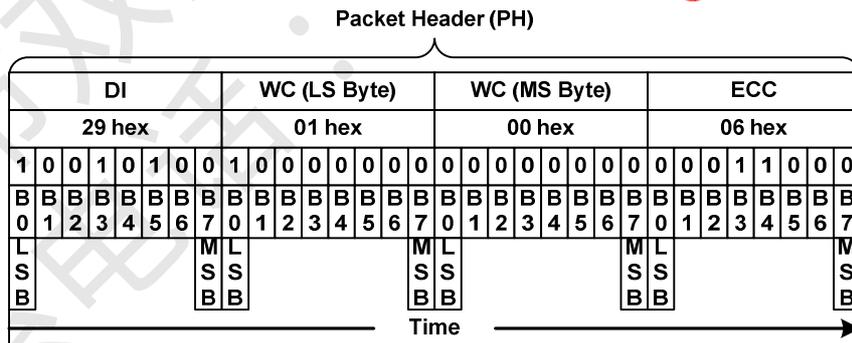
Figure 43 Packet Header (PH) on the Long Packet (LPa)

● **Data Identification (DI)**

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 44 Data Identification (DI) Structure

Figure 45 Data Identification (DI) on the Packet Header(PH)

● **Virtual Channel (VC)**

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.
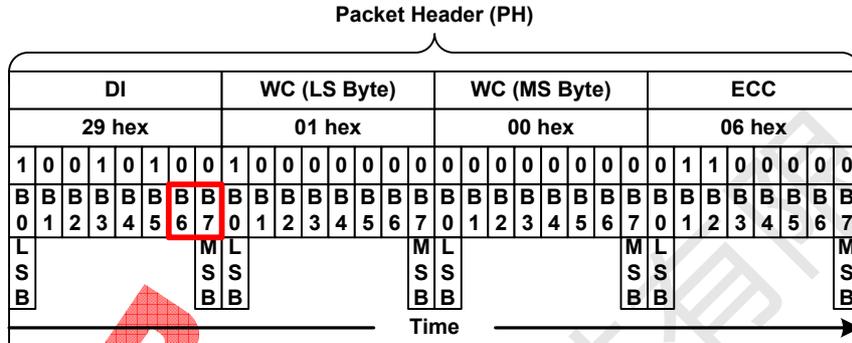
Packet Header (PH)

Figure 46 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

• The MCU is using the virtual channel 0 when it sends packets to this display module

• This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.
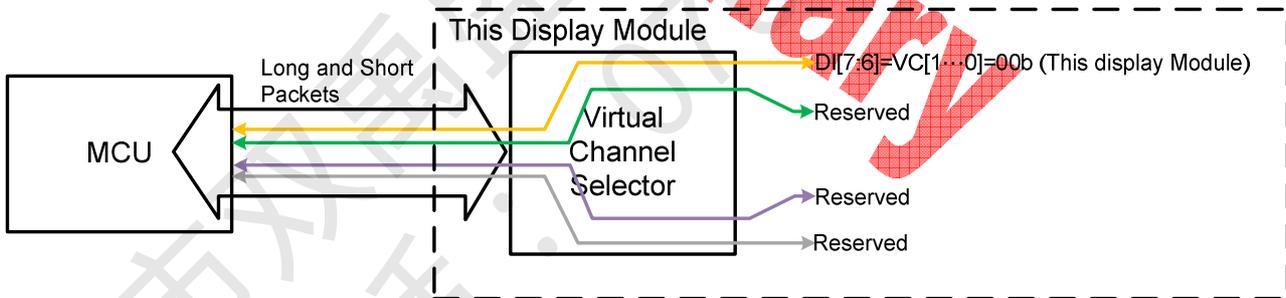
Figure 47 Virtual Channel (VC) Configuration

● **Data Type (DT)**

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a

packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.
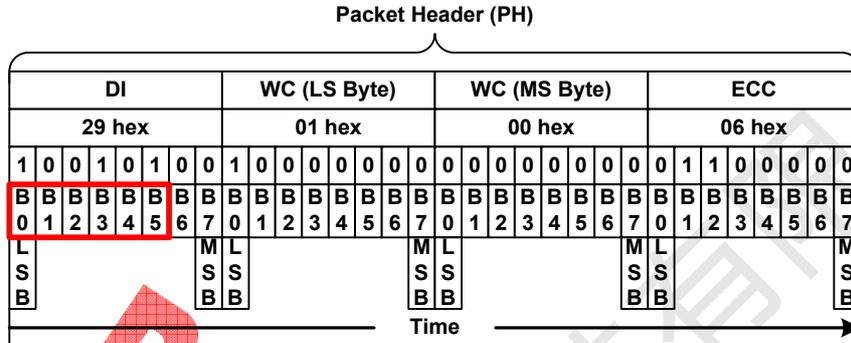
Figure 48 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type Hex	Data Type Binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
hh22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

Data Type (DT) from MCU to the Display Module (or Other Devices)

Data Type Hex	B5	B4	B3	B2	B1	B0	Description	Packet	Abbreviation
							From the Display Module (or Other Devices) to the MCU		
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or " Data Type (DT) from the Display Module (or Other Devices) to the MCU".

● **Packet Data (PD) on the Short Packet (SPa)**

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)
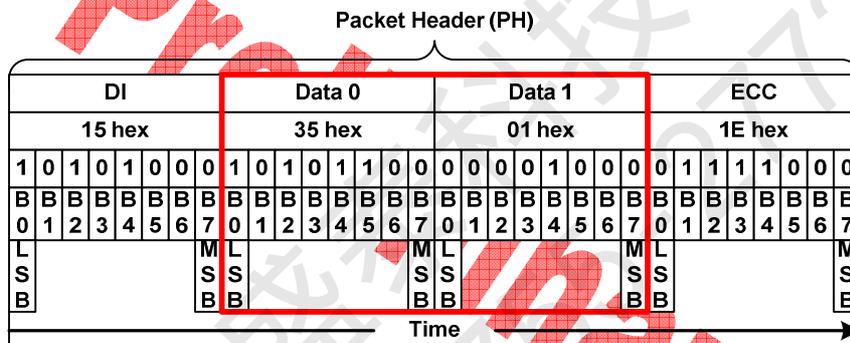
Figure 49 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)
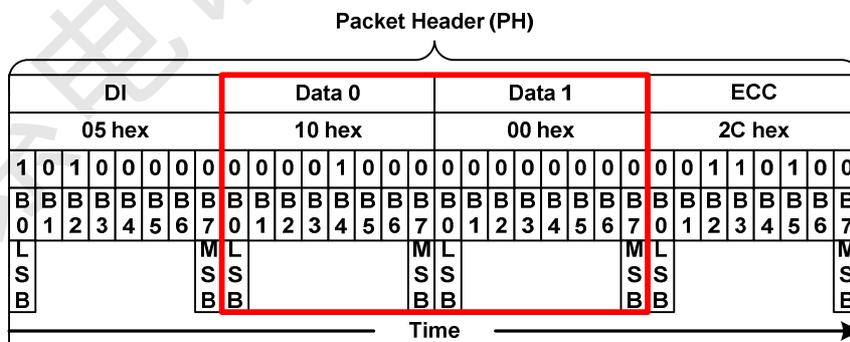
Figure 50 Packet Data (PD) for Short Packet (SPa), 1 Bytes Information

● **Word Count (WC) on the Long Packet (LPa)**

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has

indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after

Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most

Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

Figure 51 Word Count (WC) on the Long Packet (LPa)

LP-11:Low Power-Stop State
SoT:Start of transmission
DI:Data Identification (8 bit)
Data 0 and Data 1:Packet Data (8+8 bit)
ECC:Error Correction Code (8 bit)
EoT:End of Transmission

Figure 52 Packet Data (PD) on the Short Packet (SPa)

Figure 53 Packet Data (PD) on the Long Packet (LPa)

● **Error Correction Code (ECC)**

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field"

• Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

Packet Header (PH)

DI	Data 0	Data 1	ECC
05 hex	10 hex	00 hex	2C hex

1 0 1 0 0 0 0 0	0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0	0 0 1 1 0 1 0 0
D0 D1 D2 D3 D4 D5 D6 D7	D8 D9 D10 D11 D12 D13 D14 D15	D16 D17 D18 D19 D20 D21 D22 D23	P0 P1 P2 P3 P4 P5 P6 P7
B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7
LSB … MSB	LSB … MSB	LSB … MSB	LSB … MSB

Time →
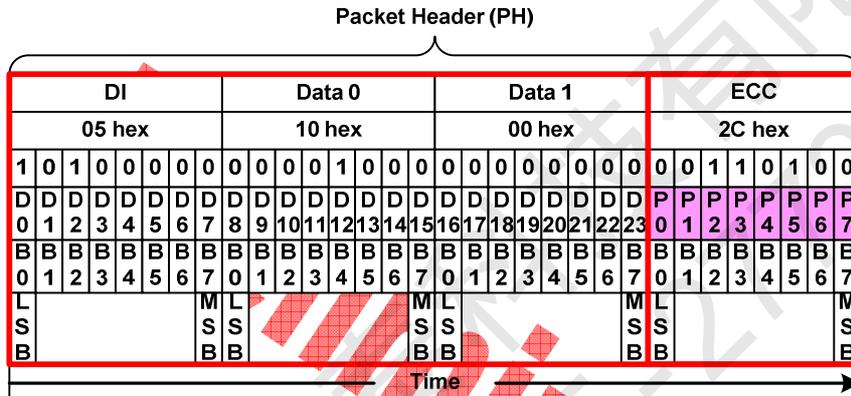
Figure 54 D[23..0] and P[7…0] on the Short Packet (SPa)

Packet Header (PH)

DI	WC (LS Byte)	WC (MS Byte)	ECC
29 hex	01 hex	00 hex	06 hex

1 0 0 1 0 1 0 0	1 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0 1 1 0 0 0 0 0
D0 D1 D2 D3 D4 D5 D6 D7	D8 D9 D10 D11 D12 D13 D14 D15	D16 D17 D18 D19 D20 D21 D22 D23	P0 P1 P2 P3 P4 P5 P6 P7
B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7	B0 B1 B2 B3 B4 B5 B6 B7
LSB … MSB	LSB … MSB	LSB … MSB	LSB … MSB

Time →
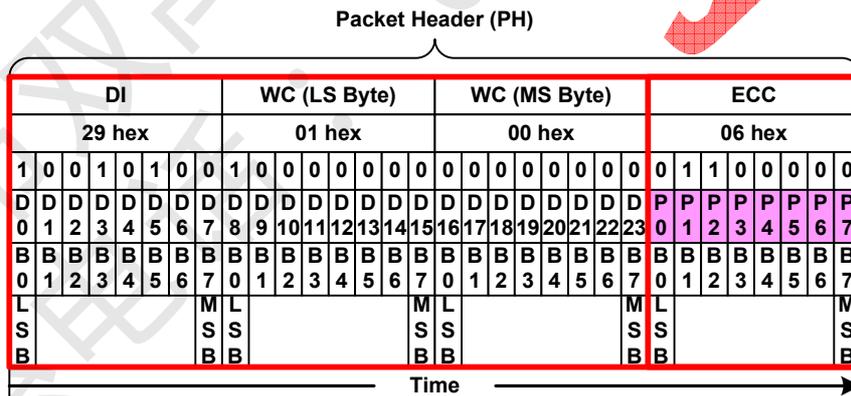
Figure 55 D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function

(Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this

implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error

Correction Code (ECC).

Figure 56 XOR Functionality on the Short Packet (SPa)

Packet Header (PH)

Figure 57 XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0].

The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.
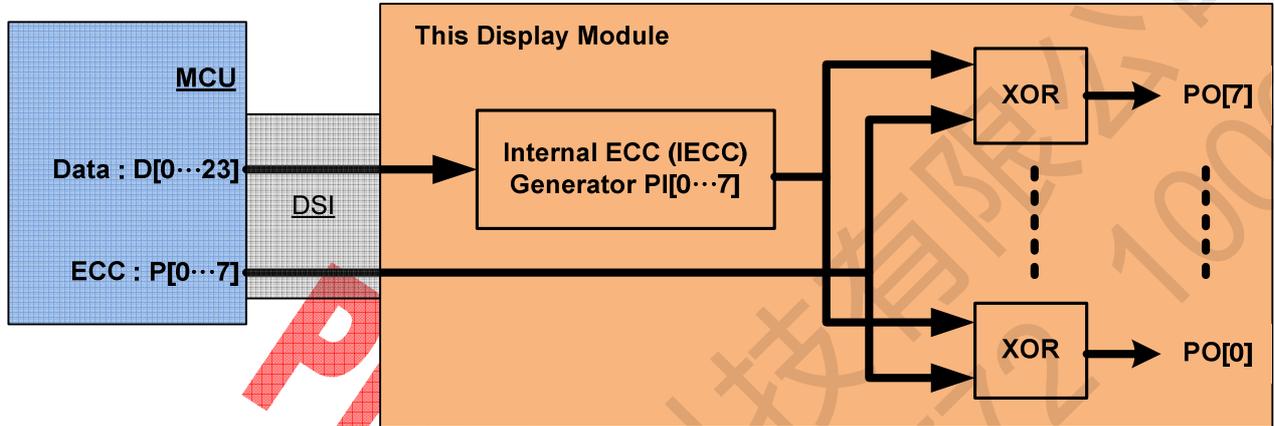
Figure 58 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 0 0h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h=>No Error
	L S B					M S B			

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch=> Error
	L S B					M S B			

Internal XOR Calculation between ECC and IECC Values- Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

5.4.2.3.1.4 Packet Date (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter "Word Count (WC) on the Long Packet (LPa)".

5.4.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X16+X12+X5+X0$ as it is illustrated below.
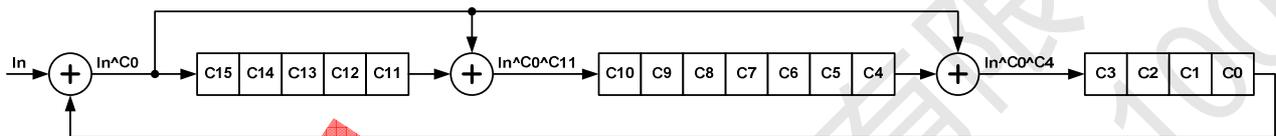
Figure 59 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

Step	In	In^C0	C15	C14	C13	C12	C11	In^C0^C11	C10	C9	C8	C7	C6	C5	C4	In^C0^C4	C3	C2	C1	C0
0	1(LSB)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1
5	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
6	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0
7	0(MSB)	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
8	X	X	0	0	0	1	1	X	1	1	0	0	0	0	0	X	1	1	1	0
CRC Result:			0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0
			MSB																	LSB

Figure 60 CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is Illustrated below.

Packet Header (PH)

DI	WC (LS Byte)	WC (MS Byte)	ECC
39 hex	01 hex	00 hex	15 hex

1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Packet Data (PD) | **Packet Footer (PF)**

Data 0	CRC(LS Byte)	CRC(MS Byte)
01 hex	0E hex	1E hex

1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time →

Figure 61 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.4.2.3.2 Packet Transmissions

5.4.2.3.2.1 Packet from the MCU to the Display Module

● **Display Command Set (DCS)**

Display Command Set (DCS), which is defined on chapter "Command Description", is used from the MCU to the display

module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD),which is included in

Short Packet (SPa) and Long Packet (LPa) as these are illustrated below.
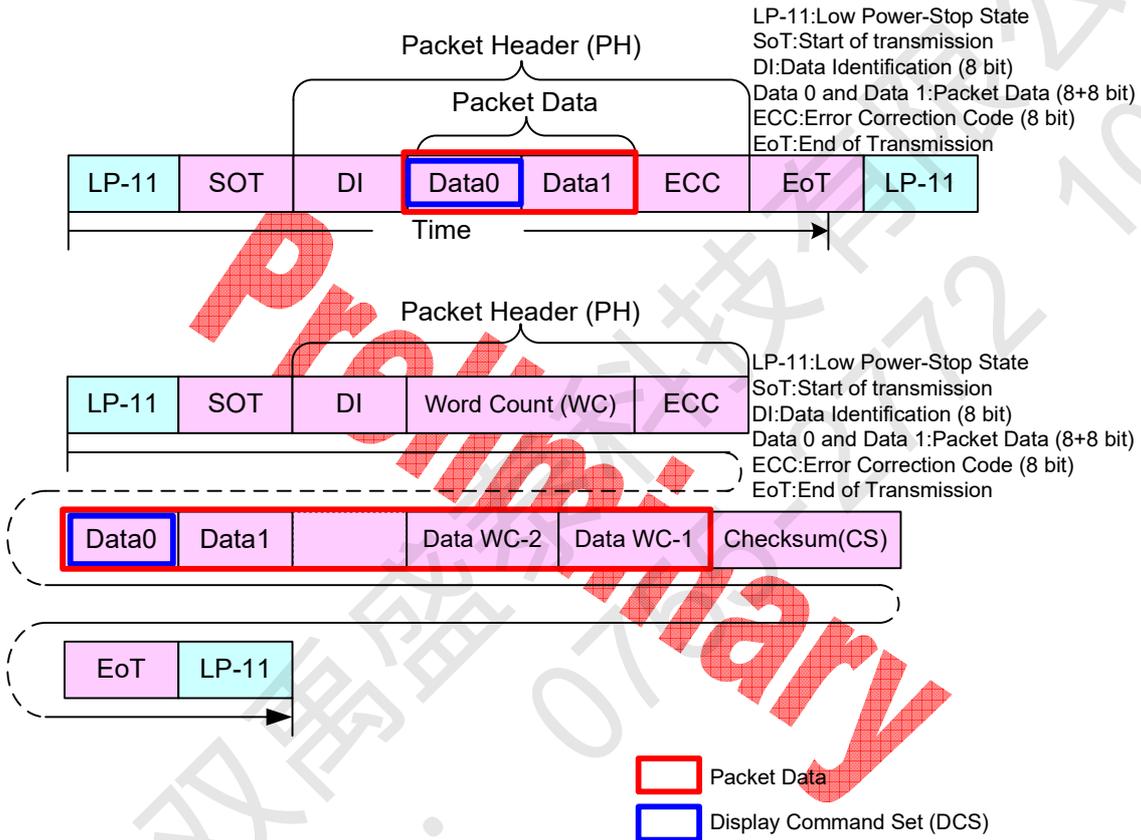
Figure 62 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

5.4.2.3.2.2 Packet from the Display Module to the MCU

● **Used Packet Types**

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report.

The used packet type is defined on Data Type (DT).

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.
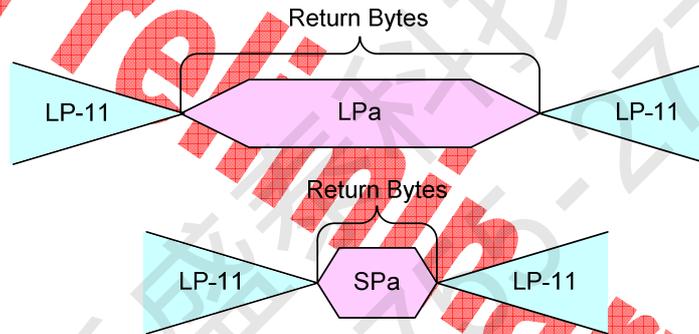
Figure 63 Return Bytes on Signal Packet

Data Type Hex	B 5	B 4	B 3	B 2	B 1	B 0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge and Error Report	Short	AwER
11h	0	1	0	0	0	1	Generic Short READ Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Short READ Response,2 bytes returned	Short	GENRR2-S
1Ah	0	1	1	0	1	0	Generic Long READ Response	Short	GENRR-L
1Ch	0	1	1	1	0	0	DCS Long READ Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Short READ Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Short READ Response, 2 bytes returned	Short	DCSRR2_S

From the Display Module (or Other Devices) to the MCU

Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet: Acknowledge with Error Report) to the MCU when the display module has received a read command. These return packets are illustrated for reference purpose below.
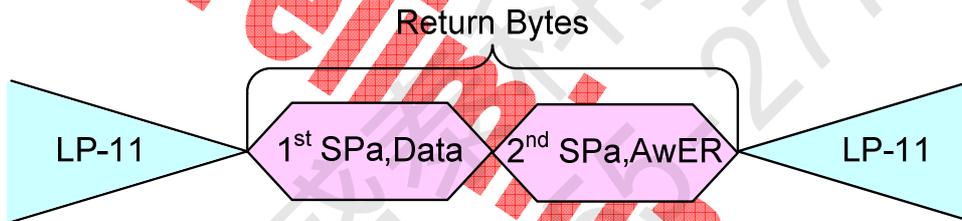
Figure 64 Exception When Return Bytes on Several Packet

Note:

1. AwER=Acknowledge with Error Report

● **Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)**

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Bit	Description	Sitronix LCD Driver Implementation
0	SoT Error	NO
1	SoT Sync Error	NO
2	EoT Sync Error	NO
3	Escape Mode Entry Command Error	YES
4	Low-Power Transmit Sync Error	YES
5	Any Protocol Timer Time-Out	NO
6	False Control Error	YES
7	Contention is Detected on the Display Module	NO
8	ECC Error, single-bit (detected and corrected)	YES
9	ECC Error, multi-bit (detected, not corrected)	YES
10	Set to "0" internally (Only for Long Packet (LP))	YES
11	DSI Data Type (DT) Not Recognized	YES
12	DSI Virtual Channel (VC) ID Invalid	YES
13	Invalid Transmission Length	NO
14	Reserved, Set to '0' internally	NO
15	DSI Protocol Violation	NO

Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Note

AwER will return1-bit zero if the item is no implementation.

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

    Virtual Channel (VC, DI[7…6]): 00b

    Data Type (DT, DI[5…0]): 00 0010b

• Packet Data (PD):

    Bit 8: ECC Error, single-bit (detected and corrected)

    AwER: 0100h

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.
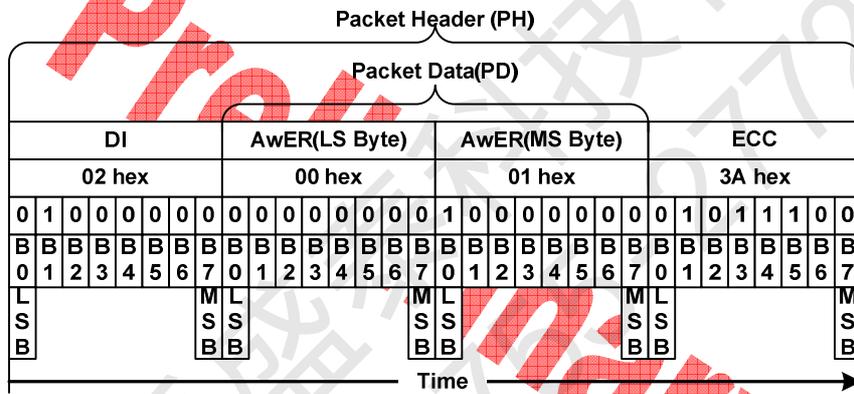
Figure 65 Acknowledge with Error Report (AwER)-Example

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.
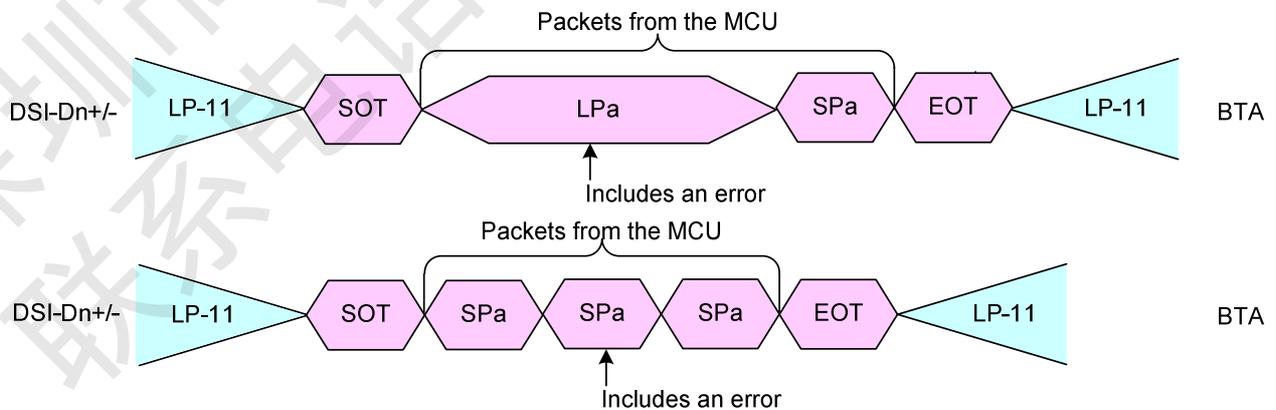
Figure 66 Error Packet

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check "Read Number of the Errors on DSI (05h)" command.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h after the MCU has read the RDNUMED register from the display module.

5.5 Digital Gamma

Digital gamma correct makes three sub-pixel (Red, Green, Blue) gamma curve by using one analog gamma curve.

By setting the digital gamma correction registers we can make three equivalent gamma curve Vgamma_total_r,

Vgamma_total_g, Vgamma_total_b as desired.
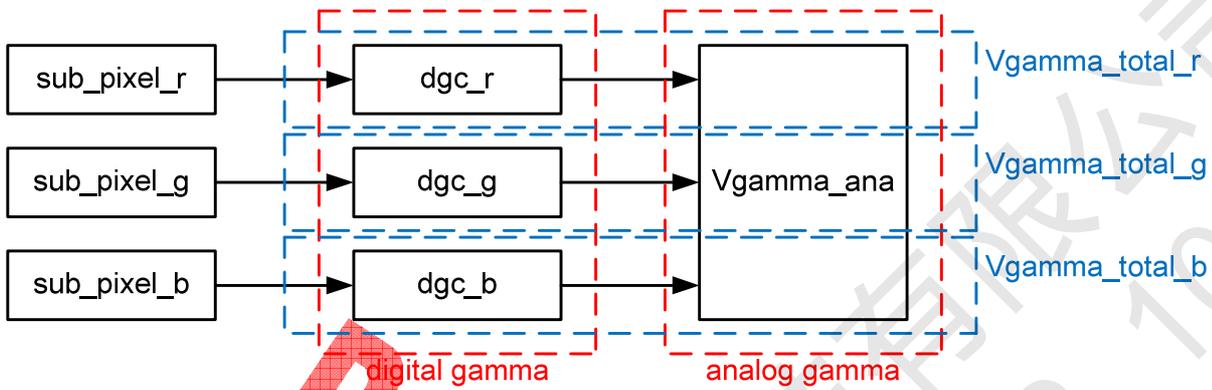
5.6 Gamma Correction Function

ST7123 incorporates the gamma correction function to display 16,777,216 colors for the LCD panel. There is a analog gamma correction is performed with 2 registers to set both positive and negative polarity voltage for gamma curve.

5.6.1 Gamma Correction Registers

The all of grayscale reference levels are shown blow.

Register Groups	Gamma Polarity		Description
	Positive	**Negative**	
Grayscale adjustment	VGMP0[9:0]	VGMN0[9:0]	1023-to-1 selector (voltage level of R grayscale 0)
	VGMP1[9:0]	VGMN1[9:0]	1023-to-1 selector (voltage level of R grayscale 1)
	VGMP2[9:0]	VGMN2[9:0]	1023-to-1 selector (voltage level of R grayscale 2)
	VGMP3[9:0]	VGMN3[9:0]	1023-to-1 selector (voltage level of R grayscale 4)
	VGMP4[9:0]	VGMN4[9:0]	1023-to-1 selector (voltage level of R grayscale 8)
	VGMP5[5:0]	VGMN5[5:0]	1023-to-1 selector (voltage level of R grayscale 12)
	VGMP6[9:0]	VGMN6[9:0]	1023-to-1 selector (voltage level of R grayscale 16)
	VGMP7[5:0]	VGMN7[5:0]	1023-to-1 selector (voltage level of R grayscale 24)
	VGMP8[9:0]	VGMN8[9:0]	1023-to-1 selector (voltage level of R grayscale 32)
	VGMP9[5:0]	VGMN9[5:0]	1023-to-1 selector (voltage level of R grayscale 48)
	VGMP10[9:0]	VGMN10[9:0]	1023-to-1 selector (voltage level of R grayscale 64)
	VGMP11[3:0]	VGMN11[3:0]	1023-to-1 selector (voltage level of R grayscale 80)
	VGMP12[9:0]	VGMN12[9:0]	1023-to-1 selector (voltage level of R grayscale 96)
	VGMP13[3:0]	VGMN13[3:0]	1023-to-1 selector (voltage level of R grayscale 112)
	VGMP14[9:0]	VGMN14[9:0]	1023-to-1 selector (voltage level of R grayscale 128)
	VGMP15[3:0]	VGMN15[3:0]	1023-to-1 selector (voltage level of R grayscale 144)
	VGMP16[9:0]	VGMN16[9:0]	1023-to-1 selector (voltage level of R grayscale 160)
	VGMP17[3:0]	VGMN17[3:0]	1023-to-1 selector (voltage level of R grayscale 176)
	VGMP18[9:0]	VGMN18[9:0]	1023-to-1 selector (voltage level of R grayscale 192)
	VGMP19[3:0]	VGMN19[3:0]	1023-to-1 selector (voltage level of R grayscale 208)
	VGMP20[9:0]	VGMN20[9:0]	1023-to-1 selector (voltage level of R grayscale 224)
	VGMP21[3:0]	VGMN21[3:0]	1023-to-1 selector (voltage level of R grayscale 232)
	VGMP22[9:0]	VGMN22[9:0]	1023-to-1 selector (voltage level of R grayscale 240)
	VGMP23[3:0]	VGMN23[3:0]	1023-to-1 selector (voltage level of R grayscale 244)
	VGMP24[9:0]	VGMN24[9:0]	1023-to-1 selector (voltage level of R grayscale 248)
	VGMP25[3:0]	VGMN25[3:0]	1023-to-1 selector (voltage level of R grayscale 250)

	VGMP26[9:0]	VGMN26[9:0]	1023-to-1 selector (voltage level of R grayscale 252)
	VGMP27[9:0]	VGMN27[9:0]	1023-to-1 selector (voltage level of R grayscale 254)
	VGMP28[9:0]	VGMN28[9:0]	1023-to-1 selector (voltage level of R grayscale 255)

5.6.2   Gamma function architecture
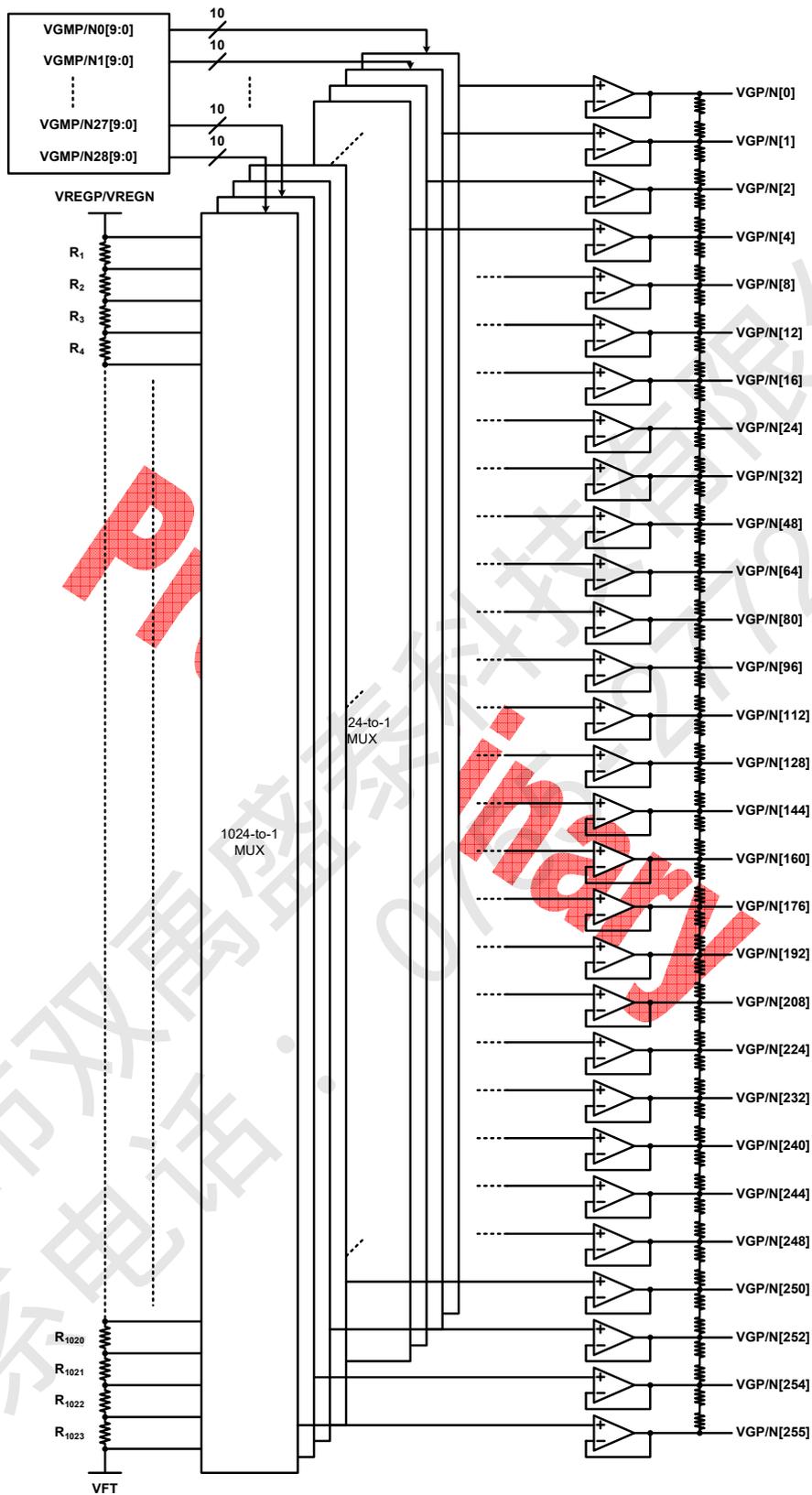
Figure 67 positive and Negative grayscale voltage generation

Note1. VFT: Feed through voltage

Note2.VREGP: VFT+VGPAMP=feed through voltage + positive gamma amplitude.

Note3.VREGN: VFT+VGNAMP=feed through voltage + negative gamma amplitude.

5.6.3 Grayscale voltage formula

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VGP/N0	V64	VGP/N10
V1	VGP/N1	V65	15/16 * VGP/N10 + 1/16 * VGP/N11
V2	VGP/N2	V66	14/16 * VGP/N10 + 2/16 * VGP/N11
V3	1/2 * VGP/N2 + 1/2* VGP/N3	V67	13/16 * VGP/N10 + 3/16 * VGP/N11
V4	VGP/N3	V68	12/16 * VGP/N10 + 4/16 * VGP/N11
V5	3/4 * VGP/N3 + 1/4* VGP/N4	V69	11/16 * VGP/N10 + 5/16 * VGP/N11
V6	2/4 * VGP/N3 + 2/4* VGP/N4	V70	10/16 * VGP/N10 + 6/16 * VGP/N11
V7	1/4 * VGP/N3 + 3/4* VGP/N4	V71	9/16 * VGP/N10 + 7/16 * VGP/N11
V8	VGP/N4	V72	8/16 * VGP/N10 + 8/16 * VGP/N11
V9	3/4 * VGP/N4 + 1/4* VGP/N5	V73	7/16 * VGP/N10 + 9/16 * VGP/N11
V10	2/4 * VGP/N4 + 2/4* VGP/N5	V74	6/16 * VGP/N10 + 10/16 * VGP/N11
V11	1/4 * VGP/N4 + 3/4* VGP/N5	V75	5/16 * VGP/N10 + 11/16 * VGP/N11
V12	VGP/N5	V76	4/16 * VGP/N10 + 12/16 * VGP/N11
V13	3/4 * VGP/N5 + 1/4* VGP/N6	V77	3/16 * VGP/N10 + 13/16 * VGP/N11
V14	2/4 * VGP/N5 + 2/4* VGP/N6	V78	2/16 * VGP/N10 + 14/16 * VGP/N11
V15	1/4 * VGP/N5 + 3/4* VGP/N6	V79	1/16 * VGP/N10 + 15/16 * VGP/N11
V16	VGP/N6	V80	VGP/N11
V17	7/8 * VGP/N6 + 1/8 * VGP/N7	V81	15/16 * VGP/N11 + 1/16 * VGP/N12
V18	6/8 * VGP/N6 + 2/8 * VGP/N7	V82	14/16 * VGP/N11 + 2/16 * VGP/N12
V19	5/8 * VGP/N6 + 3/8 * VGP/N7	V83	13/16 * VGP/N11 + 3/16 * VGP/N12
V20	4/8 * VGP/N6 + 4/8 * VGP/N7	V84	12/16 * VGP/N11 + 4/16 * VGP/N12
V21	3/8 * VGP/N6 + 5/8 * VGP/N7	V85	11/16 * VGP/N11 + 5/16 * VGP/N12
V22	2/8 * VGP/N6 + 6/8 * VGP/N7	V86	10/16 * VGP/N11 + 6/16 * VGP/N12
V23	1/8 * VGP/N6 + 7/8 * VGP/N7	V87	9/16 * VGP/N11 + 7/16 * VGP/N12
V24	VGP/N7	V88	8/16 * VGP/N11 + 8/16 * VGP/N12
V25	7/8 * VGP/N7 + 1/8 * VGP/N8	V89	7/16 * VGP/N11 + 9/16 * VGP/N12
V26	6/8 * VGP/N7 + 2/8 * VGP/N8	V90	6/16 * VGP/N11 + 10/16 * VGP/N12
V27	5/8 * VGP/N7 + 3/8 * VGP/N8	V91	5/16 * VGP/N11 + 11/16 * VGP/N12

V28	4/8 * VGP/N7 + 4/8 * VGP/N8	V92	4/16 * VGP/N11 + 12/16 * VGP/N12
V29	3/8 * VGP/N7 + 5/8 * VGP/N8	V93	3/16 * VGP/N11 + 13/16 * VGP/N12
V30	2/8 * VGP/N7 + 6/8 * VGP/N8	V94	2/16 * VGP/N11 + 14/16 * VGP/N12
V31	1/8 * VGP/N7 + 7/8 * VGP/N8	V95	1/16 * VGP/N11 + 15/16 * VGP/N12
V32	VGP/N8	V96	VGP/N12
V33	15/16 * VGP/N8 + 1/16 * VGP/N9	V97	15/16 * VGP/N12 + 1/16 * VGP/N13
V34	14/16 * VGP/N8 + 2/16 * VGP/N9	V98	14/16 * VGP/N12 + 2/16 * VGP/N13
V35	13/16 * VGP/N8 + 3/16 * VGP/N9	V99	13/16 * VGP/N12 + 3/16 * VGP/N13
V36	12/16 * VGP/N8 + 4/16 * VGP/N9	V100	12/16 * VGP/N12 + 4/16 * VGP/N13
V37	11/16 * VGP/N8 + 5/16 * VGP/N9	V101	11/16 * VGP/N12 + 5/16 * VGP/N13
V38	10/16 * VGP/N8 + 6/16 * VGP/N9	V102	10/16 * VGP/N12 + 6/16 * VGP/N13
V39	9/16 * VGP/N8 + 7/16 * VGP/N9	V103	9/16 * VGP/N12 + 7/16 * VGP/N13
V40	8/16 * VGP/N8 + 8/16 * VGP/N9	V104	8/16 * VGP/N12 + 8/16 * VGP/N13
V41	7/16 * VGP/N8 + 9/16 * VGP/N9	V105	7/16 * VGP/N12 + 9/16 * VGP/N13
V42	6/16 * VGP/N8 + 10/16 * VGP/N9	V106	6/16 * VGP/N12 + 10/16 * VGP/N13
V43	5/16 * VGP/N8 + 11/16 * VGP/N9	V107	5/16 * VGP/N12 + 11/16 * VGP/N13
V44	4/16 * VGP/N8 + 12/16 * VGP/N9	V108	4/16 * VGP/N12 + 12/16 * VGP/N13
V45	3/16 * VGP/N8 + 13/16 * VGP/N9	V109	3/16 * VGP/N12 + 13/16 * VGP/N13
V46	2/16 * VGP/N8 + 14/16 * VGP/N9	V110	2/16 * VGP/N12 + 14/16 * VGP/N13
V47	1/16 * VGP/N8 + 15/16 * VGP/N9	V111	1/16 * VGP/N12 + 15/16 * VGP/N13
V48	VGP/N9	V112	VGP/N13
V49	15/16 * VGP/N9 + 1/16 * VGP/N10	V113	15/16 * VGP/N13 + 1/16 * VGP/N14
V50	14/16 * VGP/N9 + 2/16 * VGP/N10	V114	14/16 * VGP/N13 + 2/16 * VGP/N14
V51	13/16 * VGP/N9 + 3/16 * VGP/N10	V115	13/16 * VGP/N13 + 3/16 * VGP/N14
V52	12/16 * VGP/N9 + 4/16 * VGP/N10	V116	12/16 * VGP/N13 + 4/16 * VGP/N14
V53	11/16 * VGP/N9 + 5/16 * VGP/N10	V117	11/16 * VGP/N13 + 5/16 * VGP/N14
V54	10/16 * VGP/N9 + 6/16 * VGP/N10	V118	10/16 * VGP/N13 + 6/16 * VGP/N14
V55	9/16 * VGP/N9 + 7/16 * VGP/N10	V119	9/16 * VGP/N13 + 7/16 * VGP/N14
V56	8/16 * VGP/N9 + 8/16 * VGP/N10	V120	8/16 * VGP/N13 + 8/16 * VGP/N14
V57	7/16 * VGP/N9 + 9/16 * VGP/N10	V121	7/16 * VGP/N13 + 9/16 * VGP/N14
V58	6/16 * VGP/N9 + 10/16 * VGP/N10	V122	6/16 * VGP/N13 + 10/16 * VGP/N14
V59	5/16 * VGP/N9 + 11/16 * VGP/N10	V123	5/16 * VGP/N13 + 11/16 * VGP/N14
V60	4/16 * VGP/N9 + 12/16 * VGP/N10	V124	4/16 * VGP/N13 + 12/16 * VGP/N14
V61	3/16 * VGP/N9 + 13/16 * VGP/N10	V125	3/16 * VGP/N13 + 13/16 * VGP/N14
V62	2/16 * VGP/N9 + 14/16 * VGP/N10	V126	2/16 * VGP/N13 + 14/16 * VGP/N14
V63	1/16 * VGP/N9 + 15/16 * VGP/N10	V127	1/16 * VGP/N13 + 15/16 * VGP/N14

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V128	VGP/N14	V192	VGP/N18
V129	15/16 * VGP/N14 + 1/16 * VGP/N15	V193	15/16 * VGP/N18 + 1/16 * VGP/N19
V130	14/16 * VGP/N14 + 2/16 * VGP/N15	V194	14/16 * VGP/N18 + 2/16 * VGP/N19
V131	13/16 * VGP/N14 + 3/16 * VGP/N15	V195	13/16 * VGP/N18 + 3/16 * VGP/N19
V132	12/16 * VGP/N14 + 4/16 * VGP/N15	V196	12/16 * VGP/N18 + 4/16 * VGP/N19
V133	11/16 * VGP/N14 + 5/16 * VGP/N15	V197	11/16 * VGP/N18 + 5/16 * VGP/N19
V134	10/16 * VGP/N14 + 6/16 * VGP/N15	V198	10/16 * VGP/N18 + 6/16 * VGP/N19
V135	9/16 * VGP/N14 + 7/16 * VGP/N15	V199	9/16 * VGP/N18 + 7/16 * VGP/N19
V136	8/16 * VGP/N14 + 8/16 * VGP/N15	V200	8/16 * VGP/N18 + 8/16 * VGP/N19
V137	7/16 * VGP/N14 + 9/16 * VGP/N15	V201	7/16 * VGP/N18 + 9/16 * VGP/N19
V138	6/16 * VGP/N14 + 10/16 * VGP/N15	V202	6/16 * VGP/N18 + 10/16 * VGP/N19
V139	5/16 * VGP/N14 + 11/16 * VGP/N15	V203	5/16 * VGP/N18 + 11/16 * VGP/N19
V140	4/16 * VGP/N14 + 12/16 * VGP/N15	V204	4/16 * VGP/N18 + 12/16 * VGP/N19
V141	3/16 * VGP/N14 + 13/16 * VGP/N15	V205	3/16 * VGP/N18 + 13/16 * VGP/N19
V142	2/16 * VGP/N14 + 14/16 * VGP/N15	V206	2/16 * VGP/N18 + 14/16 * VGP/N19
V143	1/16 * VGP/N14 + 15/16 * VGP/N15	V207	1/16 * VGP/N18 + 15/16 * VGP/N19
V144	VGP/N15	V208	VGP/N19
V145	15/16 * VGP/N15 + 1/16 * VGP/N16	V209	15/16 * VGP/N19 + 1/16 * VGP/N20
V146	14/16 * VGP/N15 + 2/16 * VGP/N16	V210	14/16 * VGP/N19 + 2/16 * VGP/N20
V147	13/16 * VGP/N15 + 3/16 * VGP/N16	V211	13/16 * VGP/N19 + 3/16 * VGP/N20
V148	12/16 * VGP/N15 + 4/16 * VGP/N16	V212	12/16 * VGP/N19 + 4/16 * VGP/N20
V149	11/16 * VGP/N15 + 5/16 * VGP/N16	V213	11/16 * VGP/N19 + 5/16 * VGP/N20
V150	10/16 * VGP/N15 + 6/16 * VGP/N16	V214	10/16 * VGP/N19 + 6/16 * VGP/N20
V151	9/16 * VGP/N15 + 7/16 * VGP/N16	V215	9/16 * VGP/N19 + 7/16 * VGP/N20
V152	8/16 * VGP/N15 + 8/16 * VGP/N16	V216	8/16 * VGP/N19 + 8/16 * VGP/N20
V153	7/16 * VGP/N15 + 9/16 * VGP/N16	V217	7/16 * VGP/N19 + 9/16 * VGP/N20
V154	6/16 * VGP/N15 + 10/16 * VGP/N16	V218	6/16 * VGP/N19 + 10/16 * VGP/N20
V155	5/16 * VGP/N15 + 11/16 * VGP/N16	V219	5/16 * VGP/N19 + 11/16 * VGP/N20
V156	4/16 * VGP/N15 + 12/16 * VGP/N16	V220	4/16 * VGP/N19 + 12/16 * VGP/N20
V157	3/16 * VGP/N15 + 13/16 * VGP/N16	V221	3/16 * VGP/N19 + 13/16 * VGP/N20
V158	2/16 * VGP/N15 + 14/16 * VGP/N16	V222	2/16 * VGP/N19 + 14/16 * VGP/N20
V159	1/16 * VGP/N15 + 15/16 * VGP/N16	V223	1/16 * VGP/N19 + 15/16 * VGP/N20
V160	VGP/N16	V224	VGP/N20
V161	15/16 * VGP/N16 + 1/16 * VGP/N17	V225	7/8 * VGP/N20 + 1/8 * VGP/N21

V162	14/16 * VGP/N16 + 2/16 * VGP/N17	V226	6/8 * VGP/N20 + 2/8 * VGP/N21
V163	13/16 * VGP/N16 + 3/16 * VGP/N17	V227	5/8 * VGP/N20 + 3/8 * VGP/N21
V164	12/16 * VGP/N16 + 4/16 * VGP/N17	V228	4/8 * VGP/N20 + 4/8 * VGP/N21
V165	11/16 * VGP/N16 + 5/16 * VGP/N17	V229	3/8 * VGP/N20 + 5/8 * VGP/N21
V166	10/16 * VGP/N16 + 6/16 * VGP/N17	V230	2/8 * VGP/N20 + 6/8 * VGP/N21
V167	9/16 * VGP/N16 + 7/16 * VGP/N17	V231	1/8 * VGP/N20 + 7/8 * VGP/N21
V168	8/16 * VGP/N16 + 8/16 * VGP/N17	V232	VGP/N21
V169	7/16 * VGP/N16 + 9/16 * VGP/N17	V233	7/8 * VGP/N21 + 1/8 * VGP/N22
V170	6/16 * VGP/N16 + 10/16 * VGP/N17	V234	6/8 * VGP/N21 + 2/8 * VGP/N22
V171	5/16 * VGP/N16 + 11/16 * VGP/N17	V235	5/8 * VGP/N21 + 3/8 * VGP/N22
V172	4/16 * VGP/N16 + 12/16 * VGP/N17	V236	4/8 * VGP/N21 + 4/8 * VGP/N22
V173	3/16 * VGP/N16 + 13/16 * VGP/N17	V237	3/8 * VGP/N21 + 5/8 * VGP/N22
V174	2/16 * VGP/N16 + 14/16 * VGP/N17	V238	2/8 * VGP/N21 + 6/8 * VGP/N22
V175	1/16 * VGP/N16 + 15/16 * VGP/N17	V239	1/8 * VGP/N21 + 7/8 * VGP/N22
V176	VGP/N17	V240	VGP/N22
V177	15/16 * VGP/N17 + 1/16 * VGP/N18	V241	3/4 * VGP/N22 + 1/4* VGP/N23
V178	14/16 * VGP/N17 + 2/16 * VGP/N18	V242	2/4 * VGP/N22 + 2/4* VGP/N23
V179	13/16 * VGP/N17 + 3/16 * VGP/N18	V243	1/4 * VGP/N22 + 3/4* VGP/N23
V180	12/16 * VGP/N17 + 4/16 * VGP/N18	V244	VGP/N23
V181	11/16 * VGP/N17 + 5/16 * VGP/N18	V245	3/4 * VGP/N23 + 1/4* VGP/N24
V182	10/16 * VGP/N17 + 6/16 * VGP/N18	V246	2/4 * VGP/N23 + 2/4* VGP/N24
V183	9/16 * VGP/N17 + 7/16 * VGP/N18	V247	1/4 * VGP/N23 + 3/4* VGP/N24
V184	8/16 * VGP/N17 + 8/16 * VGP/N18	V248	VGP/N24
V185	7/16 * VGP/N17 + 9/16 * VGP/N18	V249	1/2 * VGP/N24 + 1/2* VGP/N25
V186	6/16 * VGP/N17 + 10/16 * VGP/N18	V250	VGP/N25
V187	5/16 * VGP/N17 + 11/16 * VGP/N18	V251	1/2 * VGP/N25 + 1/2* VGP/N26
V188	4/16 * VGP/N17 + 12/16 * VGP/N18	V252	VGP/N26
V189	3/16 * VGP/N17 + 13/16 * VGP/N18	V253	1/2 * VGP/N26 + 1/2* VGP/N27
V190	2/16 * VGP/N17 + 14/16 * VGP/N18	V254	VGP/N27
V191	1/16 * VGP/N17 + 15/16 * VGP/N18	V255	VGP/N28

5.7 Reset function

The Reset function of ST7123 is triggered by RESX input. After reset function is triggered, the ST7123 is into a reset period, and the duration of this period must be at least 1ms. During this period, the ST7123 and its power circuit is initialized.

Initial State Of Output Pins

Output Pins Name	Initial State
S[720:1] (source output)	GND
VGH	GND
VGL	GND
VGHS	AVDD
VCOM	GND
SOUT[38:1](GIP signal)	GND

5.7.1 Reset Timing Diagram

ST7123 provides Power On Reset and HWRST pin (RESX) for IC initialization and exit Deep Standby Mode (DSTB). For exiting DSTB Mode, HWRST pin should be tied to high at least 10ms. The timing diagram is located at below.

5.7.1.1 Power On Reset & HWRST Reset
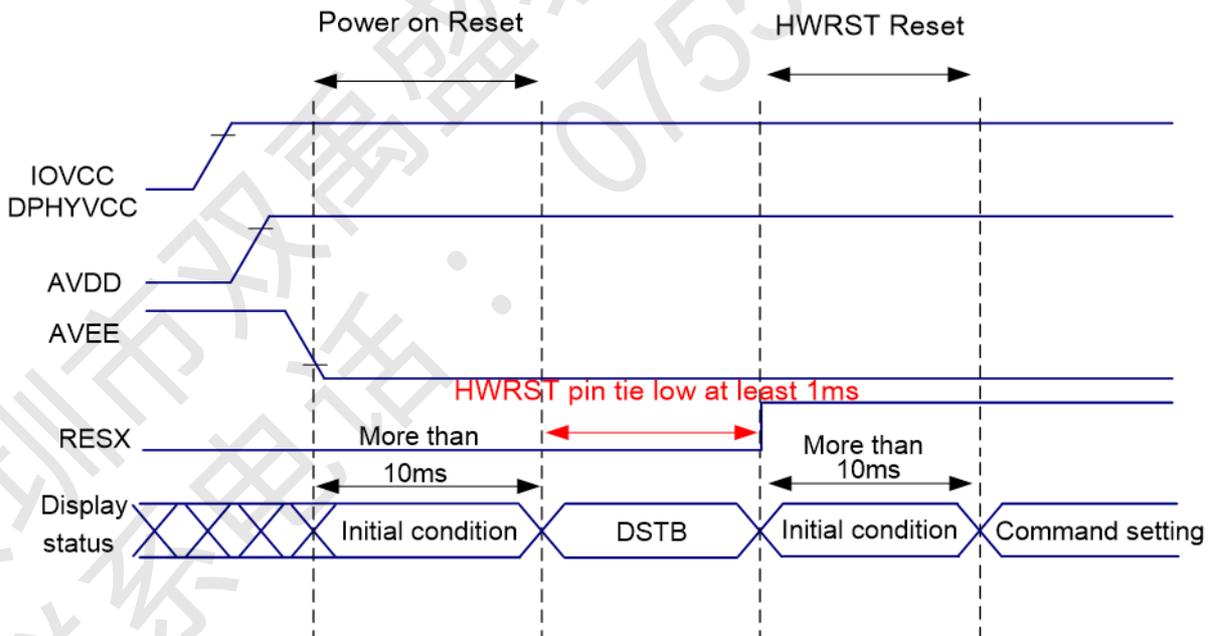
Figure 68 Power on Reset and HWRST reset

Note: RESX should be tied to high when exiting DSTB Mode.

5.8   Abnormal Power off Function

ST7123 provides Power Drop detection. If external power drops lower than circuit detection voltage, then the system will enter into Sleep In Mode.

5.8.1   Abnormal Power Off

Abnormal Power Off circuit can detect external voltage source IOVCC, AVDD, AVEE, if one of them is below detection voltage, then the system will be into Sleep In Mode. The following schematic is to show how the detection circuit produces abnormal signal.
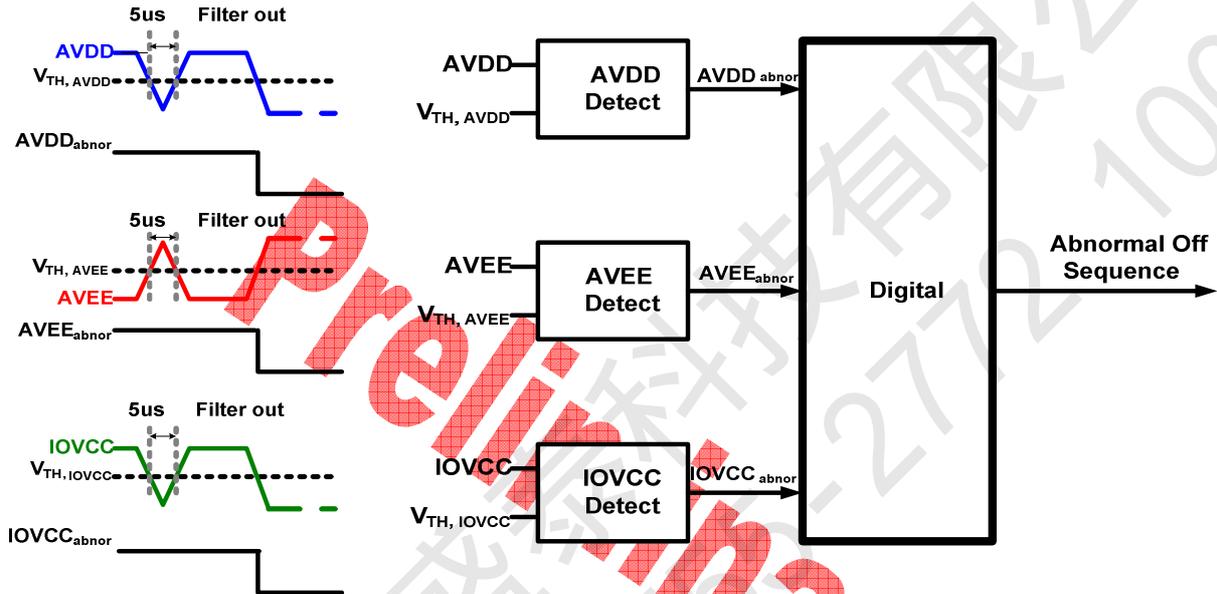
Figure 69 Abnormal Off Function Block Diagram
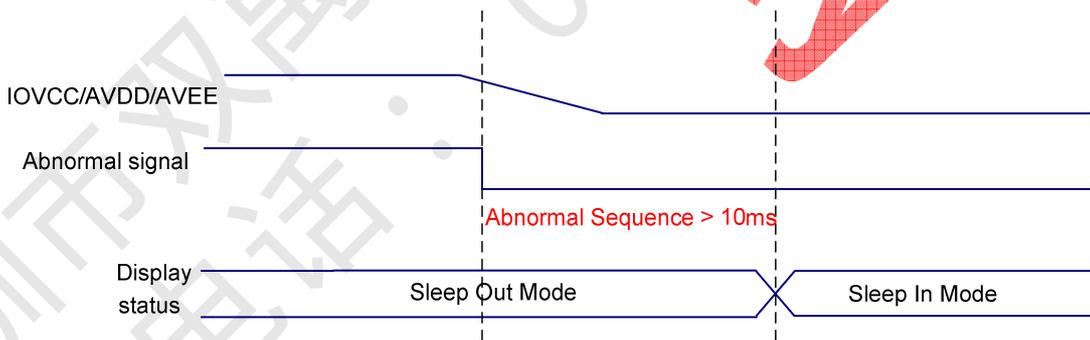
Figure 70 Abnormal Off Sequence Diagram

Note1: Abnormal function is working only in Sleep Out Mode

Note2: External power supply drop can't be so quickly, drop time must be longer than 100ms linearly (see AC characteristic).

5.9 Basic Operation Mode

The basic operation mode of ST7123 is illustrated below. When changing from one mode to another, make sure to follow

the sequence indicated in below figure.
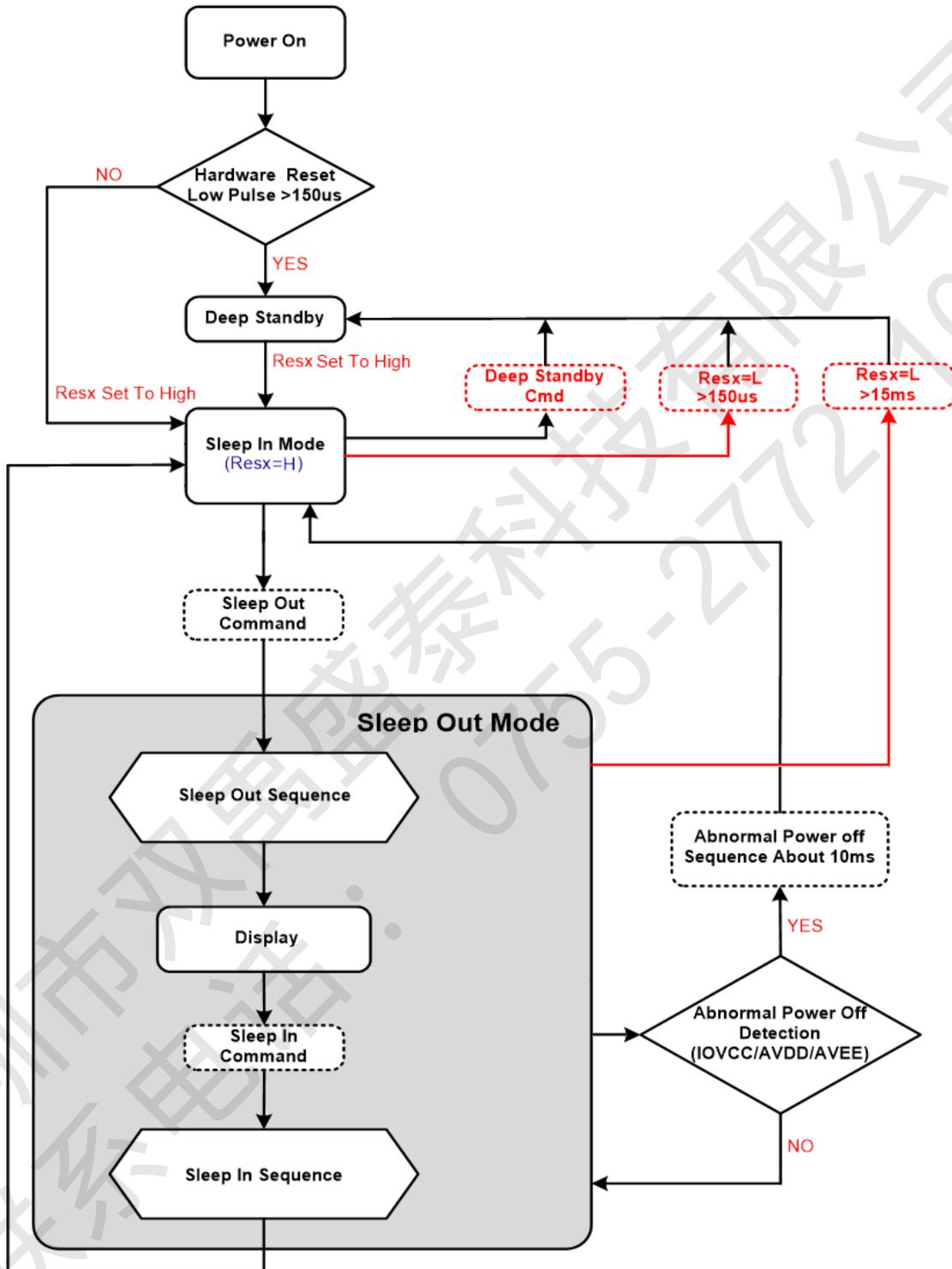
Figure 71 Basic Operation Mode

5.10 Power On/Off Sequence

The power On/Off sequence is illustrated below.
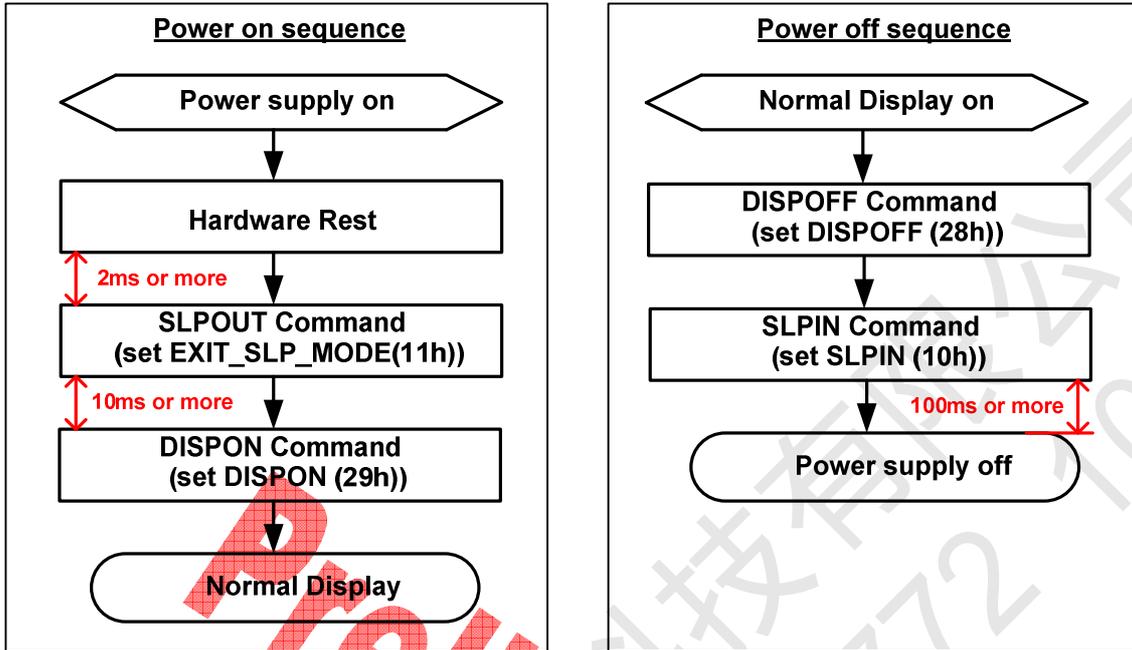
Figure 72 The power On/Off sequence block diagram

5.10.1 Power On/Off Timing

The power On/Off timing diagram is illustrated below.
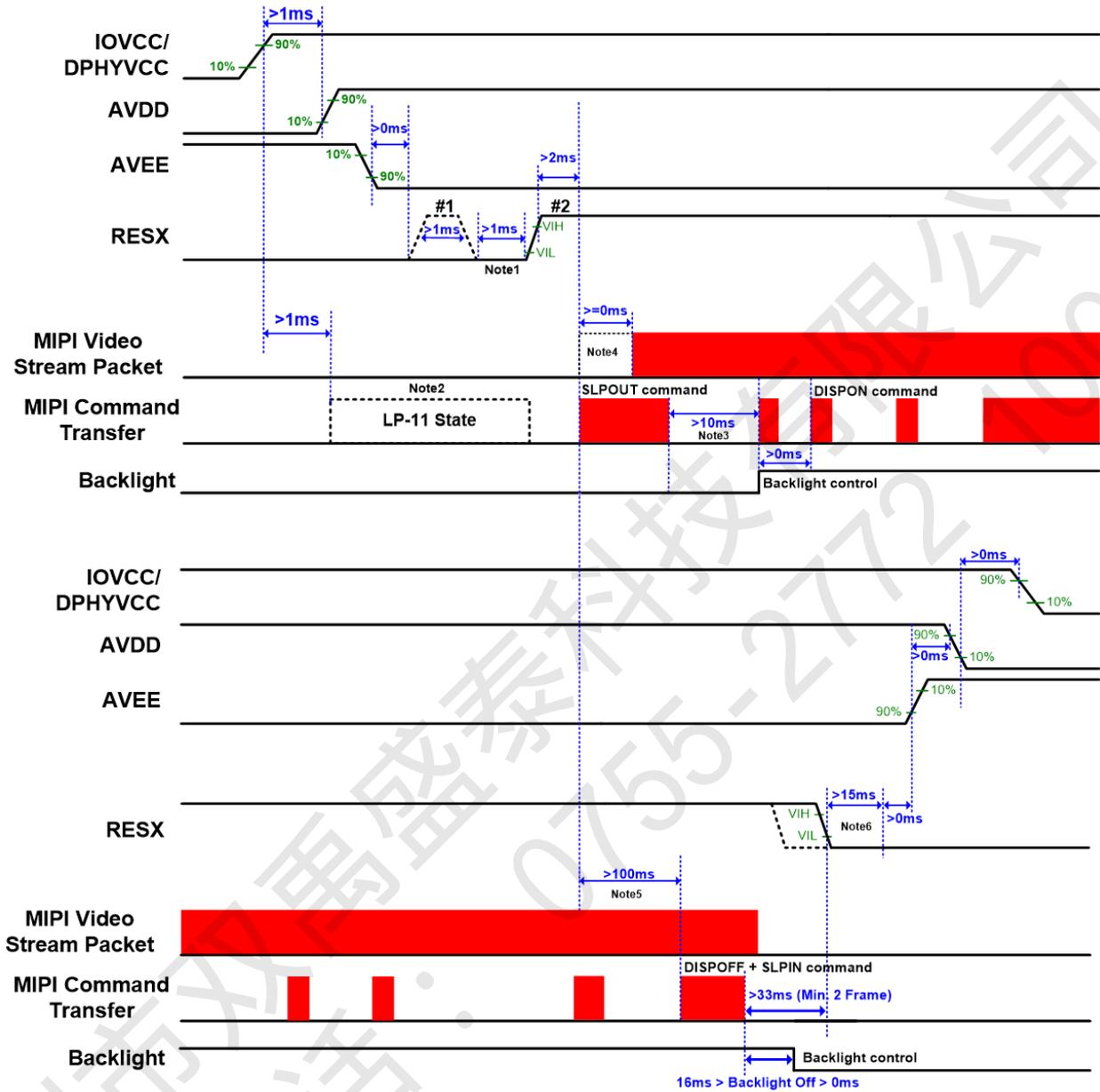
Figure 73 The power on sequence timing

Note 1: The RESX of #1 is better than that of #2.

Note 2: MIPI lanes must go to LP11 after Power IOVCC/DPHYVCC is ready

Note 3: After SLPOUT command, driver IC will start internal power on action. Any other settings should be set after SLPOUT command with a minimum of 10mS.

Note 4: MIPI video stream packet should be sent after both of RESX tied to high with a minimum delay time of 2mS, and video data will not be captured until DISPON.

Note 5: DISPOFF and SLPIN command should be set after SLPOUT command with a minimum delay time of 100mS.

Note 6: RESX tied low into deep standby mode with a minimum time of 15ms.

5.10.2 Power Ramp Up/Down Specifications

The power ramp up/down specifications are illustrate below
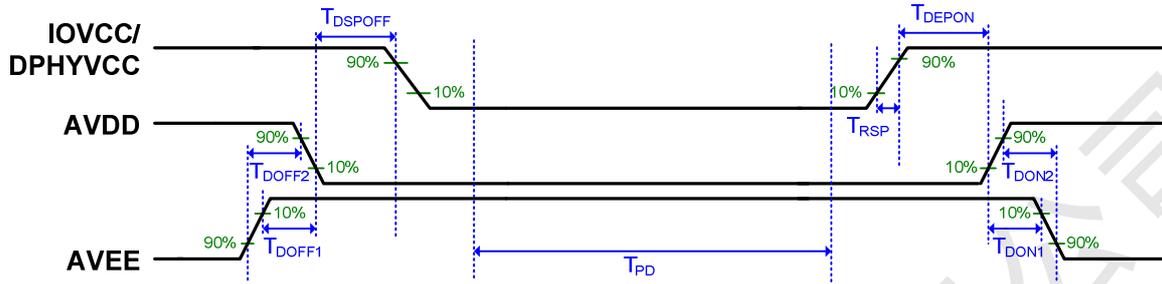
Figure 74 The power ramp up/down timing

Item	Symbol	Unit	Min.	Max.
System power (IOVCC) rise time (10% to 90%)	T_{RSP}	ms	-	2
System power (IOVCC) on to AVDD on time	T_{DEPON}	ms	1	-
AVDD-AVEE on delay time (10% to 10%)	T_{DON1}	ms	0	-
AVDD-AVEE on delay time (90% to 90%)	T_{DON2}	ms	0	-
AVEE-AVDD off delay time (10% to 10%)	T_{DOFF1}	ms	0	-
AVEE-AVDD off delay time (90% to 90%)	T_{DOFF2}	ms	0	-
AVDD off to system power off time	T_{DSPOFF}	ms	0	-
Power down time	T_{PD}	ms	10	

5.11 Instruction Setting Sequence

5.11.1 Sleep Enter/Exit Sequences

When setting instruction to the ST7123, the sequence shown in below figure must be followed to complete the instruction setting.
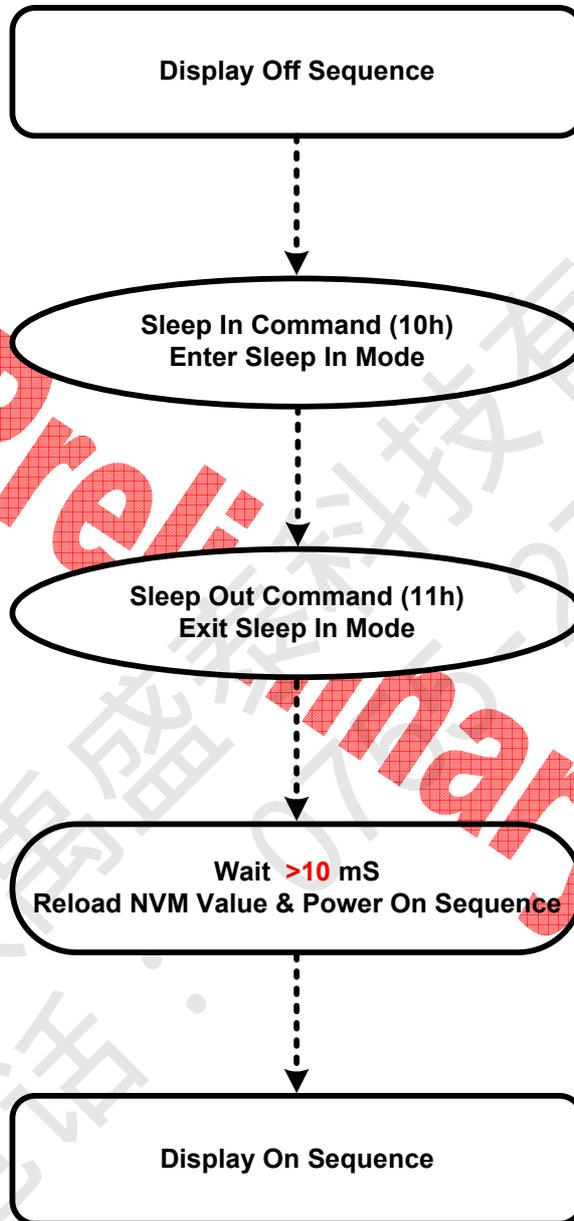
Figure 75 Sleep Enter/Exit Setting Sequence

5.11.2 Deep Standby Mode Enter/Exit Sequences

When setting instruction to the ST7123, the sequence shown in below figure must be followed to complete the

instruction setting.

```
┌─────────────────────────────────┐
│   Display Off Command (28h)     │
│      Enter Display Mode         │
└─────────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────────┐
│    Sleep In Command (10h)       │
│      Enter Sleep In Mode        │
└─────────────────────────────────┘
              ┊   Waiting time>100ms
              ▼
┌─────────────────────────────────┐
│      Deep Standby Command       │
│  (Command=4Fh, Parameter=01h)   │
│     Enter Deep Standby Mode     │
│ Note:                           │
│ For MIPI IF, if deep standby mode used, pull │
│ HSSI_CLK & HSSI_D0~D3 PIN to VSS after │
│ executing deep standby command  │
└─────────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────────┐
│    Exit Deep Standby Command    │
│(Set RESX Pin low pulse>1ms then rise to high)│
│                                 │
│ Note:                           │
│ After exiting deep standby mode, please enables │
│ HSSI_CLK &HSSI_D0~D3 Pin to 1.2V │
└─────────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────────┐
│    Initial Command Setting      │
└─────────────────────────────────┘
              ┊
              ▼
┌─────────────────────────────────┐
│      Display On Sequence        │
└─────────────────────────────────┘
```
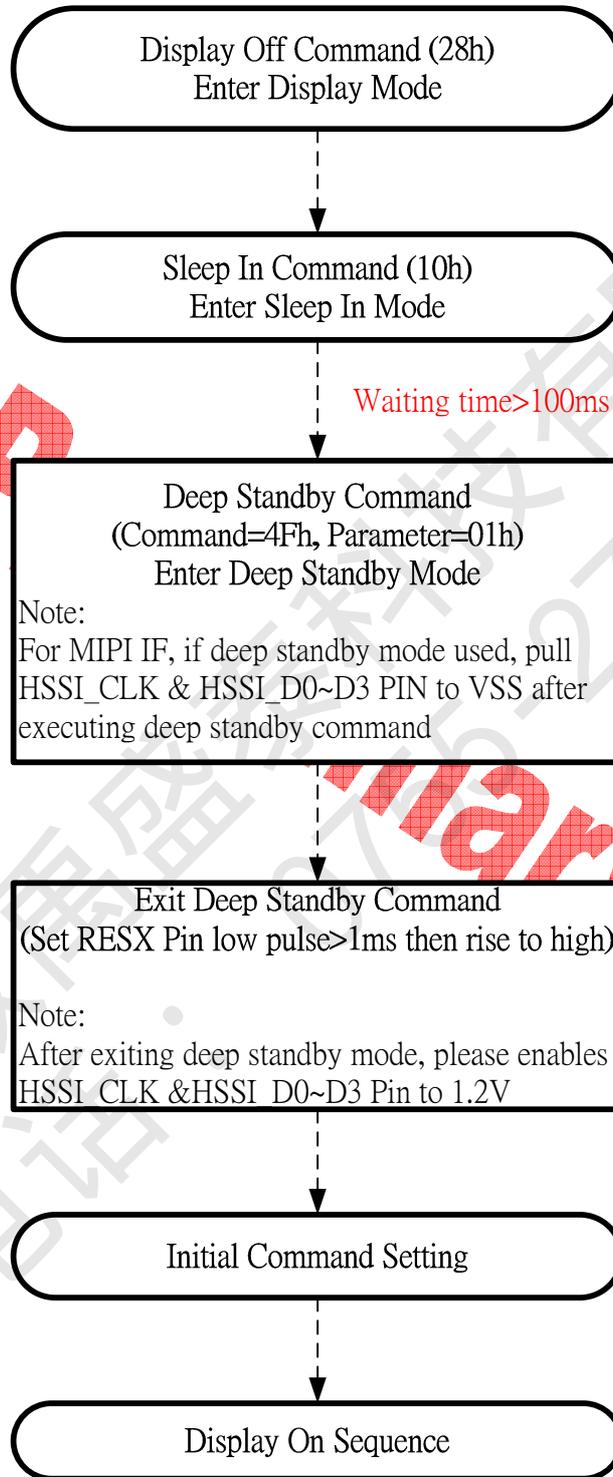
Figure 76 Deep Standby Mode Enter/Exit Setting Sequence

5.12 Touch interface protocol

ST7123 supports SPI and I2C interface, which allows full-duplex, synchronous, serial communications with host controllers. ST7123 SPI equips four serial signals, SS, SCK, MISO and MOSI.

5.12.1 SPI interface

ST7123 operates as a SPI slave device and data length is 16-bit. TP_SPI_SS, TP_SPI_SCK and TP_SPI_MOSI are Schmitt trigger inputs. The data on TP_SPI_MOSI is latched on rising edge of TP_SPI_SCK and the data on TP_SPI_MISO output on falling edge of TP_SPI_SCK. The maximum SPI clock rate is 16 MHz.
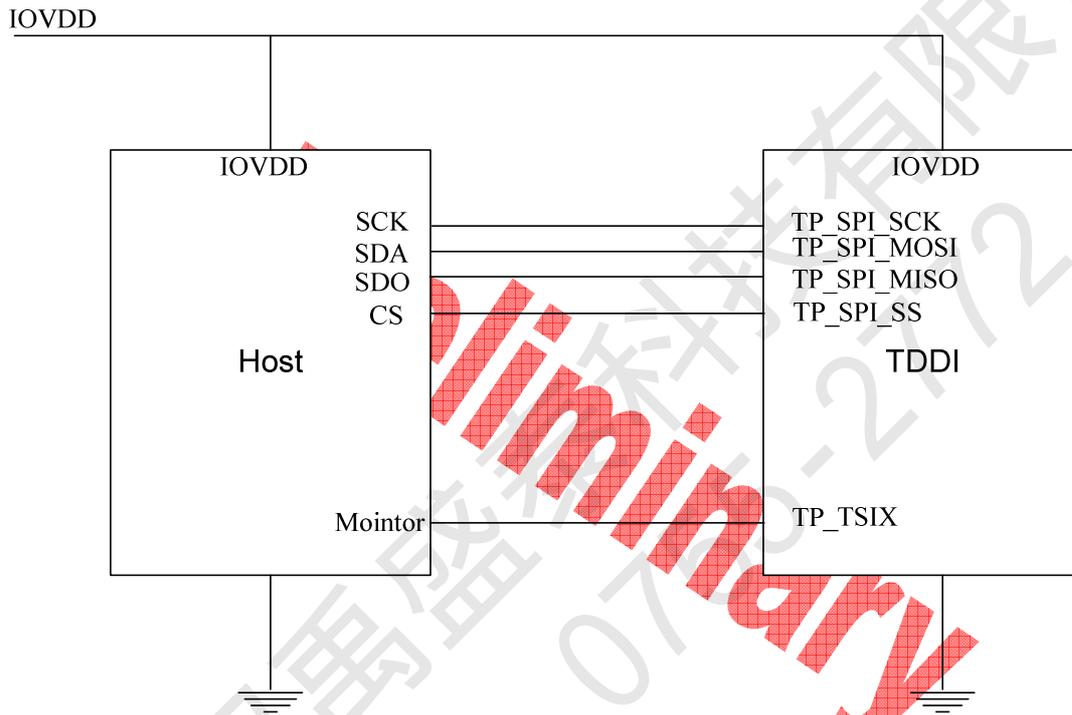
The information transmitted by SPI can be divided into command packet and data packet. Command packet can access register and data packet can access internal RAM. The most significant bit, called ID bit, after TP_SPI_SS falling edge is used to identify command or data packet. And the following bit, called R/W bit, is used to identify write or read operation.

● **Command Protocol**

In command protocol, ID bit of 1st word after TP_SPI_SS falling edge is "0" to indicate register access. R/W bit is "0" to indicate write operation and "1" to indicate read operation. Bit13 to bit0 of 1st word, called ADD bits, are address of register to be accessed. If at write operation, the 2nd word on TP_SPI_MOSI will update the register which is addressed by ADD and afterward ADD will increase one automatically. If at read operation, the 2nd word on TP_SPI_MOSI is dummy

word (value doesn't care). The 3rd word on TP_SPI_MISO will be outputted from register addressed by ADD and similarly ADD is increment afterwards. Keep writing and reading words can access the consecutive registers during one SPI transmission. If accessing non-consecutive register is happened, SS should return to "1" to end current transmission and start another SPI command protocol to assign new register address.
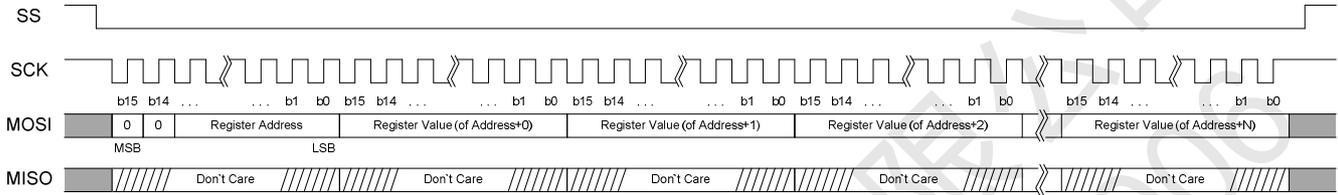
Host write register command
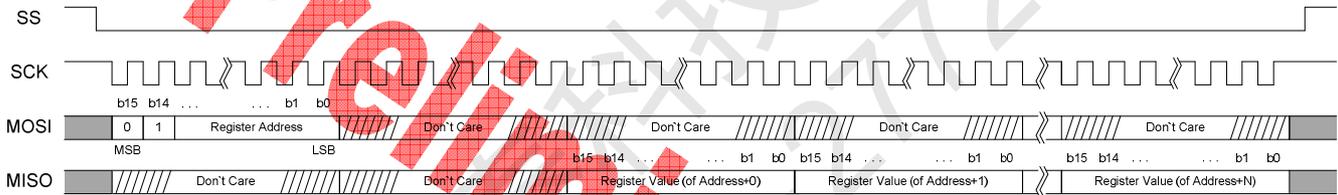
Host read register command

- **Data Protocol**

In data protocol, ID bit of 1st word after SS falling edge is "1" to indicate RAM access. R/W bit is "0" to indicate write operation and "1" to indicate read operation. Bit13 to bit0 of 1st word, called ADD bits, are address of RAM to be accessed. If at write operation, the 2nd word on MOSI will update RAM which is addressed by ADD and afterward ADD will increase one automatically. If at read operation, the 2nd word on MISO is 16-bit header. The 3rd word on MISO will be outputted from RAM addressed by ADD and similarly ADD is increment afterwards. Keep writing and reading words can access the consecutive RAM addresses during one SPI transmission. If accessing non-consecutive RAM address is happened, SS should return to "1" to end current transmission and start another SPI data protocol to assign new RAM address.
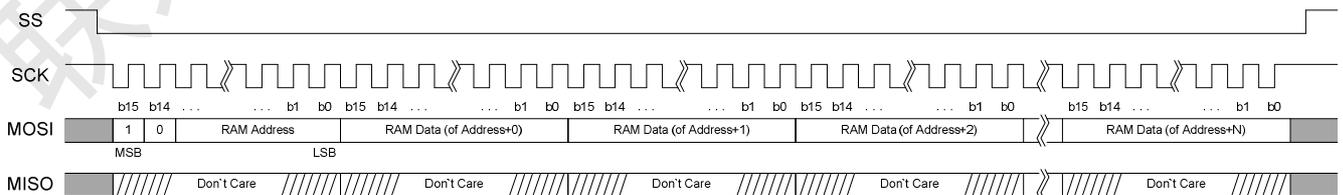
Host write RAM data
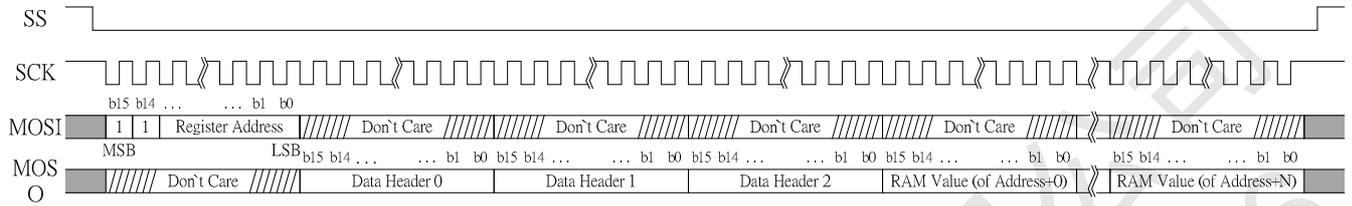
Host read RAM data

5.12.2 I2C

ST7123 protocol supports operating speeds up to 400 kb/s with 7-bit addressing and 8-bit data bytes. The TP_I2C_SCK, TP_I2C_SDA, and TP_TSIX pins are typically used in an I2C interface.

The values of the pull-up resistors should be chosen to ensure that the rise times of the TP_I2C_SDA and TP_I2C_SCK signals are within the limits set by the I2C specification. These values depend on what other devices, if any, are on the I2C bus. Typical values fall within the range of 2 kΩ to 10 kΩ.
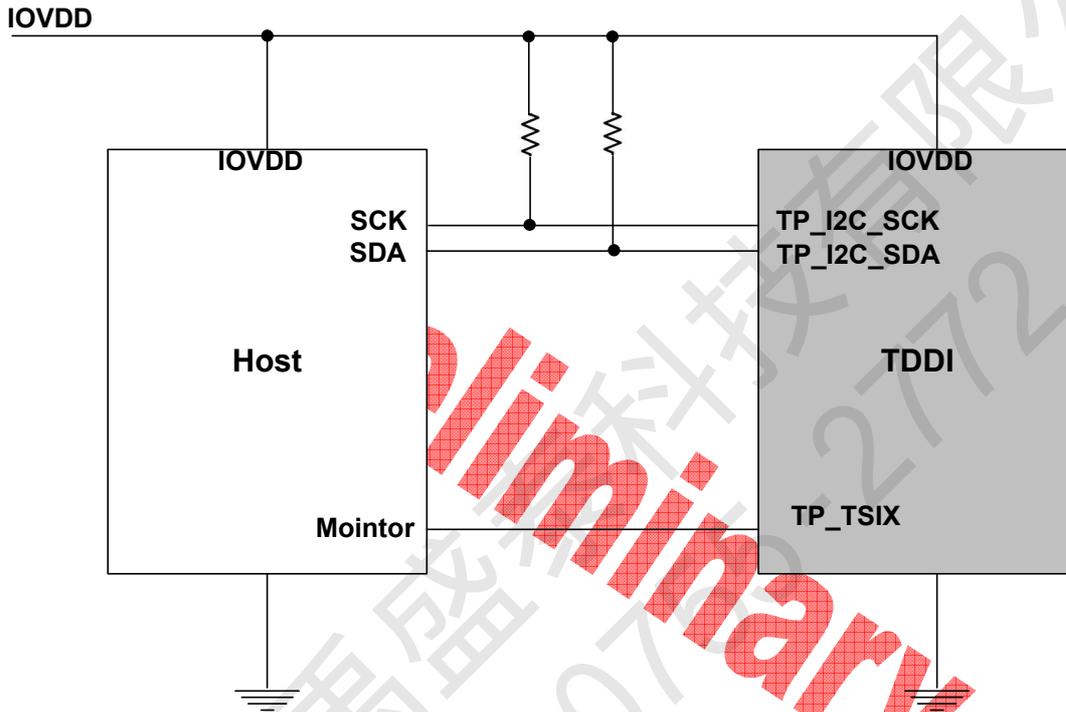
● **I2C Pin Definition**

Name	I/O	Description	Connect Pin
IOVDD	I	Power supply for I/O system	IOVDD
SCK	I	I2C clock pin	TP_I2C_SCK
SDA	I/O	I2C data pin	TP_I2C_SDA
IRQ	O	Data ready interrupt pin	TP_TSIX

● **I2C clock timing**

When a transaction contains the slave address and R/W bit (start condition), the sensor can hold SCL low and checks that the slave address matches. If the slave address fails to match, the sensor no longer clock stretches on subsequent byte transmission until it detects the next start condition. When the slave address matches, the sensor

acknowledges and can continue to clock stretch at the end of subsequent bytes within the same transaction.
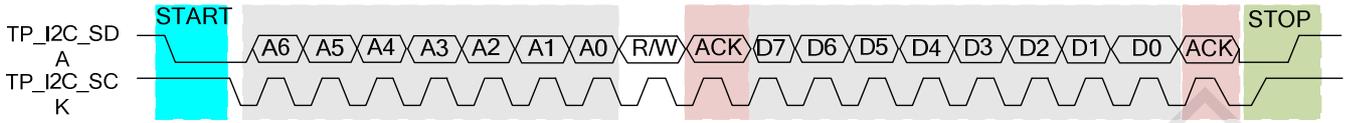
5.12.3 IRQ

ST7123 provides an interrupt pin(TP_TSIX) that is asserted to indicate that new data is available for reading by the host. The TP_TSIX signal is intended to be used as interrupt source to a host. IRQ functionality is added by MCU firmware. The IRQ to host connection as below.
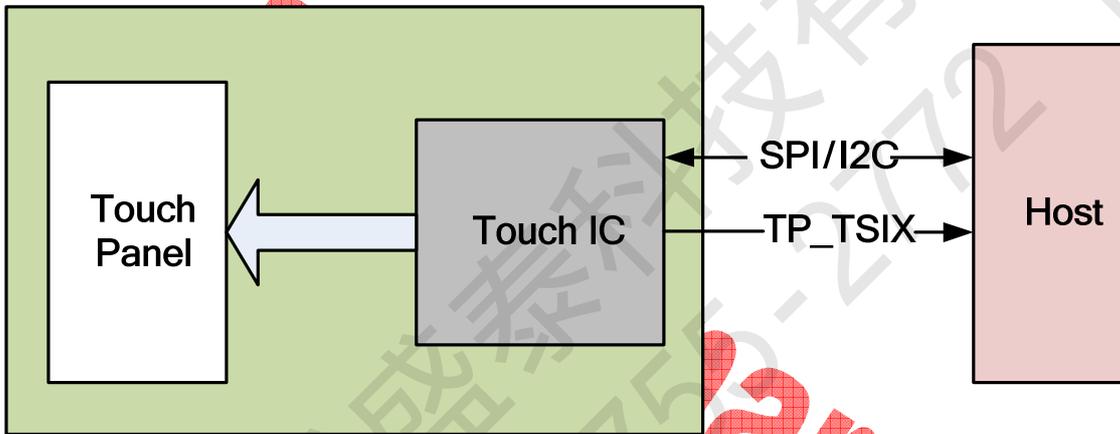
The TP_TSIX pin behavior
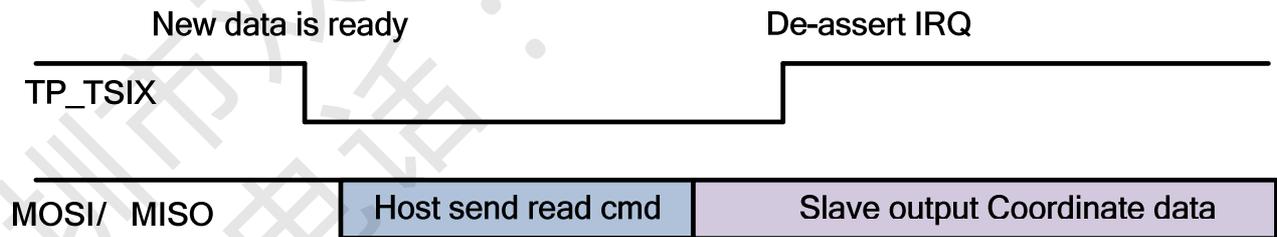
6 COMMAND DESCRIPTION

6.1 User Command Set (UCS) List

Command	(Hex)	Write/Read /Command	NVM option	Function	Parameter Number	MIPI Transmission
NOP	00	C	No	No Operation	0	LPDT/HSDT
SWRESET	01	C	No	Software Reset	0	LPDT/HSDT
RDDID	04	R	No	Read Display Identification Information	3	LPDT/HSDT
RDNUMED	05	R	No	Read Number of Errors on DSI	1	LPDT/HSDT
RDDST	09	R	No	Read Display Status	4	LPDT/HSDT
RDDPM	0A	R	No	Read Display Power Mode	1	LPDT/HSDT
RDDMADCTL	0B	R	No	Read Display MADCTL	1	LPDT/HSDT
RDDIM	0D	R	No	Read Display Image Mode	1	LPDT/HSDT
RDDSM	0E	R	No	Read Display Signal Mode	1	LPDT/HSDT
RDDSDR	0F	R	No	Read Display Self-Diagnostic Result	1	LPDT/HSDT
SLPIN	10	C	No	Enter Sleep In mode	0	LPDT/HSDT
SLPOUT	11	C	No	Enter Sleep Out mode	0	LPDT/HSDT
NORON	13	C	No	Enter Normal Display mode	0	LPDT/HSDT
INVOFF	20	C	No	Display Inversion Off	0	LPDT/HSDT
INVON	21	C	No	Display Inversion On	0	LPDT/HSDT
ALLPOFF	22	C	No	All pixel off	0	LPDT/HSDT
ALLPON	23	C	No	All pixel on	0	LPDT/HSDT
GAMSEL	26	C	No	Gamma curve select	1	LPDT/HSDT
DISPOFF	28	C	No	Display off	0	LPDT/HSDT
DISPON	29	C	No	Display on	0	LPDT/HSDT
TEOFF	34	C	No	Tearing Effect Line Off	0	LPDT/HSDT
TEEON	35	W	No	Tearing Effect Line On	1	LPDT/HSDT
MADCTL	36	W	Yes	Memory Access Direction Control	1	LPDT/HSDT
IDMOFF	38	W	No	Idle Mode OFF	0	LPDT/HSDT
IDMON	39	W	No	Idle Mode ON	0	LPDT/HSDT
TESLWR	44	W	No	Write TE Scan Line	2	LPDT/HSDT
TESLRD	45	R	No	Read Scan Line	2	LPDT/HSDT
DSTB	4F	W	No	Deep standby mode on	1	LPDT/HSDT
WRDISBV	51	W	No	Write Display Brightness	1	LPDT/HSDT
RDDISBV	52	R	No	Read Display Brightness Value	1	LPDT/HSDT
WRCTRLD	53	W	No	Write CTRL Display	1	LPDT/HSDT

RDCTRLD	54	R	No	Read CTRL Display	1	LPDT/HSDT
WRCABC	55	W	No	Write Content Adaptive Brightness Control	1	LPDT/HSDT
RDCABC	56	R	No	Read Content Adaptive Brightness Control	1	LPDT/HSDT
WRCABCMB	5E	W	No	Write CABC Minimum Brightness	1	LPDT/HSDT
RDCABCMB	5F	R	No	Read CABC Minimum Brightness	1	LPDT/HSDT
RDID1	DA	R	Yes	Read ID1	1	LPDT/HSDT
RDID2	DB	R	Yes	Read ID2	1	LPDT/HSDT
RDID3	DC	R	Yes	Read ID3	1	LPDT/HSDT
RDDDBS	A1	R	No	Read DDB Start	8	LPDT/HSDT
RDDDBC	A8	R	Yes	Read DDB Continue	8	LPDT/HSDT
RDFCS	AA	R	No	Read First Checksum	1	LPDT/HSDT
RDCCS	AF	R	No	Read Continue Checksum	1	LPDT/HSDT
RDICCD	F4	R	No	Read Sitronix IC ID	2	LPDT/HSDT
MIPIEXTFMAT	F9	W/R	YES	MIPI Extension Format	1	LPDT/HSDT

Note: LPDT (Low Power Mode), HSDT (High Speed Mode)

6.2   User Command Set (UCS) DESCRIPTION

6.2.1   NOP (00H) : No Operation

00H	NOP (No Operation)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
NOP	Write	0	0	0	0	0	0	0	0	(00H)
Parameter	No Parameter									-
Description	- This command is empty command. It does not have effect on the display module.									
Restriction	-									
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									

6.2.2 SWRESET (01H): Software Reset

01H	SWRESET (Software Reset)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
SWRESET	Write	0	0	0	0	0	0	0	1	(01H)
Parameter	No Parameter									-
Description	- When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to VSS (display off).									
Restriction	-									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.3 RDDID (04H) Read Display Identification Information

04H		RDDID (Read Display Identification Information)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID	Write	0	0	0	0	0	1	0	0	(04H)
1st Parameter	Read	ID1[7:0]								FFh
2nd Parameter	Read	ID2[7:0]								FFh
3rd Parameter	Read	ID3[7:0]								FFh
Description		- Read Display Identification Information -ID1 : LCD module's manufacturer ID (FFh: not programmed) -ID2 : LCD module/driver version ID (FFh: not programmed) -ID3 : LCD module/driver ID (FFh: not programmed)									
Restriction		-									
Register Availability											

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.4   RDNUMED (05H) Read Number of Errors on DSI

05H	RDNUMED									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDNUMED	Write	0	0	0	0	0	1	0	1	(05H)
1st Parameter	Read	DSI_NUMBER[7:0]								00h
Description	- Read Number of Errors on DSI, DSI_NUMBER[7:0] is a number of the errors on DSI.									
Restriction	-									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.5 RDDST (09H) Read Display Status

09H					RDNUMED(Read Display Status)					
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	(Default)
RDDST	Write	0	0	0	0	1	0	0	1	(09H)
1st Parameter	Read	Booster_on	0	0	0	0	BGR	0	CA	00h
2nd Parameter	Read	LA	0	0	0	IDMON	0	SLPOUT	NORON	00h
3rd Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	DSPON	TEON	GAMM_SEL[2]	00h
4th Parameter	Read	GAMMA_SEL[1]	GAMMA_SEL[0]	TEMOD	0	0	0	0	EOD	00h

	- This command indicates the current status of the display as described in the table below :		
	Bit	**Description**	**Value**
	Booster_on	Booster status	'1' = Booster on. '0' = Booster off
	CA	Column Address Order (CA)	'1' = Decrement, (Right to Left, when MADCTL (36h) CA='1') '0' = Increment, (Left to Right, when MADCTL (36h) CA='0')
	LA	Row Address Order (LA)	'1' = Row/column exchange, (when MADCTL (36h) LA='1') '0' = Normal, (when MADCTL (36h) LA='0'
	BGR	RGB/ BGR Order	'1' = BGR Order, (When MADCTL (36h) BGR='1') '0' = RGB Order, (When MADCTL (36h) BGR='0')
	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
	SLPOUT	Sleep In/Out Mode	'1' = Sleep Out Mode '0' = Sleep In Mode
Description	NORON	Normal mode	'1' = Normal Mode on '0' = Normal Mode off
	DSPON	Display On/Off Mode	'1' = Display On Mode '0' = Display Off Mode
	INVON	Inversion On/Off Mode	'1' = Inversion On Mode '0' = Inversion Off Mode
	ALLPON	All pixel on	'1' = All pixel on '0' = Normal mode
	ALLPOFF	All pixel off	'1' = All pixel off '0' = Normal mode
	TEON	Tearing effect line on/off	'1' = Inversion On Mode '0' = Inversion Off Mode
	GAMMA_SEL[2:0]	Gamma curve selection	'000' = Gamma curve 1(gamma 2.2) 'others' = reserved
	TEMOD	Tearing effect line mode	'1' = V- blanking and H-blanking

			'0' = V-blanking only
	EOD	Error on DSI	'1' = Error
			'0' = No Error
Restriction	-		
Register Availability			

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.6 RDDPM (0AH): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDPM	Write	0	0	0	0	1	0	1	0	(0AH)
1st Parameter	Read	Booster_on	IDMON	0	SLPOUT	NORON	DSPON	0	0	00h

Description	- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
Booster_on	Booster status	'1' = Booster on. '0' = Booster off
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off
SLPOUT	Sleep In/Out Mode	'1' = Sleep Out Mode '0' = Sleep In Mode
NORON	Normal mode	'1' = Normal Mode on '0' = Normal Mode off
DSPON	Display On/Off Mode	'1' = Display On Mode '0' = Display Off Mode

Restriction	-

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.7 RDDMADCTR (0BH): Read Display MADCTR

0BH	RDDMADCTR (Read Display MADCTR)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDMADCTR	Write	0	0	0	0	1	0	1	1	(0BH)
1st Parameter	Read	0	0	0	0	BGR	0	CA	LA	00h

Description	- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
CA	Column Address Order (CA)	'1' = Decrement, (Right to Left, when MADCTL (36h) CA='1')
		'0' = Increment, (Left to Right, when MADCTL (36h) CA='0')
LA	Row Address Order (LA)	'1' = Row/column exchange, (when MADCTL (36h) LA='1')
		'0' = Normal, (when MADCTL (36h) LA='0'
BGR	RGB/ BGR Order	'1' = BGR Order, (When MADCTL (36h) BGR='1')
		'0' = RGB Order, (When MADCTL (36h) BGR='0')

Restriction	-

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.8 RDDCOLM (0CH): Read Display Color Mode

0DH	RDDIM (Read Display Image Mode)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDIM	Write	0	0	0	0	1	1	0	1	(0CH)
1st Parameter	Read	0	0	0	0	0	DBI[2:0]			00h

Description	- This command indicates the current status of the display as described in the table.
	<table><tr><th>DBI[2:0]</th><th>Color Format</th></tr><tr><td>0h~4h</td><td>Reserved</td></tr><tr><td>5h</td><td>16-bit/pixel</td></tr><tr><td>6h</td><td>18-bit/pixel</td></tr><tr><td>7h</td><td>24-bit/pixel</td></tr></table>
	Note: For DBI[2:0] definition refer to interface Pixel Format (3Ah)
Restriction	-
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>

6.2.9 RDDIM (0DH): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDIM	Write	0	0	0	0	1	1	0	1	(0DH)
1st Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	GAMMA_SEL[2:0]			00h

- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
INVON	Inversion On/Off Mode	'1' = Inversion On Mode '0' = Inversion Off Mode
ALLPON	All pixel on	'1' = All pixel on '0' = Normal display
ALLPOFF	All pixel off	'1' = All pixel off '0' = Normal display
GAMMA_SEL[2:0]	Gamma curve selection	'000' = Gamma curve 1(gamma 2.2) 'others' = Reserved

Restriction -

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.10   RDDSM (0EH): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Mode)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDSM	Write	0	0	0	0	1	1	0	1	(0EH)
1st Parameter	Read	TEON	TEM	0	0	0	0	0	EOD	00h

Description	- This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = Inversion On Mode '0' = Inversion Off Mode
TEM	Tearing effect line mode	'1' = V- blanking and H-blanking '0' = V-blanking only
EOD	Error on DSI	'1' = Error '0' = No Error

Restriction	-

Register Availability	**Status**	**Availability**
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.11 RDDSDR(0FH): Read Display Self-Diagnostic Result

0FH	RDDSM (Read Display Signal Mode)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDSDR	Write	0	0	0	0	1	1	1	1	(0FH)
1st Parameter	Read	RLD	FD	0	0	0	0	0	CCR	00h

Description	- This command indicates the current status of the display as described in the below:
	
	-RLD: This bit is the Register Loading Detection
	
	-FD: This bit is the Functionality Detection
	
	-CCR: The checksum compare result.
	
	    0 = Checksum is the same.
	
	    1 = Checksum is not the same

Restriction	-
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>

6.2.12 SLPIN (10H): Sleep In

10H	SLPIN (Sleep In)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
SLPIN	Write	0	0	0	1	0	0	0	0	(10H)
Parameter	No Parameter								-
Description	- This command causes the LCD module to enter the minimum power consumption mode. - In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped. 								
Restriction	- This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11H). - It will be necessary to wait 5ms before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. - It will be necessary to wait 120ms after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.								
Register Availability		Status			Availability				
		Sleep Out, Display On			Yes				
		Sleep In			No				

6.2.13 SLPOUT (11H): Sleep Out

11H	SLPOUT (Sleep Out)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
SLPOUT	Write	0	0	0	1	0	0	0	1	(11H)
Parameter	No Parameter									-
Description	- This command turns off sleep mode. - In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started. Sleep Out Internal Oscillator — Stop — Start Gate Output — Stop — Stop Source Output — 0V — 0V Blanking Display(over 1 Frame)									
Restriction	- This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10H). - It will be necessary to wait 5ms before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. - DRIVER loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the DRIVER is already Sleep Out mode. - It will be necessary to wait 120ms after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent									
Register Availability		Status				Availability				

Status	Availability
Sleep Out, Display On	No
Sleep In	Yes

6.2.14   NORON (13H): Normal display mode On

13H	NORON (Normal Display Mode On)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
INVOFF	Write	0	0	0	1	0	0	1	1	(13H)
Parameter	No Parameter									-
Description	- This command is used to return display to normal display mode. -.This command can exit all pixel on/off mode to normal display mode.									
Restriction										
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.15　INVOFF (20H) : Display Inversion Off

20H	INVOFF (Display Inversion Off)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
INVOFF	Write	0	0	1	0	0	0	0	0	(20H)
Parameter	No Parameter								-
Description	- This command is used to recover from display inversion mode. - This command makes no change of contents of frame memory. - This command does not change any other status. (Example) Memory　　　　　　Display .								
Restriction	- This command has no effect when module is already in inversion off mode.								
Register Availability	Status			Availability					
	Sleep Out, Display On			Yes					
	Sleep In			Yes					

6.2.16 INVON (21H) : Display Inversion On

21H	INVON (Display Inversion On)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
INVON	Write	0	0	1	0	0	0	0	1	(21H)
Parameter	No Parameter									-
Description	- This command is used to enter into display inversion mode. - This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. - This command does not change any other status. 									
Restriction	- This command has no effect when module is already in inversion off mode.									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									

6.2.17 ALLPOFF (22H): All pixel off

22H	ALLPOFF (All pixel off)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
ALLPOFF	Write	0	0	1	0	0	0	1	0	(22H)
Parameter	No Parameter									-
Description	- This command is used to black display In sleep out mode. - Exit from this command by All pixel on(23H) or Normal display mode(13H)									
Restriction										
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	No

6.2.18 ALLPON (23H): All pixel on

23H	ALLPOFF (All pixel off)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
ALLPON	Write	0	0	1	0	0	0	1	1	(23H)
Parameter	No Parameter								-
Description	- This command is used to white display In sleep out mode. - Exit from this command by All pixel off(22H) or Normal display mode(13H)								
Restriction									
Register Availability									

Status	Availability
Sleep Out, Display On	Yes
Sleep In	No

6.2.19 GAMSEL (26H): Gamma Curve Select

26H		(Gamma Curve Select)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
GAMSEL	Write	0	0	1	0	0	1	1	0	(26H)
Parameter	Write	0	0	0	0	GC[3:0]				

Description	- This command is used to select gamma curve, and only 1 curve (gamma 2.2) can be selected. 	GC[3:0]	Gamma Curve
1	Gamma 2.2
others	Reserved	
Restriction	
Register Availability		Status	Availability
Sleep Out, Display On	Yes
Sleep In	No	

6.2.20 DISPOFF (28H): Display Off

28H	DISPOFF (Display Off)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
DISPOFF	Write	0	0	1	0	1	0	0	0	(28H)
Parameter	No Parameter									-
Description	- This command is used to enter into DISPLAY OFF mode. In this mode. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29H) 								
Restriction	-This command has no effect when module is already in Display Off mode.								
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	No

6.2.21 DISPON (29H): Display On

29H	DISPON (Display On)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
DISPON	Write	0	0	1	0	1	0	0	1	(29H)
Parameter	No Parameter									-
Description	- This command is used to recover from DISPLAY OFF mode. - This command makes no change of contents of frame memory. - This command does not change any other status.								

(Example) Memory → Display

Restriction	-This command has no effect when module is already in Display Off mode.

Register Availability	Status	Availability
	Sleep Out, Display On	No
	Sleep In	Yes

6.2.22 TEOFF (34H): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
TEOFF	Write	0	0	1	1	0	1	0	0	(34H)
Parameter	No Parameter									-
Description	- This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	- This command has no effect when Tearing Effect output is already OFF.									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.23 TEON (35H): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
TEON	Write	0	0	1	1	0	1	0	1	(35H)
1st Parameter	Write	0	0	0	0	0	0	0	TEM	00h

Description	-Tearing Effect Mode ON - Mode 1: When TEM = '0', The tearing effect output line consists of V-blanking information only. t_{vdl} t_{vdh} Vertical Time Scale - Mode 2: When TEM = '1': The tearing effect output line consists of both V-blanking and H-blanking information. t_{vdl} t_{vdh} Vertical Time Scale *Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.*
Restriction	- This command has no effect when Tearing Effect output is already ON.
Register Availability	
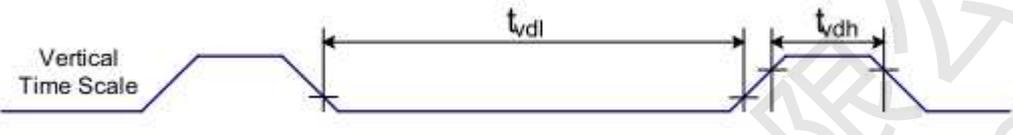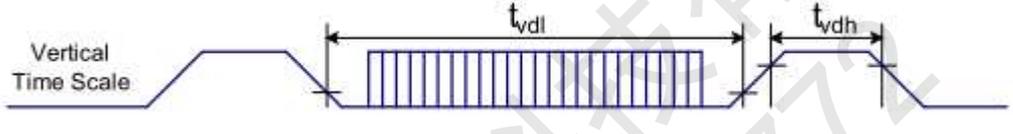
Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.24 MADCTR (36H): Memory Data Access Control

36H	MADCTR (Memory Data Access Control)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
MADCTR	Write	0	0	1	1	0	1	1	0	(36H)
1st Parameter	Read	0	0	0	0	BGR	0	CA	LA	00h

Description

- Bit Assignment

Bit	Description	Value
CA	Column Address Order (CA)	'1' = Decrement, (Right to Left, when MADCTL (36h) CA='1') '0' = Increment, (Left to Right, when MADCTL (36h) CA='0')
LA	Row Address Order (LA)	'1' = Row/column exchange, (when MADCTL (36h) LA='1') '0' = Normal, (when MADCTL (36h) LA='0'
BGR	RGB/ BGR Order	'1' = BGR Order, (When MADCTL (36h) BGR='1') '0' = RGB Order, (When MADCTL (36h) BGR='0')

-CA :

LA :

Top-Left (0,0)   MIPI Input   Top-Left (0,0)   Display

LA = '0'

Send first
Send 2nd
Send 3rd
:
Send last

Top-Left (0,0)   MIPI Input   Top-Left (0,0)   Display

LA = '1'

Send last
:
Send 3rd
Send 2nd
Send first

BGR :

RGB="0"

Drive IC

| R | G | B | | R | G | B | — — — | R | G | B |

SIG   SIG   SIG720

SIG   SIG   SIG720
| R | G | B | | R | G | B | — — — | R | G | B |

| R | G | B | | R | G | B | — — — | R | G | B |

Display

RGB="1"

Drive IC

| R | G | B | | R | G | B | — — — | R | G | B |

SIG   SIG   SIG720

SIG   SIG   SIG720
| B | G | R | | B | G | R | — — — | B | G | R |

| B | G | R | | B | G | R | — — — | B | G | R |

Display

Restriction	-

Register Availability

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.25 IDMOFF (38H): Idle Mode Off

38H	IDMOFF (Idle Mode Off)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
IDMOFF	Write	0	0	1	1	1	0	0	0	(38H)
Parameter	No Parameter	No Parameter								-
Description	-This command is used to recover from Idle mode on.									
Restriction	-This command has no effect when module is already in idle off mode									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.26 IDMON (39H): Idle Mode On

38H		IDMOFF (Idle Mode Off)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
IDMON	Write	0	0	1	1	1	0	0	1	(39H)
Parameter	No Parameter	No Parameter								-

Description	-This command is used to enter into Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle on mode, 1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from IDMON by Idle Mode Off (38h) command

Color	R[7:0]	G[7:0]	B[7:0]
Blank	0xxxxxxx	0xxxxxxx	0xxxxxxx
Blue	0xxxxxxx	0xxxxxxx	1xxxxxxx
Red	1xxxxxxx	0xxxxxxx	0xxxxxxx
Magenta	1xxxxxxx	0xxxxxxx	1xxxxxxx
Green	0xxxxxxx	1xxxxxxx	0xxxxxxx
Cyan	0xxxxxxx	1xxxxxxx	1xxxxxxx
Yellow	1xxxxxxx	1xxxxxxx	0xxxxxxx
White	1xxxxxxx	1xxxxxxx	1xxxxxxx

Restriction	-This command has no effect when module is already in idle on mode

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.27 TESLWR (44H): Write TE Scan Line

44H		WRTESCN (Write TE Scan Line)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
TESLWR	Write	0	1	0	0	0	1	0	0	(44H)
1st Parameter	Write	-	-	-	-	TESN[11:8]				00h
2nd Parameter	Write	TESN[7:0]								00h
Description	- This command turns on the display module's TE signal when the display module reaches line TESN.									
Restriction	- The command takes affect with the end of one frame.									
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									

6.2.28 RDSCNL (45H): Read Scan Line

45H	RDSCNL (Read Scan Line)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDSCNL	Write	0	1	0	0	0	1	0	1	(45H)
1st Parameter	Read	-	-	-	-	TESN[11:8]				00h
2nd Parameter	Read	TESN[7:0]								00h
Description	- This read byte returns the current scan line.									
Restriction	- The command takes affect with the end of one frame.									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.29   DSTB (4FH): Deep Standby Mode ON

4FH	DSTB (Deep Standby Mode ON)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
DSTB	Write	0	1	0	0	1	1	1	1	(4FH)
Parameter	Write	0	0	0	0	0	0	0	DSTB	00H

Description	- When DSTB = 1 :Deep Standby Mode ON Exit deep standby mode by pulling low "RESX" pin at least 1ms
Restriction	- Only effect at Sleep In mode.

Register Availability	Status	Availability
	Sleep Out, Display On	No
	Sleep In	Yes

6.2.30 WRDISBV (51H) Write Display Brightness

51H	WRDISBV (Write Display Brightness)									
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDSCNL	Write	0	1	0	1	0	0	0	1	(51h)
1st Parameter	Write	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h
Description	- This command is used to adjust the brightness value of the display. - It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. - In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									
Register Availability	<table><tr><td>Status</td><td>Availability</td></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									

6.2.31 RDDISBV (52H) Read Display Brightness Value

52H	RDDISBV (Read Display Brightness Value)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDISBV	Write	0	1	0	1	0	0	1	0	(52h)
1st Parameter	Read	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	00h

Description	- This command returns the brightness value of the display. - It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. - In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. - See command "Write Display Brightness (51H)". - This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode. - DBV [7:0] is reset when display is in sleep-in mode. - DBV [7:0] is '0' when bit BCTRL of "Write CTRL Display (53H)" command is '0'. - DBV[7:0] is manual set brightness specified with "Write CTRL Display (53H)" command when bit BCTRL is '1'
Restriction	-
Register Availability	Status / Availability table below

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.32   WRCTRLD (53H) Write CTRL Display

53H	WRCTRLD (Write CTRL Display)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
WRCTRLD	Write	0	1	0	1	0	0	1	1	(53h)
1st Parameter	Write	0	0	BCTRL	0	DD	BL	0	0	00h

Description	- This command is used to control ambient light, brightness and gamma settings. -BCTRL：Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard. '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the other parameters.) -DD：Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on -BL：Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On -Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at dimming-on (DD=1). -When BL bit changed from 'on' to 'off', backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.
Restriction	-
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>

6.2.33 RDCTRLD (54H) Read CTRL Display

54H	RDCTRLD (Read CTRL Display)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCTRLD	Write	0	1	0	1	0	1	0	0	(54h)
1st Parameter	Read	0	0	BCTRL	0	DD	BL	0	0	00h

Description	-This command returns ambient light and brightness control values. -BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. '0' = Off '1' = On -DD: Display Dimming On/Off (Only for manual brightness setting) '0' = Off '1' = On -BL: Backlight Control On/Off '0' = Off '1' = On
Restriction	-

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.34   WRCABC (55H) Write Content Adaptive Brightness Control

55H	| WRCABC (Write Content Adaptive Brightness Control)							
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
WRCABD	Write	0	1	0	1	0	1	0	1	(55h)
1st Parameter	Write	CEON	SREON	EN_LEVEL[1:0]		0	0	CABC_MODE[1:0]		00h

Description
- CEON: Color and Skin Enhancement ON/OFF.
'0' = OFF
'1' = ON
- SREON: Sunlight Readability Enhancement ON/OFF
'0' = OFF
'1' = ON
-EN_LEVEL: Enhancement mode Selection

CEON	SREON	EN_LEVEL[1:0]		Function
0	0	0	0	Enhancement OFF
1	0	0	0	CE LOW
1	0	0	1	CE MIDDLE
1	0	1	1	CE HIGH
0	1	0	0	SRE LOW
0	1	0	1	SRE MIDDLE
0	1	1	0	SRE HIGH
0	1	1	1	SRE USER DEFINE
1	1	0	0	CE / SRE LOW
1	1	0	1	CE / SRE MIDDLE
1	1	1	X	CE / SRE HIGH

Note: "X" is don't care

-CABC_MODE: CABC mode selection

CABC_MODE	Function
0	Off
1	User Interface Mode
2	Still Picture
3	Moving Image

Restriction	-

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.35 RDCABC (56H) Read Content Adaptive Brightness Control

56H	WRCABC (Write Content Adaptive Brightness Control)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCABD	Write	0	1	0	1	0	1	1	0	(56h)
1st Parameter	Read	CEON	SREON	EN_LEVEL[1:0]		0	0	CABC_MODE[1:0]		00h

Description	- CEON: Color and Skin Enhancement ON/OFF.

'0' = OFF

'1' = ON

- SREON: Sunlight Readability Enhancement ON/OFF

'0' = OFF

'1' = ON

-EN_LEVEL: Enhancement mode Selection

CEON	SREON	EN_LEVEL[1:0]		Function
0	0	0	0	Enhancement OFF
1	0	0	0	CE LOW
1	0	0	1	CE MIDDLE
1	0	1	1	CE HIGH
0	1	0	0	SRE LOW
0	1	0	1	SRE MIDDLE
0	1	1	0	SRE HIGH
0	1	1	1	SRE USER DEFINE

Note: "X" is don't care.

-CABC_MODE: CABC mode selection

CABC_MODE[1:0]	Function
00b	Off
01b	User Interface Mode
10b	Still Picture
11b	Moving Image

Restriction	-

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.36 WRCABCMB (5EH) Write CABC Minimum Brightness

5EH	WRCABCMB (Write CABC Minimum Brightness)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
WRCABCMB	Write	0	1	0	1	1	1	1	0	(5Eh)
1st Parameter	Write	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00h
Description	- This command is used to set the minimum brightness value of the display for CABC function. - In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.								
Restriction	-								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>								

6.2.37 RDCABCMB (5FH) Read CABC Minimum Brightness

5FH	RDCABCMB (Read CABC Minimum Brightness)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCABCMB	Write	0	1	0	1	1	1	1	1	(5Fh)
1st Parameter	Read	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	00h
Description	- This command returns the minimum brightness value of CABC function. - In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. - See command "Write CABC Minimum Brightness (5EH)".									
Restriction	-									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.38   RDDID1 (DAH) Read Display Identification Information

DAH	RDDID1 (Read Display Identification Information 1)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID1	Write	0	0	0	0	0	1	0	1	(DAH)
1st Parameter	Read	ID1[7:0]								FFh
Description	- Read Display Identification Information ID1:LCD module's manufacturer ID (FFh: not programmed)									
Restriction	-									
Register Availability										

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.39 RDDID2 (DBH) Read Display Identification Information

DBH	RDDID2 (Read Display Identification Information 2)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID2	Write	0	0	0	0	0	1	0	1	(DBH)
1st Parameter	Read	ID2[7:0]								FFh
Description	- Read Display Identification Information ID2:LCD module/driver version ID (FFh: not programmed)									
Restriction	-									
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									

6.2.40   RDDID3 (DCH) Read Display Identification Information

DCH	RDDID 3 (Read Display Identification Information 3)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDID3	Write	0	0	0	0	0	1	0	1	(DCH)
1st Parameter	Read	ID3[7:0]								FFh
Description	- Read Display Identification Information ID3:LCD module/driver ID (FFh: not programmed)									
Restriction	-									

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.41 RDDDBS (A1H) : Read DDB Start

A1H		RDDDBS (Read DDB Start)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDDBS	Write	1	0	1	0	0	0	0	1	(A1H)
1st Parameter	Read	SID[7:0]								FFh
2nd Parameter	Read	SID[15:8]								FFh
3rd Parameter	Read	MID[7:0]								FFh
4th Parameter	Read	MID[15:8]								FFh
5th parameter	Read	RID[7:0]								FFh
6th Parameter	Read	RID[15:8]								FFh
7th Parameter	Read	DDB_ID_1[7:0]								FFh
8th Parameter	Read	DDB_ID_2[7:0]								FFh
9th Parameter	Read	DDB_ID_3[7:0]								FFh
10th Parameter	Read	DDB_ID_4[7:0]								FFh

Description	- This command returns supplier identification and display module / revision information. Note: 1. This information is not the same what DAh/DBh/DCh commands are returning. 2. Parameter 8th is an "Exit code", this means that there is no more data in the DDB block. This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue(A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.
Restriction	-

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.42 RDDDBC (A8H) : Read DDB Continue

A8H					RDDDBC (Read DDB Continue)					
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDDDBC	Write	1	0	1	0	1	0	0	0	(A8H)
1st Parameter	Read	DDB1[7:0]								FFh
2nd Parameter	Read	DDB2[7:0]								FFh
3rd Parameter	Read	DDB3[7:0]								FFh
4th Parameter	Read	DDB4[7:0]								FFh
5th parameter	Read	DDB5[7:0]								FFh
6th Parameter	Read	DDB6[7:0]								FFh
7th Parameter	Read	DDB7[7:0]								FFh

Description	- This command returns supplier's identification and display module model/revision information from the point where RDDDBS command was interrupt by an other command e.g. RDDDBS was interrupt after 3rd parameter (DDB3). The first parameter (DDB1), what RDDDBC is returning, is DDB4[7:0]. See also section "6.2.36 Read DDB Start (A1h)".
Restriction	-
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out, Display On</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>

6.2.43 RDFCS (AAH) : Read First Checksum

AAH	RDFCS (Read First Checksum)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDFCS	Write	1	0	1	0	1	0	1	0	(AAH)
1st Parameter	Read	FCS[7:0]								00h

Description	- Read the first checksum that has been calculated from user commands after write access to these commands has been done.
Restriction	-only in sleep out mode
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.44   RDCCS (AFH) : Read Continue Checksum

AFH	RDCCS (Read Continue Checksum)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDCCS	Write	1	0	1	0	1	1	1	1	(AFH)
1st Parameter	Read	CCS[7:0]								00h

Description	-Read the continue checksum that has been calculated continuously after the first checksum has calculated from user commands after write access to these commands has been done.
Restriction	-
Register Availability	

Status	Availability
Sleep Out, Display On	Yes
Sleep In	Yes

6.2.45 RDICID (F4H) : Read Sitronix IC ID

F4H	RDICID (Read Sitronix IC ID Code)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
RDICID	Write	1	1	1	1	0	1	0	0	(F4H)
1st Parameter	Read	0	1	1	1	0	0	0	1	71h
2nd Parameter	Read	0	0	1	0	0	0	1	1	23h

Description	- Read Sitronix IC ID Code	
Restriction	-	
Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

6.2.46   MIPIEXTFMAT (F9H) : MIPI Extension Format

F9H	MIPIEXTFMAT (MIPI Extension Format)								
Inst / Para	Write/Read	D7	D6	D5	D4	D3	D3	D1	D0	(Default)
MIPIEXTFMAT	Write	1	1	1	1	1	0	0	1	(F9H)
1st Parameter	Write	0	0	0	0	0	0	PIXEL_EXTEN[1:0]		00h

Description	-The PIXEL_EXTEN is used for pixel extension format.			
	PIXEL_EXTEN[1:0]	**5-6-5 Format**	**6-6-6 Format**	**8-8-8 Format**
	00	R[7:0] = {R[4:0] , 000b } G[7:0] = {G[5:0] , 00b } B[7:0] = {B[4:0] , 000b }	R[7:0] = {R[5:0] , 00b } G[7:0] = {G[5:0] , 00b } B[7:0] = {B[5:0] , 00b }	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
	01	R[7:0] = {R[4:0] , 111b} G[7:0] = {G[5:0] , 11b} B[7:0] = {B[4:0] , 111b}	R[7:0] = {R[5:0] , 11b} G[7:0] = {G[5:0] , 11b} B[7:0] = {B[5:0] , 11b}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
	10	R[7:0] = {R[4:0] ,R[4:2]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[4:0] , B[4:2]}	R[7:0] = {R[5:0] ,R[5:4]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[5:0] , B[5:4]}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]
	11	R[7:0] = {R[4:0] , G[5:3]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[4:0] , G[5:3]}	R[7:0] = {R[5:0] , G[5:4]} G[7:0] = {G[5:0] , G[5:4]} B[7:0] = {B[5:0] , B[5:4]}	R[7:0] = R[7:0] G[7:0] = G[7:0] B[7:0] = B[7:0]

Restriction	-

Register Availability	Status	Availability
	Sleep Out, Display On	Yes
	Sleep In	Yes

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Item	Symbol	Range	Unit
Supply Voltage (Analog)	IOVCC	- 0.3 ~ +2.1	V
Supply Voltage (I/O)	DPHYVCC	- 0.3 ~ +2.1	V
Driver Supply Voltage	AVDD-VSS	-0.3 ~ +6.6	V
Driver Supply Voltage	AVEE-VSS	- 6.6 ~ +0.3	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	0.5 ~ DPHYVCC + 0.5	V
Logic Output Voltage Range	VO	0.5 ~ DPHYVCC + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

7.2 DC Characteristics

7.2.1 Basic Characteristics

Parameter	Symbol	Condition	Specification			Unit	Note
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
Power supply Voltage	IOVCC		1.65	1.8	1.95	V	
	DPHYVCC		1.65	1.8	1.95	V	
	AVDD		4.5	5.5	6.5	V	
	AVEE		4.5	5.5	6.5	V	
Gate Driver High Voltage	VGH		7.3		20	V	Note 2
Gate Driver Low Voltage	VGL		-5.3		-18	V	
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Input Leakage Current	IIL	VIN=VDDI/VSS	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM		-2.75		-0.2	V	
Source Driver							
Gamma Amplitude (Positive)	VGPAMP		3		6	V	
Gamma Amplitude (Negative)	VGNAMP		-6		-3	V	
Feed through voltage	VFT		0		1.2	V	

Notes:

1. TA= -30 to 70℃ (to +85℃ no damage).

2. When evaluating the maximum and minimum of VGH/VGL. IOVCC/AVDD/AVEE is typical value.

7.2.2 Current Consumption

(Ta = 25℃)

Parameter	Symbol	Test Condition	Specification			Unit
			MIN.	TYP.	MAX.	
Power supply voltage	IOVCC = 1.8	Deep standby mode No load on panel	-	TBD		uA
	AVDD = 5.5		-	TBD		uA
	AVEE = -5.5		-	TBD		uA
	IOVCC = 1.8	Sleep in mode No load on panel	-	TBD		mA
	AVDD = 5.5		-	TBD		mA
	AVEE = -5.5		-	TBD		mA

7.2.3 MIPI DC Characteristic
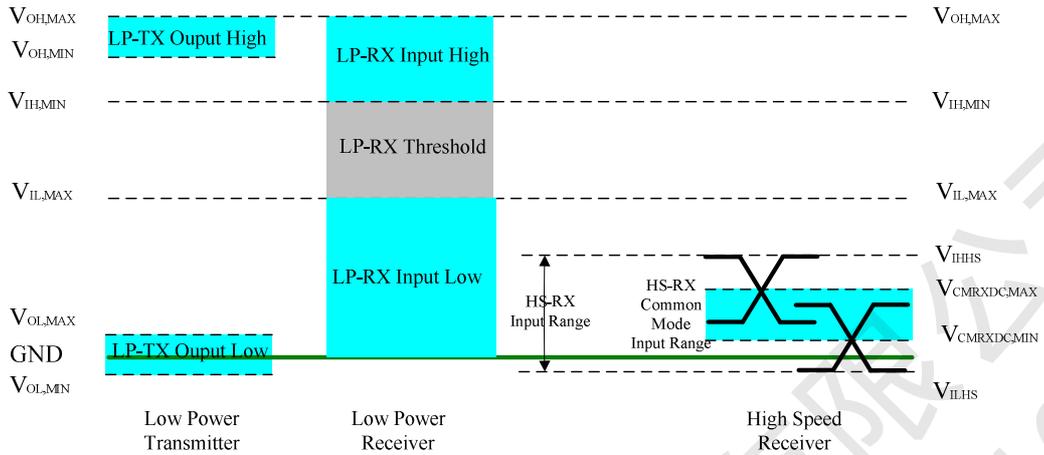
Figure 77 MIPI Signaling Voltage Levels

Parameter	Symbol	Specification			Unit
		MIN	**TYP**	**MAX**	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	VLPH	-	-	-	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	VILHS	-40	-	-	mV
Single-ended input high voltage	VIHHS	-	-	460	mV
Common-mode voltage	VCMRXDC	70	-	330	mV
Differential input impedance	ZID	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	-	1350	mV
Logic 0 input threshold	VIL	0	-	550	mV
Logic 1 input threshold	VIH	880	-	-	mV
Output low level	VOL	-50	-	50	mV
Output high level	VOH	1.1	1.2	1.3	V

7.3 AC Characteristics

7.3.1 MIPI Timing
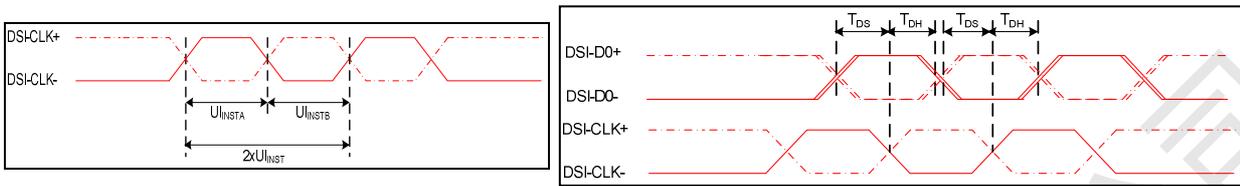
Figure 78 High Speed Mode – Clock Channel Timing

Signal	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	1.6	-	10	ns	
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous half	0.8	-	5	ns	
fDSI-CLK+/-	F_{DSICLK}	DSI-CLK+/- frequency	100	-	625	MHz	
DSI-Dn+/-	T_{DS}	Data to clock setup time	0.15	-	-	UI	
DSI-Dn+/-	T_{DH}	Data to clock hold time	0.15	-	-	UI	
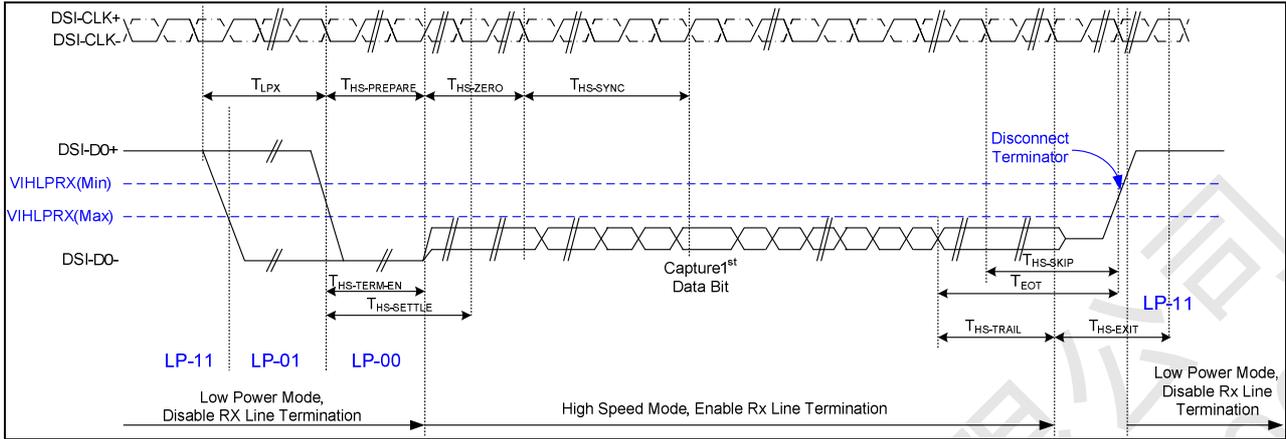
Figure 79 High-Speed Data Transmission

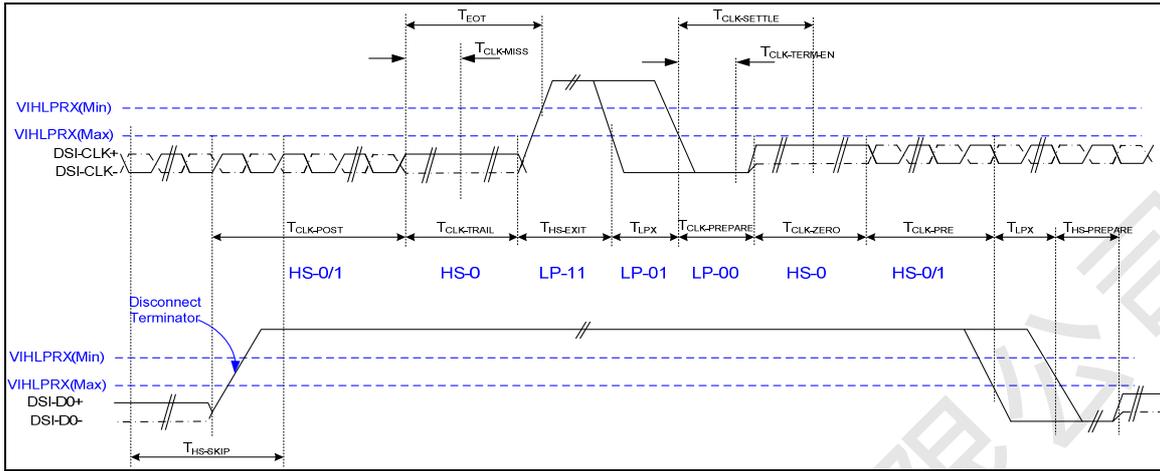| Parameter	Symbol	Specification			Unit
		MIN	**TYP**	**MAX**	
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40	-	145+10UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns
Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPAR}$	$T_{CLK-SETTLE}$	95	-	300	ns
Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPAR}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	$T_{HS-SETTLE}$	85+6UI	-	145+10UI	ns

Figure 80 Switching the Clock Lane between Clock Transmission and Low-Power Mode

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

Note: 3-Lane = $(1000 / f_{mipi} * 8 * 52 - T_{HS\_TRAIL} - 60) / (1000/f_{mipi})$

   4-Lane = $(1000 / f_{mipi} * 8 * 39 - T_{HS\_TRAIL} - 60) / (1000/f_{mipi})$

   Example: 3-Lane, 600Mbps : $n = (1000 / 600 * 8 * 52 - T_{HS\_TRAIL} - 60) / (1000/600) = 340$

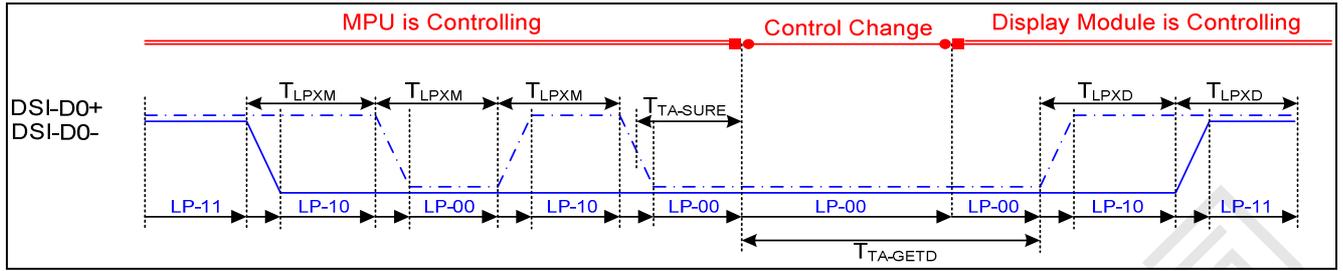   4-Lane, 600Mbps : $n = (1000 / 600 * 8 * 39 - T_{HS\_TRAIL} - 60) / (1000/600) = 236$

Figure 81 Bus Turn-around Procedure

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Length of any Low-Power state period : Master side	T_{LPX}	50	-	75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	47.5	-	52.5	ns
Ratio of T_{LPX} (MASTER)/ T_{LPX} (SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}	-	$2 T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	$5 T_{LPX}$	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	$4 T_{LPX}$	-	ns

7.3.2 MIPI Interface Timing

Parameter	Symbol	Min.	Typ..	Max.	Unit
Horizontal Sync. Width	HPW	2	-	-	Byte Clock
Horizontal Sync. Back Porch	HBP	2	-	-	Byte Clock
Horizontal Sync. Front Porch	HFP	4	-	-	Byte Clock
Vertical Sync. Width	VSW	2	-	-	Line
Vertical Sync. Back Porch	VBP	2	-	-	Line
Vertical Sync. Front Porch	VFP	4	-	-	Line
Vertical Frequency		-	60	-	Hz

7.3.3 I2C timing
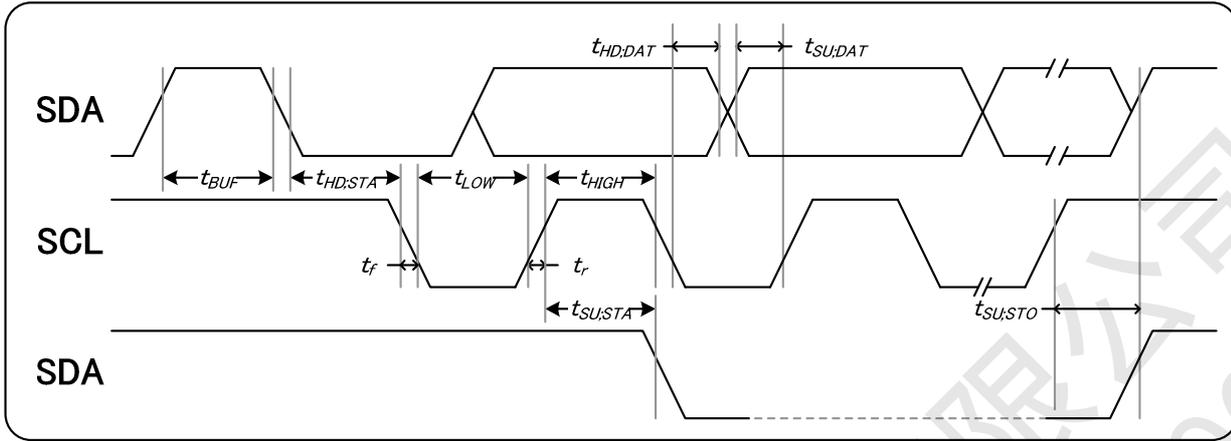
Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
SCL clock frequency		fSCL		-	400	kHZ
SCL clock low period	SCL	tLOW		1300	-	ns
SCL clock high period		tHIGH		1300	-	
Data set-up time	SDA	tSU;Data		100	-	
Data hold time		tHD;Data		0	-	
Setup time for a repeated START condition		tSU;STA		600	-	
Start condition hold time	SDA	tHD;STA		600	-	
Setup time for STOP condition		tSU;STO		600	-	
Bus free time between a STOP and START		tBUF		1300	-	

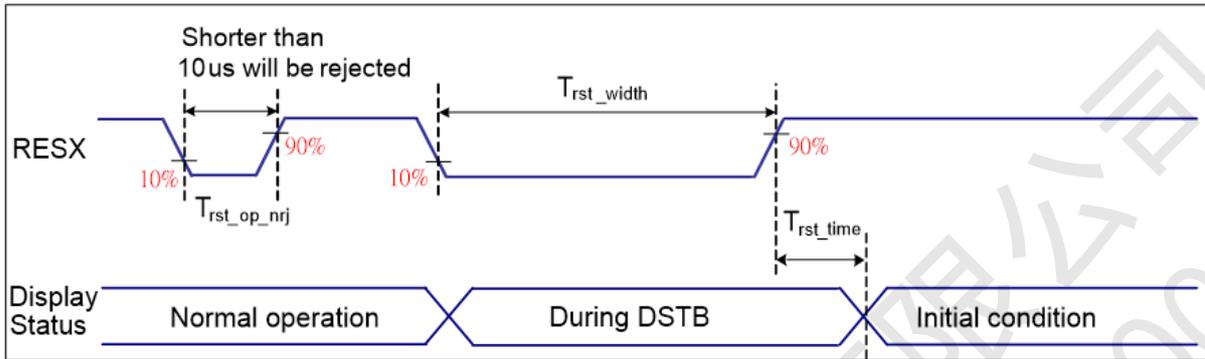### 7.3.4 Reset Timing

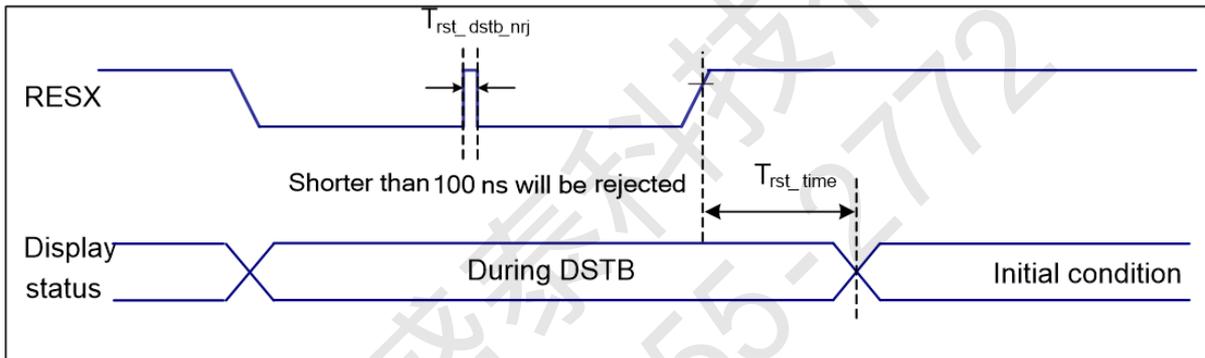**Figure 82 Reset Operation**

Figure 83 Reset Noise Rejected Diagram

Reset Timing Characteristics IOVCC=1.65~1.95v Ta=25℃

Parameter	Symbol	Specification			Unit
		Min.	Typ.	Max.	
Reset low width	Trst_width	1	-	-	ms
Reset time	Trst_time	10	-	-	ms
OP noise reject	Trst_op_nrj	-	-	10	us
DSTB Noise reject	Trst_dstb_nrj	-	-	100	ns

- During the reset period, the display will be blanked, then return to default condition for IC initialization

- It is necessary to wait 2ms after releasing HWRST pin before sending commands.

7.3.5 Abnormal Timing:

ST7123 provides abnormal power drop detection function, but there has a premise that external power must drop at low ramp, or the discharge function will not work. The following diagram is show how much time that external power drop from 90% to 10% is suitable.
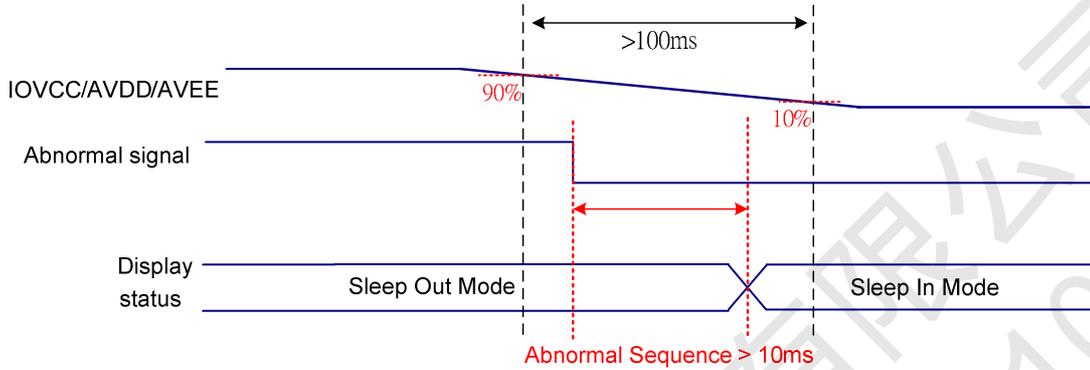


Figure 84 Reset Noise Rejected Diagram

Reset Timing Characteristics IOVCC=1.8v, AVDD=5.8v, AVEE=-5.8v Ta=25℃

External power	Power drop time from 90% to 10%			Unit
	Min.	Typ.	Max.	
IOVCC	100			ms
AVDD	100			ms
AVEE	100			ms

Note: Due to IOVCC is critical for whole chip, keep IOVCC as stable as possible.

7.3.6 Feed through voltage compensation

ST7123 provides VCOM=GND mode and DC VCOM mode to compensate feed through voltage
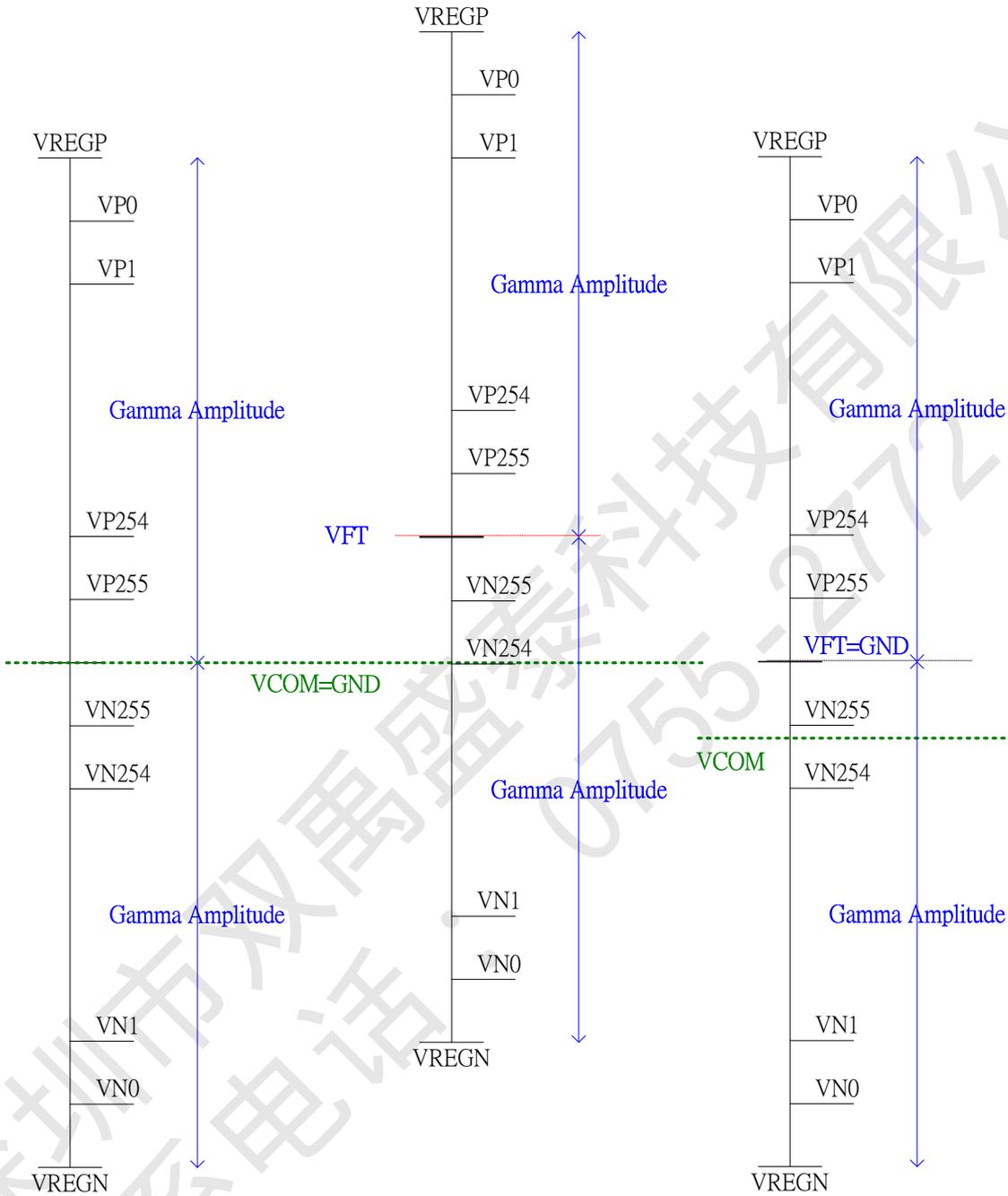
8   REVISION HISTORY

Version	Date	Description
V0.1	2019/06	**First issue**
V0.2	2021/01	**Add block diagram and pin description**
V0.3	2021/05	**Fix type error in user command set.**
V0.4	2021/07	1. **Modify positive and negative power supply rang, p.7.** 2. **Modify operating temperature range, p.8.**
V0.5	2021/09	**Modify pin definition: pad 760~763, pad 774~777, p.20**