StamPLC IO I2C Protocol

0x01 (FW Version)

6/16/2026

REG MAP (Addr:0X20-0x2F)		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	note
INA226 Data	0x00 R	V_CH1 LSB (0x00)	V_CH1 MSB (0x01)	I_CH1 Byte0 (0x02)	I_CH1 Byte1 (0x03)	I_CH1 Byte2 (0x04)	I_CH1 Byte3 (0x05)	V_CH2 LSB (0x06)	V_CH2 MSB (0x07)	I_CH2 byte0 (0x08)	I_CH2 byte1 (0x09)	I_CH2 byte2 (0x0A)	I_CH2 byte3 (0x0B)					1. Voltage and current of INA226 channels 1 and 2, in mV and uA respectively. This register is read-only. 2. Configuration takes time to take effect; after writing, the register must be read to verify the data's validity.
IO Control	0x10 W/R	IO Control (0x10)																IO Control: bit0 ex_ctr_1; bit1 ex_ctr_2; bit2 ch1_pu_en; bit3 ch2_pu_en; bit4 relay_trig_0; all are 1 for high level and 0 for low level. bit5 mode_select 0 = IO mode (controlled by bits 0-1), 1 = PWM mode (controlled by registers 0x30-0x34)
INA226 Config	0x20 W/R	CH1 INA226 Config LSB (0x20)	CH1 INA226 Config MSB (0x21)	CH2 INA226 Config LSB (0x22)	CH1 INA226 Config MSB (0x23)													This register is a mapping of INA226 register 00H. See the INA226 manual for details on AVG/VBUSCT/VSHCT Bit Setting (bits 3-11). It can be used to configure the sampling time and averaging count. Other bits are readable and writable, but are protected and read-only.
Time config	0x30 W/R	Freq	Duty1_Low	Duty1_High	Duty2_Low	Duty2_High												Freq: Timer frequency 1~100Hz (default: 50) Duty: Duty cycle (per mille) 0~1000 (default: 0)
SYS	0xF0 R												SysStatus (0xFB)			Firmware (0xFE)	I2C Addr (0xFF)	SysStatus: bit0=1, Channel 1 INA226 initialization error; bit0=0, Channel 1 INA226 initialization normal; bit1=1, Channel 2 INA226 initialization error; bit1=0, Channel 2 INA226 initialization normal. Firmware: Firmware version. I2C Addr: When the STM32 is running, reading bits 0-6 of register 0xFF can obtain the 7-bit address set by the DIP switch. Writing the desired 7-bit address to bits 0-6 (used to verify that the user's desired I2C address matches the I2C address read by the DIP switch, and does not change the read values of bits 0-6), writing 1 to bit7 refreshes the setting, and the I2C address will be updated (bit7 is automatically cleared).

I2C address corresponding to the DIP switch				
I2C ADDR SW	0	1	2	3
0x20	OFF	OFF	OFF	OFF
0x21	ON	OFF	OFF	OFF
0x22	OFF	ON	OFF	OFF
0x23	ON	ON	OFF	OFF
0x24	OFF	OFF	ON	OFF
0x25	ON	OFF	ON	OFF
0x26	OFF	ON	ON	OFF
0x27	ON	ON	ON	OFF
0x28	OFF	OFF	OFF	ON
0x29	ON	OFF	OFF	ON
0x2A	OFF	ON	OFF	ON
0x2B	ON	ON	OFF	ON
0x2C	OFF	OFF	ON	ON
0x2D	ON	OFF	ON	ON
0x2E	OFF	ON	ON	ON
0x2F	ON	ON	ON	ON