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ILI9342E

a-Si TFT LCD Single Chip Driver 320RGBx240 Resolution and 262K color

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1. Introduction

ILI9342E is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with maximum resolution of 320RGBx240 dots, comprising a 960-channel source driver, a 240-channel gate driver, 172,800 bytes GRAM for graphic display data of 320RGBx240 dots, and power supply circuit.

ILI9342E supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/8-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The ILI9342E also can configure functions via the MIPI[1] DSI[2] Interface; transmit video data via MIPI DSI Interface. The ILI9342E supports three kinds of data types, 16-bit, 18-bit and 24-bit, for video image display in MIPI DSI interfaces. In the MIPI DSI high-speed mode, the ILI9342E provides user-selectable hardware structures：One data lane supports up to 180Mbps on the MIPI DSI link.

ILI9342E supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9342E an ideal LCD driver for medium or small size portable products such as digital cellular phones, industrial control and automation, MP3 and PMP where long battery life is a major concern.

[1] *MIPI: Mobile Industry Processor Interface*

[2] *DSI: Display Serial Interface*

2. Features

- Display resolution
  - Channel Selection
    (1) 320RGB X 240
    (2) 240RGB X 240
  - Others Selection
    (1) Max：320RGB X 240；min：128RGB X 128
    (2) Source：320RGB to 128RGB , 2XRGB/step
    (3) Gate：240 to 128 , 2H/step
- Output:
  - 960 source outputs
  - 240 gate outputs
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-Ⅰ/8080-Ⅱ series MCU
  - 6-bits, 8-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
  - 1-lane MIPI DSI interface
- Display mode(selectable color depth mode by software):
  - Full color mode (Idle mode OFF): 262,144-color at maximum
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - Oscillator
  - DC/DC converter
  - Dot/Column inversion
  - 1 preset Gamma curves
- Dynamic backlight control
- OTP :
  - 8-bits for ID1, ID2, ID3 (Support OTP 2 times)
  - MADCTL (MY/MX/MV/ML/RGB) (Support OTP 2 times)
  - Positive/Negative Gamma Setting (Support OTP 1 time)
  - 7-bits for VCOM adjustment (Support OTP 3 times)
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.6V (logic)
    - VCI = 2.5V ~ 3.6V (analog)
- LCD Voltage drive:
  - Source output voltage range
    - VSP - GND = 6.2V ~ 6.7V (0.1V/step)
    - VSN - GND = -4.4V ~ -4.9V (0.1V/step)
  - Gate driver output voltage
    - VGH - GND = 10.5V ~ 15.0V (0.5V/step)
    - VGL - GND = -6.0V ~ -10.5V (0.5V/step)
    - VGH - VGL ≦ 30.0V
  - VCOM driver output voltage
    - VCOM = 0 V
- Operate temperature range: -30℃ to 70℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Device Overview

3.1. Block Diagram

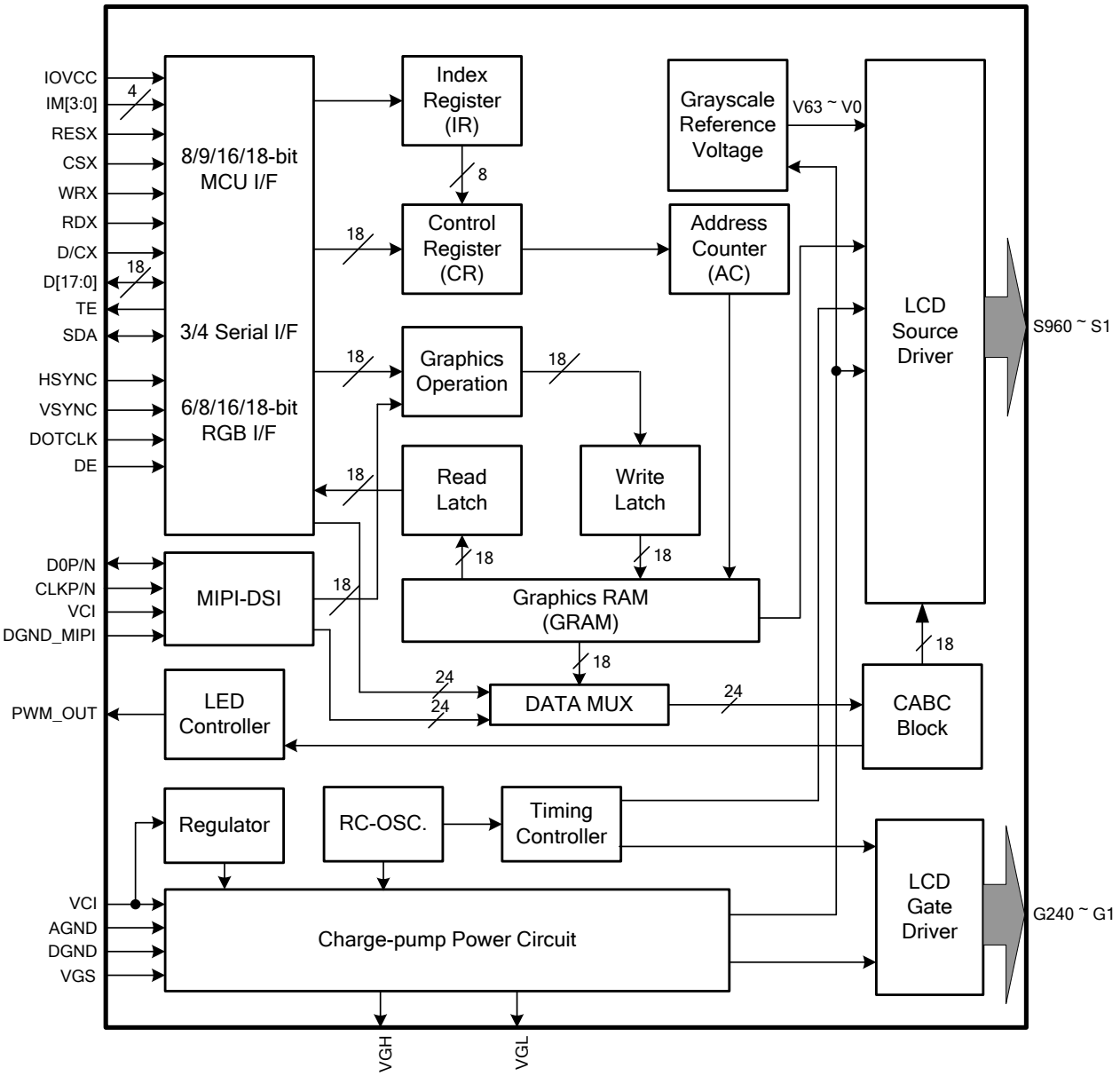


Figure 1: Block Diagram

3.2. Pin Descriptions

Table 1: Pin Definition

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td colspan="4">Interface Logic Signals</td></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(IOVCC/GND)</td><td>- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>80 MCU 16-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>80 MCU 9-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 16-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:10] D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:10],</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 9-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>MIPI 1 lane</td><td>MIPI Data/Clock</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>MIPI 1 lane – P/N swap</td><td>MIPI Data/Clock</td><td></td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
Fix this pin at IOVCC or GND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU (IOVCC/GND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU (IOVCC/GND)</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” in MPU interface mode only.
* note1,2
Fix to IOVCC level when not in use.</td></tr>
<tr><td>DCX_SCL</td><td>I</td><td>MCU (IOVCC/GND)</td><td>(D/CX) This pin is used to select “Data or Command” in the parallel interface.
When D/CX = ’1’, data is selected.
When D/CX = ’0’, command is selected.
(SCL) This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
Fix to IOVCC or GND level when not in use.</td></tr>
<tr><td>RDX</td><td>I</td><td>MCU (IOVCC/GND)</td><td>8080-Ⅰ/ 8080-Ⅱ system (RDX) : Serves as a read signal and MCU read data at the rising edge.
Fix to IOVCC level when not in use.</td></tr>
</table>

WRX (D/CX)	I	MCU (IOVCC/GND)	8080-Ⅰ / 8080-Ⅱ system (WRX) : Serves as a write signal and writes data at the rising edge. 4-line system (D/CX): Serves as command or parameter select. ***Fix to IOVCC level when not in use.***
D[17:0]	I/O	MCU (IOVCC/GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode ***Fix to GND level when not in use***
SDA	I/O	MCU (IOVCC/GND)	When IM[3] : High, Serial in/out signal. The data is applied on the rising edge of the DCX_SCL signal. ***Fix this pin at IOVCC or GND when not in use.***
TE	O	MCU (IOVCC/GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. ***Leave it open when not in use.***
TE1	O	MCU (IOVCC/GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. TE1 is equal to TE. ***Leave it open when not in use.***
PWM_OUT	O	IOVCC	Output pin for PWM (Pulse Width Modulation) signal of LED driving. ***Leave the pin to open when not in use.***
PWM_OUT1	O	IOVCC	Output pin for PWM (Pulse Width Modulation) signal of LED driving. PWM_OUT1 is equal to PWM_OUT. ***Leave the pin to open when not in use.***
DOTCLK	I	MCU (IOVCC/GND)	Dot clock signal for RGB interface operation. ***Fix to IOVCC or GND level when not in use.***
VSYNC	I	MCU (IOVCC/GND)	Frame synchronizing signal for RGB interface operation. ***Fix to IOVCC or GND level when not in use.***
HSYNC	I	MCU (IOVCC/GND)	Line synchronizing signal for RGB interface operation. ***Fix to IOVCC or GND level when not in use.***
DE	I	MCU (IOVCC/GND)	Data enable signal for RGB interface operation. ***Fix to IOVCC or GND level when not in use.*** ***Fix to GND level when use RGB interface SYNC mode.***
CLKP CLKN	I	LVDSVDD	- MIPI DSI differential clock pair ***Leave it open or fix to DGND_MIPI level when not in use.***
D0P D0N	I/O	LVDSVDD	- MIPI DSI differential data pair. (Data lane 0) ***Leave it open or fix to DGND_MIPI level when not in use.***
Power Supply Pins			
IOVCC	I	Power Supply	Power supply for interface logic circuits. Connect to an external power supply of 1.65V to 3.6V.
VCI	I	Power Supply	Power supply for analog circuit. Connect to an external power supply of 2.5V to 3.6V.
AGND	I	Ground	System ground for the analog circuit. ***In the case of COG, connect to GND on the FPC to prevent noise.***

DGND	I	Ground	System ground for digital circuit. ***In the case of COG, connect to GND on the FPC to prevent noise.***
VGS	I	Groung	System ground for the analog circuit. ***In the case of COG, connect to GND on the FPC to prevent noise.***
DGND_MIPI	I	Ground	System ground for MIPI DSI ground. ***In the case of COG, connect to GND on the FPC to prevent noise.***
VPP	I	Power Supply	Input power for OTP programming. VPP=8. 5V ***Leave VPP pin to open when not under programming.***
LCD Driver Output Pins			
S960~S1	O	Source	Source output signals. ***Leave the pin to open when not in use.***
G240~G1	O	Gate	Gate output signals. ***Leave the pin to open when not in use.***
VGH	O	Analog	Output positive voltage from step-up circuit for the liquid crystal panel.
VGL	O	Analog	Output negative voltage from step-up circuit for the liquid crystal panel.
Test / Dummy Pins			
RESX1	I	MCU (IOVCC/GND)	RESX1 is an invalid pin. ***Leave the pin to open.***
CSX1	I	MCU (IOVCC/GND)	CSX1 is an invalid pin. ***Leave the pin to open.***
DCX_SCL1	I	MCU (IOVCC/GND)	DCX_SCL1 is an invalid pin. ***Leave the pin to open.***
TEST_EN TESTOSC	I	IOVCC	TEST pin. ***Leave the pin to open.***
TEST0~8	I	IOVCC	TEST pin. ***Leave the pin to open.***
TESTO1~O2	I/O	IOVCC	TEST pin. ***Leave the pin to open.***
GPIO0~7	I/O	IOVCC	TEST pin. ***Leave the pin to open.***
MIPI_TEST	O	Analog	MIPI Test Pins. ***Leave the pin to open.***
VCORE_TEST	O	Analog	Vcore Test Pins. ***Leave the pin to open.***

VSP_DC_TEST	O	Analog	VSP DC Test Pins. ***Leave the pin to open.***
VSN_DC_TEST	O	Analog	VSN DC Test Pins. ***Leave the pin to open.***
VAP_TEST	O	Analog	VAP Test Pins. ***Leave the pin to open.***
VAN_TEST	O	Analog	VAN Test Pins. ***Leave the pin to open.***
VSP_AC_TEST	O	Analog	VSP AC Test Pins. ***Leave the pin to open.***
VSN_AC_TEST	O	Analog	VSN AC Test Pins. ***Leave the pin to open.***
DUMMYR1 DUMMYR2 DUMMYR3 DUMMYR4	-	Open	Dummy Pin ***Leave the pin to open***
DUMMY	-	Open	Dummy Pin ***Leave the pin to open***

3.3. Liquid crystal power supply specifications table

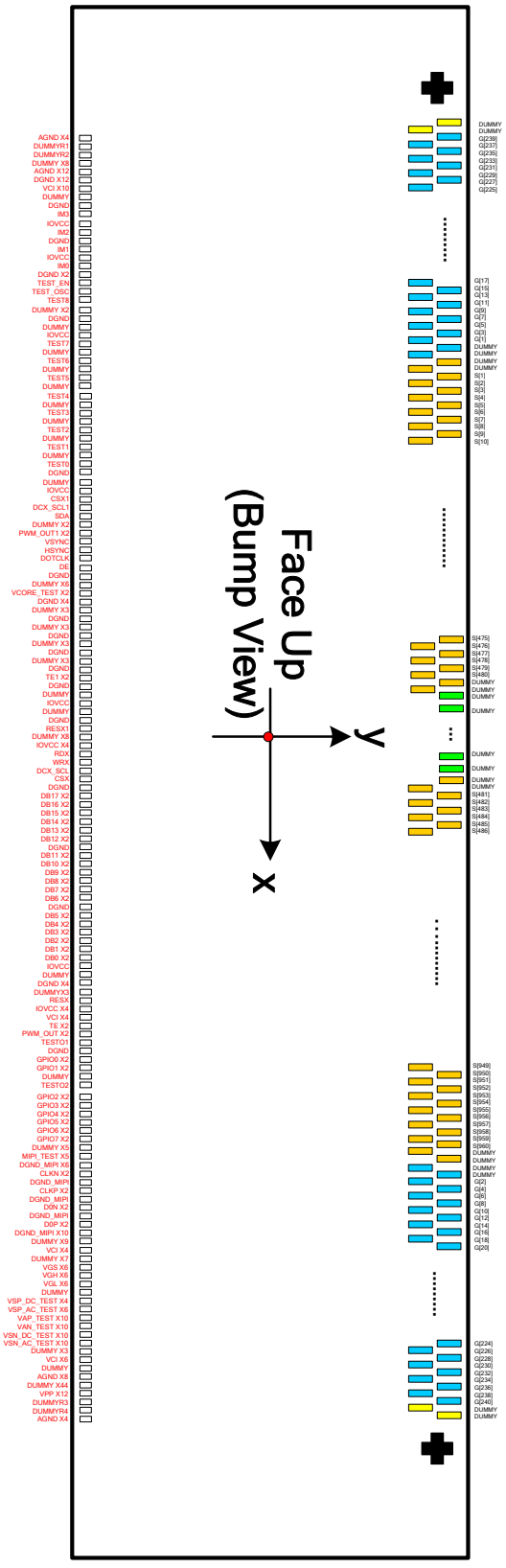
No.	Item		Description
1	TFT Source Driver		960 pins (320 x RGB)
2	TFT Gate Driver		240 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S960	V0 ~ V63 grayscales
		G1 ~ G240	VGH - VGL
5	Input Voltage	IOVCC	1.65V ~3.6V
		VCI	2.5V ~ 3.6V
6	Liquid Crystal Drive Voltages	VSP	6.2V ~ 6.7V
		VSN	-4.4V ~ -4.9V
		VGH	10.5V ~ 15.0V
		VGL	-6.0V ~ -10.5V
		VGH - VGL	Max. 30.0V

3.4. Pad Arrangement and Coordination

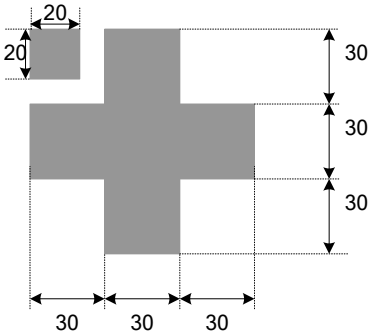
Chip Size: 18620um x 690um (scribe line included)
Chip thickness : 250um (typ.)
Pad Location: Pad Center.
Coordinate Origin: Chip center: (0.-3.5)
Leftest & down coordinate : (-9310,-348.5)
Rightest & up coordinate : (9310, 341.5)
Au bump height: 12um (typ.)
Au Bump Size:

1. 24um x 69um
   input side :
   No. 1 ~ 436

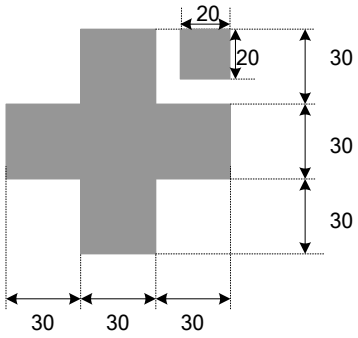
2. 14um x 90um
   Staggered LCD output side :
   No. 437 ~ 1672



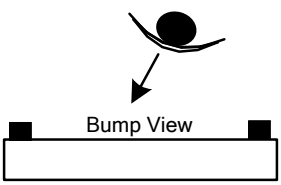
Alignment Marks



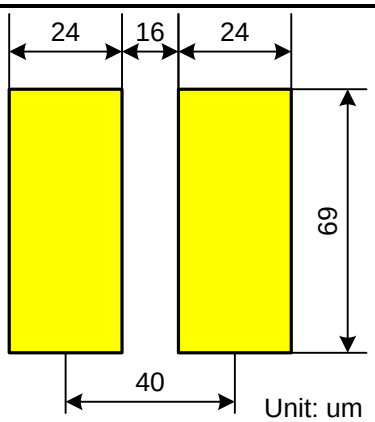
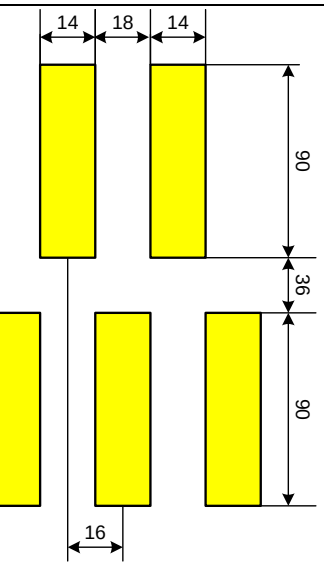
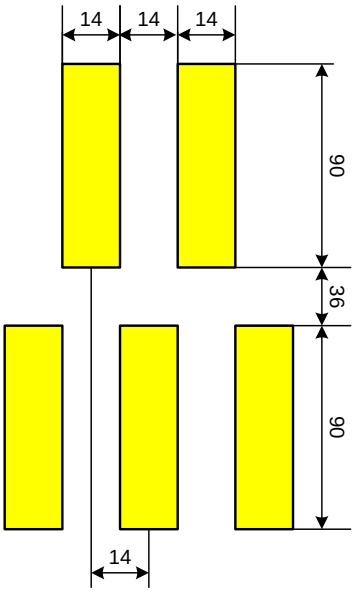
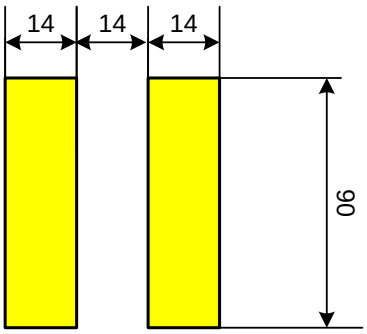
Alignment Mark: A1
(-9200, 225)



Alignment Mark: A2
(9200,225)



3.5. Bump Size and Pitch

Input Pad (NO.1 ~ NO.436)	
Output Pad (NO.437 ~ NO.1672)	 No. 437 ~ No. 561 No.1549 ~ No.1672 Unit: um  No. 562 ~ No.1045 No.1065 ~ No.1548  No.1046 ~ No.1054 No.1055 ~ No.1064 Unit: um

3.6. Pad Coordination

No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
1	AGND	-8989	-245.5	61	TESTOSC	-6589	-245.5	121	DGND	-4189	-245.5	181	DB3	-1789	-245.5
2	AGND	-8949	-245.5	62	TEST8	-6549	-245.5	122	DUMMY	-4149	-245.5	182	DB3	-1749	-245.5
3	AGND	-8909	-245.5	63	DUMMY	-6509	-245.5	123	DUMMY	-4109	-245.5	183	DB2	-1709	-245.5
4	AGND	-8869	-245.5	64	DUMMY	-6469	-245.5	124	DUMMY	-4069	-245.5	184	DB2	-1669	-245.5
5	DUMMYR1	-8829	-245.5	65	DGND	-6429	-245.5	125	DGND	-4029	-245.5	185	DB1	-1629	-245.5
6	DUMMYR2	-8789	-245.5	66	DUMMY	-6389	-245.5	126	TE1	-3989	-245.5	186	DB1	-1589	-245.5
7	DUMMY	-8749	-245.5	67	IOVCC	-6349	-245.5	127	TE1	-3949	-245.5	187	DB0	-1549	-245.5
8	DUMMY	-8709	-245.5	68	TEST7	-6309	-245.5	128	DGND	-3909	-245.5	188	DB0	-1509	-245.5
9	DUMMY	-8669	-245.5	69	DUMMY	-6269	-245.5	129	DUMMY	-3869	-245.5	189	IOVCC	-1469	-245.5
10	DUMMY	-8629	-245.5	70	TEST6	-6229	-245.5	130	IOVCC	-3829	-245.5	190	DUMMY	-1429	-245.5
11	DUMMY	-8589	-245.5	71	DUMMY	-6189	-245.5	131	DUMMY	-3789	-245.5	191	DGND	-1389	-245.5
12	DUMMY	-8549	-245.5	72	TEST5	-6149	-245.5	132	DGND	-3749	-245.5	192	DGND	-1349	-245.5
13	DUMMY	-8509	-245.5	73	DUMMY	-6109	-245.5	133	RESX1	-3709	-245.5	193	DGND	-1309	-245.5
14	DUMMY	-8469	-245.5	74	TEST4	-6069	-245.5	134	DUMMY	-3669	-245.5	194	DGND	-1269	-245.5
15	AGND	-8429	-245.5	75	DUMMY	-6029	-245.5	135	DUMMY	-3629	-245.5	195	DUMMY	-1229	-245.5
16	AGND	-8389	-245.5	76	TEST3	-5989	-245.5	136	DUMMY	-3589	-245.5	196	DUMMY	-1189	-245.5
17	AGND	-8349	-245.5	77	DUMMY	-5949	-245.5	137	DUMMY	-3549	-245.5	197	DUMMY	-1149	-245.5
18	AGND	-8309	-245.5	78	TEST2	-5909	-245.5	138	DUMMY	-3509	-245.5	198	RESX	-1109	-245.5
19	AGND	-8269	-245.5	79	DUMMY	-5869	-245.5	139	DUMMY	-3469	-245.5	199	IOVCC	-1069	-245.5
20	AGND	-8229	-245.5	80	TEST1	-5829	-245.5	140	DUMMY	-3429	-245.5	200	IOVCC	-1029	-245.5
21	AGND	-8189	-245.5	81	DUMMY	-5789	-245.5	141	DUMMY	-3389	-245.5	201	IOVCC	-989	-245.5
22	AGND	-8149	-245.5	82	TEST0	-5749	-245.5	142	IOVCC	-3349	-245.5	202	IOVCC	-949	-245.5
23	AGND	-8109	-245.5	83	DGND	-5709	-245.5	143	IOVCC	-3309	-245.5	203	VCI	-909	-245.5
24	AGND	-8069	-245.5	84	DUMMY	-5669	-245.5	144	IOVCC	-3269	-245.5	204	VCI	-869	-245.5
25	AGND	-8029	-245.5	85	IOVCC	-5629	-245.5	145	IOVCC	-3229	-245.5	205	VCI	-829	-245.5
26	AGND	-7989	-245.5	86	CSX1	-5589	-245.5	146	RDX	-3189	-245.5	206	VCI	-789	-245.5
27	DGND	-7949	-245.5	87	DCX_SCL1	-5549	-245.5	147	WRX	-3149	-245.5	207	TE	-749	-245.5
28	DGND	-7909	-245.5	88	SDA	-5509	-245.5	148	DCX_SCL	-3109	-245.5	208	TE	-709	-245.5
29	DGND	-7869	-245.5	89	DUMMY	-5469	-245.5	149	CSX	-3069	-245.5	209	PWM_OUT	-669	-245.5
30	DGND	-7829	-245.5	90	DUMMY	-5429	-245.5	150	DGND	-3029	-245.5	210	PWM_OUT	-629	-245.5
31	DGND	-7789	-245.5	91	PWM_OUT1	-5389	-245.5	151	DB17	-2989	-245.5	211	TESTO1	-589	-245.5
32	DGND	-7749	-245.5	92	PWM_OUT1	-5349	-245.5	152	DB17	-2949	-245.5	212	DGND	-549	-245.5
33	DGND	-7709	-245.5	93	VSYNC	-5309	-245.5	153	DB16	-2909	-245.5	213	GPIO0	-509	-245.5
34	DGND	-7669	-245.5	94	HSYNC	-5269	-245.5	154	DB16	-2869	-245.5	214	GPIO0	-469	-245.5
35	DGND	-7629	-245.5	95	DOTCLK	-5229	-245.5	155	DB15	-2829	-245.5	215	GPIO1	-429	-245.5
36	DGND	-7589	-245.5	96	DE	-5189	-245.5	156	DB15	-2789	-245.5	216	GPIO1	-389	-245.5
37	DGND	-7549	-245.5	97	DGND	-5149	-245.5	157	DB14	-2749	-245.5	217	DUMMY	-349	-245.5
38	DGND	-7509	-245.5	98	DUMMY	-5109	-245.5	158	DB14	-2709	-245.5	218	TESTO2	-309	-245.5
39	VCI	-7469	-245.5	99	DUMMY	-5069	-245.5	159	DB13	-2669	-245.5	219	GPIO2	309	-245.5
40	VCI	-7429	-245.5	100	DUMMY	-5029	-245.5	160	DB13	-2629	-245.5	220	GPIO2	349	-245.5
41	VCI	-7389	-245.5	101	DUMMY	-4989	-245.5	161	DB12	-2589	-245.5	221	GPIO3	389	-245.5
42	VCI	-7349	-245.5	102	DUMMY	-4949	-245.5	162	DB12	-2549	-245.5	222	GPIO3	429	-245.5
43	VCI	-7309	-245.5	103	DUMMY	-4909	-245.5	163	DGND	-2509	-245.5	223	GPIO4	469	-245.5
44	VCI	-7269	-245.5	104	VCORE_TEST	-4869	-245.5	164	DB11	-2469	-245.5	224	GPIO4	509	-245.5
45	VCI	-7229	-245.5	105	VCORE_TEST	-4829	-245.5	165	DB11	-2429	-245.5	225	GPIO5	549	-245.5
46	VCI	-7189	-245.5	106	DGND	-4789	-245.5	166	DB10	-2389	-245.5	226	GPIO5	589	-245.5
47	VCI	-7149	-245.5	107	DGND	-4749	-245.5	167	DB10	-2349	-245.5	227	GPIO6	629	-245.5
48	VCI	-7109	-245.5	108	DGND	-4709	-245.5	168	DB9	-2309	-245.5	228	GPIO6	669	-245.5
49	DUMMY	-7069	-245.5	109	DGND	-4669	-245.5	169	DB9	-2269	-245.5	229	GPIO7	709	-245.5
50	DGND	-7029	-245.5	110	DUMMY	-4629	-245.5	170	DB8	-2229	-245.5	230	GPIO7	749	-245.5
51	IM3	-6989	-245.5	111	DUMMY	-4589	-245.5	171	DB8	-2189	-245.5	231	DUMMY	789	-245.5
52	IOVCC	-6949	-245.5	112	DUMMY	-4549	-245.5	172	DB7	-2149	-245.5	232	DUMMY	829	-245.5
53	IM2	-6909	-245.5	113	DGND	-4509	-245.5	173	DB7	-2109	-245.5	233	DUMMY	869	-245.5
54	DGND	-6869	-245.5	114	DUMMY	-4469	-245.5	174	DB6	-2069	-245.5	234	DUMMY	909	-245.5
55	IM1	-6829	-245.5	115	DUMMY	-4429	-245.5	175	DB6	-2029	-245.5	235	DUMMY	949	-245.5
56	IOVCC	-6789	-245.5	116	DUMMY	-4389	-245.5	176	DGND	-1989	-245.5	236	MIPI_TEST	989	-245.5
57	IM0	-6749	-245.5	117	DGND	-4349	-245.5	177	DB5	-1949	-245.5	237	MIPI_TEST	1029	-245.5
58	DGND	-6709	-245.5	118	DUMMY	-4309	-245.5	178	DB5	-1909	-245.5	238	MIPI_TEST	1069	-245.5
59	DGND	-6669	-245.5	119	DUMMY	-4269	-245.5	179	DB4	-1869	-245.5	239	MIPI_TEST	1109	-245.5
60	TEST_EN	-6629	-245.5	120	DUMMY	-4229	-245.5	180	DB4	-1829	-245.5	240	MIPI_TEST	1149	-245.5

No.	Text Name	X-axis	Y-axis
241	DGND_MIPI	1189	-245.5
242	DGND_MIPI	1229	-245.5
243	DGND_MIPI	1269	-245.5
244	DGND_MIPI	1309	-245.5
245	DGND_MIPI	1349	-245.5
246	DGND_MIPI	1389	-245.5
247	CLKN	1429	-245.5
248	CLKN	1469	-245.5
249	DGND_MIPI	1509	-245.5
250	CLKP	1549	-245.5
251	CLKP	1589	-245.5
252	DGND_MIPI	1629	-245.5
253	D0N	1669	-245.5
254	D0N	1709	-245.5
255	DGND_MIPI	1749	-245.5
256	D0P	1789	-245.5
257	D0P	1829	-245.5
258	DGND_MIPI	1869	-245.5
259	DGND_MIPI	1909	-245.5
260	DGND_MIPI	1949	-245.5
261	DGND_MIPI	1989	-245.5
262	DGND_MIPI	2029	-245.5
263	DGND_MIPI	2069	-245.5
264	DGND_MIPI	2109	-245.5
265	DGND_MIPI	2149	-245.5
266	DGND_MIPI	2189	-245.5
267	DGND_MIPI	2229	-245.5
268	DUMMY	2269	-245.5
269	DUMMY	2309	-245.5
270	DUMMY	2349	-245.5
271	DUMMY	2389	-245.5
272	DUMMY	2429	-245.5
273	DUMMY	2469	-245.5
274	DUMMY	2509	-245.5
275	DUMMY	2549	-245.5
276	DUMMY	2589	-245.5
277	VCI	2629	-245.5
278	VCI	2669	-245.5
279	VCI	2709	-245.5
280	VCI	2749	-245.5
281	DUMMY	2789	-245.5
282	DUMMY	2829	-245.5
283	DUMMY	2869	-245.5
284	DUMMY	2909	-245.5
285	DUMMY	2949	-245.5
286	DUMMY	2989	-245.5
287	DUMMY	3029	-245.5
288	VGS	3069	-245.5
289	VGS	3109	-245.5
290	VGS	3149	-245.5
291	VGS	3189	-245.5
292	VGS	3229	-245.5
293	VGS	3269	-245.5
294	VGH	3309	-245.5
295	VGH	3349	-245.5
296	VGH	3389	-245.5
297	VGH	3429	-245.5
298	VGH	3469	-245.5
299	VGH	3509	-245.5
300	VGL	3549	-245.5
301	VGL	3589	-245.5
302	VGL	3629	-245.5
303	VGL	3669	-245.5
304	VGL	3709	-245.5
305	VGL	3749	-245.5
306	DUMMY	3789	-245.5
307	VSP_DC_TEST	3829	-245.5
308	VSP_DC_TEST	3869	-245.5
309	VSP_DC_TEST	3909	-245.5
310	VSP_DC_TEST	3949	-245.5
311	VSP_AC_TEST	3989	-245.5
312	VSP_AC_TEST	4029	-245.5
313	VSP_AC_TEST	4069	-245.5
314	VSP_AC_TEST	4109	-245.5
315	VSP_AC_TEST	4149	-245.5
316	VSP_AC_TEST	4189	-245.5
317	VAP_TEST	4229	-245.5
318	VAP_TEST	4269	-245.5
319	VAP_TEST	4309	-245.5
320	VAP_TEST	4349	-245.5
321	VAP_TEST	4389	-245.5
322	VAP_TEST	4429	-245.5
323	VAP_TEST	4469	-245.5
324	VAP_TEST	4509	-245.5
325	VAP_TEST	4549	-245.5
326	VAP_TEST	4589	-245.5
327	VAN_TEST	4629	-245.5
328	VAN_TEST	4669	-245.5
329	VAN_TEST	4709	-245.5
330	VAN_TEST	4749	-245.5
331	VAN_TEST	4789	-245.5
332	VAN_TEST	4829	-245.5
333	VAN_TEST	4869	-245.5
334	VAN_TEST	4909	-245.5
335	VAN_TEST	4949	-245.5
336	VAN_TEST	4989	-245.5
337	VSN_DC_TEST	5029	-245.5
338	VSN_DC_TEST	5069	-245.5
339	VSN_DC_TEST	5109	-245.5
340	VSN_DC_TEST	5149	-245.5
341	VSN_DC_TEST	5189	-245.5
342	VSN_DC_TEST	5229	-245.5
343	VSN_DC_TEST	5269	-245.5
344	VSN_DC_TEST	5309	-245.5
345	VSN_DC_TEST	5349	-245.5
346	VSN_DC_TEST	5389	-245.5
347	VSN_AC_TEST	5429	-245.5
348	VSN_AC_TEST	5469	-245.5
349	VSN_AC_TEST	5509	-245.5
350	VSN_AC_TEST	5549	-245.5
351	VSN_AC_TEST	5589	-245.5
352	VSN_AC_TEST	5629	-245.5
353	VSN_AC_TEST	5669	-245.5
354	VSN_AC_TEST	5709	-245.5
355	VSN_AC_TEST	5749	-245.5
356	VSN_AC_TEST	5789	-245.5
357	DUMMY	5829	-245.5
358	DUMMY	5869	-245.5
359	DUMMY	5909	-245.5
360	VCI	5949	-245.5
361	VCI	5989	-245.5
362	VCI	6029	-245.5
363	VCI	6069	-245.5
364	VCI	6109	-245.5
365	VCI	6149	-245.5
366	DUMMY	6189	-245.5
367	AGND	6229	-245.5
368	AGND	6269	-245.5
369	AGND	6309	-245.5
370	AGND	6349	-245.5
371	AGND	6389	-245.5
372	AGND	6429	-245.5
373	AGND	6469	-245.5
374	AGND	6509	-245.5
375	DUMMY	6549	-245.5
376	DUMMY	6589	-245.5
377	DUMMY	6629	-245.5
378	DUMMY	6669	-245.5
379	DUMMY	6709	-245.5
380	DUMMY	6749	-245.5
381	DUMMY	6789	-245.5
382	DUMMY	6829	-245.5
383	DUMMY	6869	-245.5
384	DUMMY	6909	-245.5
385	DUMMY	6949	-245.5
386	DUMMY	6989	-245.5
387	DUMMY	7029	-245.5
388	DUMMY	7069	-245.5
389	DUMMY	7109	-245.5
390	DUMMY	7149	-245.5
391	DUMMY	7189	-245.5
392	DUMMY	7229	-245.5
393	DUMMY	7269	-245.5
394	DUMMY	7309	-245.5
395	DUMMY	7349	-245.5
396	DUMMY	7389	-245.5
397	DUMMY	7429	-245.5
398	DUMMY	7469	-245.5
399	DUMMY	7509	-245.5
400	DUMMY	7549	-245.5
401	DUMMY	7589	-245.5
402	DUMMY	7629	-245.5
403	DUMMY	7669	-245.5
404	DUMMY	7709	-245.5
405	DUMMY	7749	-245.5
406	DUMMY	7789	-245.5
407	DUMMY	7829	-245.5
408	DUMMY	7869	-245.5
409	DUMMY	7909	-245.5
410	DUMMY	7949	-245.5
411	DUMMY	7989	-245.5
412	DUMMY	8029	-245.5
413	DUMMY	8069	-245.5
414	DUMMY	8109	-245.5
415	DUMMY	8149	-245.5
416	DUMMY	8189	-245.5
417	DUMMY	8229	-245.5
418	DUMMY	8269	-245.5
419	VPP	8309	-245.5
420	VPP	8349	-245.5
421	VPP	8389	-245.5
422	VPP	8429	-245.5
423	VPP	8469	-245.5
424	VPP	8509	-245.5
425	VPP	8549	-245.5
426	VPP	8589	-245.5
427	VPP	8629	-245.5
428	VPP	8669	-245.5
429	VPP	8709	-245.5
430	VPP	8749	-245.5
431	DUMMYR3	8789	-245.5
432	DUMMYR4	8829	-245.5
433	AGND	8869	-245.5
434	AGND	8909	-245.5
435	AGND	8949	-245.5
436	AGND	8989	-245.5
437	DUMMY	9035	233
438	DUMMY	9019	107
439	G240	9003	233
440	G238	8987	107
441	G236	8971	233
442	G234	8955	107
443	G232	8939	233
444	G230	8923	107
445	G228	8907	233
446	G226	8891	107
447	G224	8875	233
448	G222	8859	107
449	G220	8843	233
450	G218	8827	107
451	G216	8811	233
452	G214	8795	107
453	G212	8779	233
454	G210	8763	107
455	G208	8747	233
456	G206	8731	107
457	G204	8715	233
458	G202	8699	107
459	G200	8683	233
460	G198	8667	107
461	G196	8651	233
462	G194	8635	107
463	G192	8619	233
464	G190	8603	107
465	G188	8587	233
466	G186	8571	107
467	G184	8555	233
468	G182	8539	107
469	G180	8523	233
470	G178	8507	107
471	G176	8491	233
472	G174	8475	107
473	G172	8459	233
474	G170	8443	107
475	G168	8427	233
476	G166	8411	107
477	G164	8395	233
478	G162	8379	107
479	G160	8363	233
480	G158	8347	107

No.	Text Name	X-axis	Y-axis
481	G156	8331	233
482	G154	8315	107
483	G152	8299	233
484	G150	8283	107
485	G148	8267	233
486	G146	8251	107
487	G144	8235	233
488	G142	8219	107
489	G140	8203	233
490	G138	8187	107
491	G136	8171	233
492	G134	8155	107
493	G132	8139	233
494	G130	8123	107
495	G128	8107	233
496	G126	8091	107
497	G124	8075	233
498	G122	8059	107
499	G120	8043	233
500	G118	8027	107
501	G116	8011	233
502	G114	7995	107
503	G112	7979	233
504	G110	7963	107
505	G108	7947	233
506	G106	7931	107
507	G104	7915	233
508	G102	7899	107
509	G100	7883	233
510	G98	7867	107
511	G96	7851	233
512	G94	7835	107
513	G92	7819	233
514	G90	7803	107
515	G88	7787	233
516	G86	7771	107
517	G84	7755	233
518	G82	7739	107
519	G80	7723	233
520	G78	7707	107
521	G76	7691	233
522	G74	7675	107
523	G72	7659	233
524	G70	7643	107
525	G68	7627	233
526	G66	7611	107
527	G64	7595	233
528	G62	7579	107
529	G60	7563	233
530	G58	7547	107
531	G56	7531	233
532	G54	7515	107
533	G52	7499	233
534	G50	7483	107
535	G48	7467	233
536	G46	7451	107
537	G44	7435	233
538	G42	7419	107
539	G40	7403	233
540	G38	7387	107

No.	Text Name	X-axis	Y-axis
541	G36	7371	233
542	G34	7355	107
543	G32	7339	233
544	G30	7323	107
545	G28	7307	233
546	G26	7291	107
547	G24	7275	233
548	G22	7259	107
549	G20	7243	233
550	G18	7227	107
551	G16	7211	233
552	G14	7195	107
553	G12	7179	233
554	G10	7163	107
555	G8	7147	233
556	G6	7131	107
557	G4	7115	233
558	G2	7099	107
559	DUMMY	7083	233
560	DUMMY	7067	107
561	DUMMY	7051	233
562	DUMMY	7037	107
563	S960	7023	233
564	S959	7009	107
565	S958	6995	233
566	S957	6981	107
567	S956	6967	233
568	S955	6953	107
569	S954	6939	233
570	S953	6925	107
571	S952	6911	233
572	S951	6897	107
573	S950	6883	233
574	S949	6869	107
575	S948	6855	233
576	S947	6841	107
577	S946	6827	233
578	S945	6813	107
579	S944	6799	233
580	S943	6785	107
581	S942	6771	233
582	S941	6757	107
583	S940	6743	233
584	S939	6729	107
585	S938	6715	233
586	S937	6701	107
587	S936	6687	233
588	S935	6673	107
589	S934	6659	233
590	S933	6645	107
591	S932	6631	233
592	S931	6617	107
593	S930	6603	233
594	S929	6589	107
595	S928	6575	233
596	S927	6561	107
597	S926	6547	233
598	S925	6533	107
599	S924	6519	233
600	S923	6505	107

No.	Text Name	X-axis	Y-axis
601	S922	6491	233
602	S921	6477	107
603	S920	6463	233
604	S919	6449	107
605	S918	6435	233
606	S917	6421	107
607	S916	6407	233
608	S915	6393	107
609	S914	6379	233
610	S913	6365	107
611	S912	6351	233
612	S911	6337	107
613	S910	6323	233
614	S909	6309	107
615	S908	6295	233
616	S907	6281	107
617	S906	6267	233
618	S905	6253	107
619	S904	6239	233
620	S903	6225	107
621	S902	6211	233
622	S901	6197	107
623	S900	6183	233
624	S899	6169	107
625	S898	6155	233
626	S897	6141	107
627	S896	6127	233
628	S895	6113	107
629	S894	6099	233
630	S893	6085	107
631	S892	6071	233
632	S891	6057	107
633	S890	6043	233
634	S889	6029	107
635	S888	6015	233
636	S887	6001	107
637	S886	5987	233
638	S885	5973	107
639	S884	5959	233
640	S883	5945	107
641	S882	5931	233
642	S881	5917	107
643	S880	5903	233
644	S879	5889	107
645	S878	5875	233
646	S877	5861	107
647	S876	5847	233
648	S875	5833	107
649	S874	5819	233
650	S873	5805	107
651	S872	5791	233
652	S871	5777	107
653	S870	5763	233
654	S869	5749	107
655	S868	5735	233
656	S867	5721	107
657	S866	5707	233
658	S865	5693	107
659	S864	5679	233
660	S863	5665	107

No.	Text Name	X-axis	Y-axis
661	S862	5651	233
662	S861	5637	107
663	S860	5623	233
664	S859	5609	107
665	S858	5595	233
666	S857	5581	107
667	S856	5567	233
668	S855	5553	107
669	S854	5539	233
670	S853	5525	107
671	S852	5511	233
672	S851	5497	107
673	S850	5483	233
674	S849	5469	107
675	S848	5455	233
676	S847	5441	107
677	S846	5427	233
678	S845	5413	107
679	S844	5399	233
680	S843	5385	107
681	S842	5371	233
682	S841	5357	107
683	S840	5343	233
684	S839	5329	107
685	S838	5315	233
686	S837	5301	107
687	S836	5287	233
688	S835	5273	107
689	S834	5259	233
690	S833	5245	107
691	S832	5231	233
692	S831	5217	107
693	S830	5203	233
694	S829	5189	107
695	S828	5175	233
696	S827	5161	107
697	S826	5147	233
698	S825	5133	107
699	S824	5119	233
700	S823	5105	107
701	S822	5091	233
702	S821	5077	107
703	S820	5063	233
704	S819	5049	107
705	S818	5035	233
706	S817	5021	107
707	S816	5007	233
708	S815	4993	107
709	S814	4979	233
710	S813	4965	107
711	S812	4951	233
712	S811	4937	107
713	S810	4923	233
714	S809	4909	107
715	S808	4895	233
716	S807	4881	107
717	S806	4867	233
718	S805	4853	107
719	S804	4839	233
720	S803	4825	107

No.	Text Name	X-axis	Y-axis
721	S802	4811	233
722	S801	4797	107
723	S800	4783	233
724	S799	4769	107
725	S798	4755	233
726	S797	4741	107
727	S796	4727	233
728	S795	4713	107
729	S794	4699	233
730	S793	4685	107
731	S792	4671	233
732	S791	4657	107
733	S790	4643	233
734	S789	4629	107
735	S788	4615	233
736	S787	4601	107
737	S786	4587	233
738	S785	4573	107
739	S784	4559	233
740	S783	4545	107
741	S782	4531	233
742	S781	4517	107
743	S780	4503	233
744	S779	4489	107
745	S778	4475	233
746	S777	4461	107
747	S776	4447	233
748	S775	4433	107
749	S774	4419	233
750	S773	4405	107
751	S772	4391	233
752	S771	4377	107
753	S770	4363	233
754	S769	4349	107
755	S768	4335	233
756	S767	4321	107
757	S766	4307	233
758	S765	4293	107
759	S764	4279	233
760	S763	4265	107
761	S762	4251	233
762	S761	4237	107
763	S760	4223	233
764	S759	4209	107
765	S758	4195	233
766	S757	4181	107
767	S756	4167	233
768	S755	4153	107
769	S754	4139	233
770	S753	4125	107
771	S752	4111	233
772	S751	4097	107
773	S750	4083	233
774	S749	4069	107
775	S748	4055	233
776	S747	4041	107
777	S746	4027	233
778	S745	4013	107
779	S744	3999	233
780	S743	3985	107

No.	Text Name	X-axis	Y-axis
781	S742	3971	233
782	S741	3957	107
783	S740	3943	233
784	S739	3929	107
785	S738	3915	233
786	S737	3901	107
787	S736	3887	233
788	S735	3873	107
789	S734	3859	233
790	S733	3845	107
791	S732	3831	233
792	S731	3817	107
793	S730	3803	233
794	S729	3789	107
795	S728	3775	233
796	S727	3761	107
797	S726	3747	233
798	S725	3733	107
799	S724	3719	233
800	S723	3705	107
801	S722	3691	233
802	S721	3677	107
803	S720	3663	233
804	S719	3649	107
805	S718	3635	233
806	S717	3621	107
807	S716	3607	233
808	S715	3593	107
809	S714	3579	233
810	S713	3565	107
811	S712	3551	233
812	S711	3537	107
813	S710	3523	233
814	S709	3509	107
815	S708	3495	233
816	S707	3481	107
817	S706	3467	233
818	S705	3453	107
819	S704	3439	233
820	S703	3425	107
821	S702	3411	233
822	S701	3397	107
823	S700	3383	233
824	S699	3369	107
825	S698	3355	233
826	S697	3341	107
827	S696	3327	233
828	S695	3313	107
829	S694	3299	233
830	S693	3285	107
831	S692	3271	233
832	S691	3257	107
833	S690	3243	233
834	S689	3229	107
835	S688	3215	233
836	S687	3201	107
837	S686	3187	233
838	S685	3173	107
839	S684	3159	233
840	S683	3145	107

No.	Text Name	X-axis	Y-axis
841	S682	3131	233
842	S681	3117	107
843	S680	3103	233
844	S679	3089	107
845	S678	3075	233
846	S677	3061	107
847	S676	3047	233
848	S675	3033	107
849	S674	3019	233
850	S673	3005	107
851	S672	2991	233
852	S671	2977	107
853	S670	2963	233
854	S669	2949	107
855	S668	2935	233
856	S667	2921	107
857	S666	2907	233
858	S665	2893	107
859	S664	2879	233
860	S663	2865	107
861	S662	2851	233
862	S661	2837	107
863	S660	2823	233
864	S659	2809	107
865	S658	2795	233
866	S657	2781	107
867	S656	2767	233
868	S655	2753	107
869	S654	2739	233
870	S653	2725	107
871	S652	2711	233
872	S651	2697	107
873	S650	2683	233
874	S649	2669	107
875	S648	2655	233
876	S647	2641	107
877	S646	2627	233
878	S645	2613	107
879	S644	2599	233
880	S643	2585	107
881	S642	2571	233
882	S641	2557	107
883	S640	2543	233
884	S639	2529	107
885	S638	2515	233
886	S637	2501	107
887	S636	2487	233
888	S635	2473	107
889	S634	2459	233
890	S633	2445	107
891	S632	2431	233
892	S631	2417	107
893	S630	2403	233
894	S629	2389	107
895	S628	2375	233
896	S627	2361	107
897	S626	2347	233
898	S625	2333	107
899	S624	2319	233
900	S623	2305	107

No.	Text Name	X-axis	Y-axis
901	S622	2291	233
902	S621	2277	107
903	S620	2263	233
904	S619	2249	107
905	S618	2235	233
906	S617	2221	107
907	S616	2207	233
908	S615	2193	107
909	S614	2179	233
910	S613	2165	107
911	S612	2151	233
912	S611	2137	107
913	S610	2123	233
914	S609	2109	107
915	S608	2095	233
916	S607	2081	107
917	S606	2067	233
918	S605	2053	107
919	S604	2039	233
920	S603	2025	107
921	S602	2011	233
922	S601	1997	107
923	S600	1983	233
924	S599	1969	107
925	S598	1955	233
926	S597	1941	107
927	S596	1927	233
928	S595	1913	107
929	S594	1899	233
930	S593	1885	107
931	S592	1871	233
932	S591	1857	107
933	S590	1843	233
934	S589	1829	107
935	S588	1815	233
936	S587	1801	107
937	S586	1787	233
938	S585	1773	107
939	S584	1759	233
940	S583	1745	107
941	S582	1731	233
942	S581	1717	107
943	S580	1703	233
944	S579	1689	107
945	S578	1675	233
946	S577	1661	107
947	S576	1647	233
948	S575	1633	107
949	S574	1619	233
950	S573	1605	107
951	S572	1591	233
952	S571	1577	107
953	S570	1563	233
954	S569	1549	107
955	S568	1535	233
956	S567	1521	107
957	S566	1507	233
958	S565	1493	107
959	S564	1479	233
960	S563	1465	107

No.	Text Name	X-axis	Y-axis
961	S562	1451	233
962	S561	1437	107
963	S560	1423	233
964	S559	1409	107
965	S558	1395	233
966	S557	1381	107
967	S556	1367	233
968	S555	1353	107
969	S554	1339	233
970	S553	1325	107
971	S552	1311	233
972	S551	1297	107
973	S550	1283	233
974	S549	1269	107
975	S548	1255	233
976	S547	1241	107
977	S546	1227	233
978	S545	1213	107
979	S544	1199	233
980	S543	1185	107
981	S542	1171	233
982	S541	1157	107
983	S540	1143	233
984	S539	1129	107
985	S538	1115	233
986	S537	1101	107
987	S536	1087	233
988	S535	1073	107
989	S534	1059	233
990	S533	1045	107
991	S532	1031	233
992	S531	1017	107
993	S530	1003	233
994	S529	989	107
995	S528	975	233
996	S527	961	107
997	S526	947	233
998	S525	933	107
999	S524	919	233
1000	S523	905	107
1001	S522	891	233
1002	S521	877	107
1003	S520	863	233
1004	S519	849	107
1005	S518	835	233
1006	S517	821	107
1007	S516	807	233
1008	S515	793	107
1009	S514	779	233
1010	S513	765	107
1011	S512	751	233
1012	S511	737	107
1013	S510	723	233
1014	S509	709	107
1015	S508	695	233
1016	S507	681	107
1017	S506	667	233
1018	S505	653	107
1019	S504	639	233
1020	S503	625	107

No.	Text Name	X-axis	Y-axis
1021	S502	611	233
1022	S501	597	107
1023	S500	583	233
1024	S499	569	107
1025	S498	555	233
1026	S497	541	107
1027	S496	527	233
1028	S495	513	107
1029	S494	499	233
1030	S493	485	107
1031	S492	471	233
1032	S491	457	107
1033	S490	443	233
1034	S489	429	107
1035	S488	415	233
1036	S487	401	107
1037	S486	387	233
1038	S485	373	107
1039	S484	359	233
1040	S483	345	107
1041	S482	331	233
1042	S481	317	107
1043	DUMMY	303	233
1044	DUMMY	289	107
1045	DUMMY	275	233
1046	DUMMY	247	233
1047	DUMMY	219	233
1048	DUMMY	191	233
1049	DUMMY	163	233
1050	DUMMY	135	233
1051	DUMMY	107	233
1052	DUMMY	79	233
1053	DUMMY	51	233
1054	DUMMY	23	233
1055	DUMMY	-23	233
1056	DUMMY	-51	233
1057	DUMMY	-79	233
1058	DUMMY	-107	233
1059	DUMMY	-135	233
1060	DUMMY	-163	233
1061	DUMMY	-191	233
1062	DUMMY	-219	233
1063	DUMMY	-247	233
1064	DUMMY	-275	233
1065	DUMMY	-289	107
1066	DUMMY	-303	233
1067	S480	-317	107
1068	S479	-331	233
1069	S478	-345	107
1070	S477	-359	233
1071	S476	-373	107
1072	S475	-387	233
1073	S474	-401	107
1074	S473	-415	233
1075	S472	-429	107
1076	S471	-443	233
1077	S470	-457	107
1078	S469	-471	233
1079	S468	-485	107
1080	S467	-499	233

No.	Text Name	X-axis	Y-axis
1081	S466	-513	107
1082	S465	-527	233
1083	S464	-541	107
1084	S463	-555	233
1085	S462	-569	107
1086	S461	-583	233
1087	S460	-597	107
1088	S459	-611	233
1089	S458	-625	107
1090	S457	-639	233
1091	S456	-653	107
1092	S455	-667	233
1093	S454	-681	107
1094	S453	-695	233
1095	S452	-709	107
1096	S451	-723	233
1097	S450	-737	107
1098	S449	-751	233
1099	S448	-765	107
1100	S447	-779	233
1101	S446	-793	107
1102	S445	-807	233
1103	S444	-821	107
1104	S443	-835	233
1105	S442	-849	107
1106	S441	-863	233
1107	S440	-877	107
1108	S439	-891	233
1109	S438	-905	107
1110	S437	-919	233
1111	S436	-933	107
1112	S435	-947	233
1113	S434	-961	107
1114	S433	-975	233
1115	S432	-989	107
1116	S431	-1003	233
1117	S430	-1017	107
1118	S429	-1031	233
1119	S428	-1045	107
1120	S427	-1059	233
1121	S426	-1073	107
1122	S425	-1087	233
1123	S424	-1101	107
1124	S423	-1115	233
1125	S422	-1129	107
1126	S421	-1143	233
1127	S420	-1157	107
1128	S419	-1171	233
1129	S418	-1185	107
1130	S417	-1199	233
1131	S416	-1213	107
1132	S415	-1227	233
1133	S414	-1241	107
1134	S413	-1255	233
1135	S412	-1269	107
1136	S411	-1283	233
1137	S410	-1297	107
1138	S409	-1311	233
1139	S408	-1325	107
1140	S407	-1339	233

No.	Text Name	X-axis	Y-axis
1141	S406	-1353	107
1142	S405	-1367	233
1143	S404	-1381	107
1144	S403	-1395	233
1145	S402	-1409	107
1146	S401	-1423	233
1147	S400	-1437	107
1148	S399	-1451	233
1149	S398	-1465	107
1150	S397	-1479	233
1151	S396	-1493	107
1152	S395	-1507	233
1153	S394	-1521	107
1154	S393	-1535	233
1155	S392	-1549	107
1156	S391	-1563	233
1157	S390	-1577	107
1158	S389	-1591	233
1159	S388	-1605	107
1160	S387	-1619	233
1161	S386	-1633	107
1162	S385	-1647	233
1163	S384	-1661	107
1164	S383	-1675	233
1165	S382	-1689	107
1166	S381	-1703	233
1167	S380	-1717	107
1168	S379	-1731	233
1169	S378	-1745	107
1170	S377	-1759	233
1171	S376	-1773	107
1172	S375	-1787	233
1173	S374	-1801	107
1174	S373	-1815	233
1175	S372	-1829	107
1176	S371	-1843	233
1177	S370	-1857	107
1178	S369	-1871	233
1179	S368	-1885	107
1180	S367	-1899	233
1181	S366	-1913	107
1182	S365	-1927	233
1183	S364	-1941	107
1184	S363	-1955	233
1185	S362	-1969	107
1186	S361	-1983	233
1187	S360	-1997	107
1188	S359	-2011	233
1189	S358	-2025	107
1190	S357	-2039	233
1191	S356	-2053	107
1192	S355	-2067	233
1193	S354	-2081	107
1194	S353	-2095	233
1195	S352	-2109	107
1196	S351	-2123	233
1197	S350	-2137	107
1198	S349	-2151	233
1199	S348	-2165	107
1200	S347	-2179	233

No.	Text Name	X-axis	Y-axis
1201	S346	-2193	107
1202	S345	-2207	233
1203	S344	-2221	107
1204	S343	-2235	233
1205	S342	-2249	107
1206	S341	-2263	233
1207	S340	-2277	107
1208	S339	-2291	233
1209	S338	-2305	107
1210	S337	-2319	233
1211	S336	-2333	107
1212	S335	-2347	233
1213	S334	-2361	107
1214	S333	-2375	233
1215	S332	-2389	107
1216	S331	-2403	233
1217	S330	-2417	107
1218	S329	-2431	233
1219	S328	-2445	107
1220	S327	-2459	233
1221	S326	-2473	107
1222	S325	-2487	233
1223	S324	-2501	107
1224	S323	-2515	233
1225	S322	-2529	107
1226	S321	-2543	233
1227	S320	-2557	107
1228	S319	-2571	233
1229	S318	-2585	107
1230	S317	-2599	233
1231	S316	-2613	107
1232	S315	-2627	233
1233	S314	-2641	107
1234	S313	-2655	233
1235	S312	-2669	107
1236	S311	-2683	233
1237	S310	-2697	107
1238	S309	-2711	233
1239	S308	-2725	107
1240	S307	-2739	233
1241	S306	-2753	107
1242	S305	-2767	233
1243	S304	-2781	107
1244	S303	-2795	233
1245	S302	-2809	107
1246	S301	-2823	233
1247	S300	-2837	107
1248	S299	-2851	233
1249	S298	-2865	107
1250	S297	-2879	233
1251	S296	-2893	107
1252	S295	-2907	233
1253	S294	-2921	107
1254	S293	-2935	233
1255	S292	-2949	107
1256	S291	-2963	233
1257	S290	-2977	107
1258	S289	-2991	233
1259	S288	-3005	107
1260	S287	-3019	233

No.	Text Name	X-axis	Y-axis
1261	S286	-3033	107
1262	S285	-3047	233
1263	S284	-3061	107
1264	S283	-3075	233
1265	S282	-3089	107
1266	S281	-3103	233
1267	S280	-3117	107
1268	S279	-3131	233
1269	S278	-3145	107
1270	S277	-3159	233
1271	S276	-3173	107
1272	S275	-3187	233
1273	S274	-3201	107
1274	S273	-3215	233
1275	S272	-3229	107
1276	S271	-3243	233
1277	S270	-3257	107
1278	S269	-3271	233
1279	S268	-3285	107
1280	S267	-3299	233
1281	S266	-3313	107
1282	S265	-3327	233
1283	S264	-3341	107
1284	S263	-3355	233
1285	S262	-3369	107
1286	S261	-3383	233
1287	S260	-3397	107
1288	S259	-3411	233
1289	S258	-3425	107
1290	S257	-3439	233
1291	S256	-3453	107
1292	S255	-3467	233
1293	S254	-3481	107
1294	S253	-3495	233
1295	S252	-3509	107
1296	S251	-3523	233
1297	S250	-3537	107
1298	S249	-3551	233
1299	S248	-3565	107
1300	S247	-3579	233
1301	S246	-3593	107
1302	S245	-3607	233
1303	S244	-3621	107
1304	S243	-3635	233
1305	S242	-3649	107
1306	S241	-3663	233
1307	S240	-3677	107
1308	S239	-3691	233
1309	S238	-3705	107
1310	S237	-3719	233
1311	S236	-3733	107
1312	S235	-3747	233
1313	S234	-3761	107
1314	S233	-3775	233
1315	S232	-3789	107
1316	S231	-3803	233
1317	S230	-3817	107
1318	S229	-3831	233
1319	S228	-3845	107
1320	S233	-3859	233

No.	Text Name	X-axis	Y-axis
1321	S226	-3873	107
1322	S225	-3887	233
1323	S224	-3901	107
1324	S223	-3915	233
1325	S222	-3929	107
1326	S221	-3943	233
1327	S220	-3957	107
1328	S219	-3971	233
1329	S218	-3985	107
1330	S217	-3999	233
1331	S216	-4013	107
1332	S215	-4027	233
1333	S214	-4041	107
1334	S213	-4055	233
1335	S212	-4069	107
1336	S211	-4083	233
1337	S210	-4097	107
1338	S209	-4111	233
1339	S208	-4125	107
1340	S207	-4139	233
1341	S206	-4153	107
1342	S205	-4167	233
1343	S204	-4181	107
1344	S203	-4195	233
1345	S202	-4209	107
1346	S201	-4223	233
1347	S200	-4237	107
1348	S199	-4251	233
1349	S198	-4265	107
1350	S197	-4279	233
1351	S196	-4293	107
1352	S195	-4307	233
1353	S194	-4321	107
1354	S193	-4335	233
1355	S192	-4349	107
1356	S191	-4363	233
1357	S190	-4377	107
1358	S189	-4391	233
1359	S188	-4405	107
1360	S187	-4419	233
1361	S186	-4433	107
1362	S185	-4447	233
1363	S184	-4461	107
1364	S183	-4475	233
1365	S182	-4489	107
1366	S181	-4503	233
1367	S180	-4517	107
1368	S179	-4531	233
1369	S178	-4545	107
1370	S177	-4559	233
1371	S176	-4573	107
1372	S175	-4587	233
1373	S174	-4601	107
1374	S173	-4615	233
1375	S172	-4629	107
1376	S171	-4643	233
1377	S170	-4657	107
1378	S169	-4671	233
1379	S168	-4685	107
1380	S167	-4699	233

No.	Text Name	X-axis	Y-axis
1381	S166	-4713	107
1382	S165	-4727	233
1383	S164	-4741	107
1384	S163	-4755	233
1385	S162	-4769	107
1386	S161	-4783	233
1387	S160	-4797	107
1388	S159	-4811	233
1389	S158	-4825	107
1390	S157	-4839	233
1391	S156	-4853	107
1392	S155	-4867	233
1393	S154	-4881	107
1394	S153	-4895	233
1395	S152	-4909	107
1396	S151	-4923	233
1397	S150	-4937	107
1398	S149	-4951	233
1399	S148	-4965	107
1400	S147	-4979	233
1401	S146	-4993	107
1402	S145	-5007	233
1403	S144	-5021	107
1404	S143	-5035	233
1405	S142	-5049	107
1406	S141	-5063	233
1407	S140	-5077	107
1408	S139	-5091	233
1409	S138	-5105	107
1410	S137	-5119	233
1411	S136	-5133	107
1412	S135	-5147	233
1413	S134	-5161	107
1414	S133	-5175	233
1415	S132	-5189	107
1416	S131	-5203	233
1417	S130	-5217	107
1418	S129	-5231	233
1419	S128	-5245	107
1420	S127	-5259	233
1421	S126	-5273	107
1422	S125	-5287	233
1423	S124	-5301	107
1424	S123	-5315	233
1425	S122	-5329	107
1426	S121	-5343	233
1427	S120	-5357	107
1428	S119	-5371	233
1429	S118	-5385	107
1430	S117	-5399	233
1431	S116	-5413	107
1432	S115	-5427	233
1433	S114	-5441	107
1434	S113	-5455	233
1435	S112	-5469	107
1436	S107	-5483	233
1437	S110	-5497	107
1438	S109	-5511	233
1439	S108	-5525	107
1440	S107	-5539	233

No.	Text Name	X-axis	Y-axis
1441	S106	-5553	107
1442	S105	-5567	233
1443	S104	-5581	107
1444	S103	-5595	233
1445	S102	-5609	107
1446	S101	-5623	233
1447	S100	-5637	107
1448	S99	-5651	233
1449	S98	-5665	107
1450	S97	-5679	233
1451	S96	-5693	107
1452	S95	-5707	233
1453	S94	-5721	107
1454	S93	-5735	233
1455	S92	-5749	107
1456	S91	-5763	233
1457	S90	-5777	107
1458	S89	-5791	233
1459	S88	-5805	107
1460	S87	-5819	233
1461	S86	-5833	107
1462	S85	-5847	233
1463	S84	-5861	107
1464	S83	-5875	233
1465	S82	-5889	107
1466	S81	-5903	233
1467	S80	-5917	107
1468	S79	-5931	233
1469	S78	-5945	107
1470	S77	-5959	233
1471	S76	-5973	107
1472	S75	-5987	233
1473	S74	-6001	107
1474	S73	-6015	233
1475	S72	-6029	107
1476	S71	-6043	233
1477	S70	-6057	107
1478	S69	-6071	233
1479	S68	-6085	107
1480	S67	-6099	233
1481	S66	-6113	107
1482	S65	-6127	233
1483	S64	-6141	107
1484	S63	-6155	233
1485	S62	-6169	107
1486	S61	-6183	233
1487	S60	-6197	107
1488	S59	-6211	233
1489	S58	-6225	107
1490	S57	-6239	233
1491	S56	-6253	107
1492	S55	-6267	233
1493	S54	-6281	107
1494	S53	-6295	233
1495	S52	-6309	107
1496	S51	-6323	233
1497	S50	-6337	107
1498	S49	-6351	233
1499	S48	-6365	107
1500	S47	-6379	233

No.	Text Name	X-axis	Y-axis
1501	S46	-6393	107
1502	S45	-6407	233
1503	S44	-6421	107
1504	S43	-6435	233
1505	S42	-6449	107
1506	S41	-6463	233
1507	S40	-6477	107
1508	S39	-6491	233
1509	S38	-6505	107
1510	S37	-6519	233
1511	S36	-6533	107
1512	S35	-6547	233
1513	S34	-6561	107
1514	S33	-6575	233
1515	S32	-6589	107
1516	S31	-6603	233
1517	S30	-6617	107
1518	S29	-6631	233
1519	S28	-6645	107
1520	S27	-6659	233
1521	S26	-6673	107
1522	S25	-6687	233
1523	S24	-6701	107
1524	S23	-6715	233
1525	S22	-6729	107
1526	S21	-6743	233
1527	S20	-6757	107
1528	S19	-6771	233
1529	S18	-6785	107
1530	S17	-6799	233
1531	S16	-6813	107
1532	S15	-6827	233
1533	S14	-6841	107
1534	S13	-6855	233
1535	S12	-6869	107
1536	S11	-6883	233
1537	S10	-6897	107
1538	S9	-6911	233
1539	S8	-6925	107
1540	S7	-6939	233
1541	S6	-6953	107
1542	S5	-6967	233
1543	S4	-6981	107
1544	S3	-6995	233
1545	S2	-7009	107
1546	S1	-7023	233
1547	DUMMY	-7037	107
1548	DUMMY	-7051	233
1549	DUMMY	-7067	107
1550	DUMMY	-7083	233
1551	G1	-7099	107
1552	G3	-7115	233
1553	G5	-7131	107
1554	G7	-7147	233
1555	G9	-7163	107
1556	G11	-7179	233
1557	G13	-7195	107
1558	G15	-7211	233
1559	G17	-7227	107
1560	G19	-7243	233

No.	Text Name	X-axis	Y-axis
1561	G21	-7259	107
1562	G23	-7275	233
1563	G25	-7291	107
1564	G27	-7307	233
1565	G29	-7323	107
1566	G31	-7339	233
1567	G33	-7355	107
1568	G35	-7371	233
1569	G37	-7387	107
1570	G39	-7403	233
1571	G41	-7419	107
1572	G43	-7435	233
1573	G45	-7451	107
1574	G47	-7467	233
1575	G49	-7483	107
1576	G51	-7499	233
1577	G53	-7515	107
1578	G55	-7531	233
1579	G57	-7547	107
1580	G59	-7563	233
1581	G61	-7579	107
1582	G63	-7595	233
1583	G65	-7611	107
1584	G67	-7627	233
1585	G69	-7643	107
1586	G71	-7659	233
1587	G73	-7675	107
1588	G75	-7691	233
1589	G77	-7707	107
1590	G79	-7723	233
1591	G81	-7739	107
1592	G83	-7755	233
1593	G85	-7771	107
1594	G87	-7787	233
1595	G89	-7803	107
1596	G91	-7819	233
1597	G93	-7835	107
1598	G95	-7851	233
1599	G97	-7867	107
1600	G99	-7883	233
1601	G101	-7899	107
1602	G103	-7915	233
1603	G105	-7931	107
1604	G107	-7947	233
1605	G109	-7963	107
1606	G111	-7979	233
1607	G113	-7995	107
1608	G115	-8011	233
1609	G117	-8027	107
1610	G119	-8043	233
1611	G121	-8059	107
1612	G123	-8075	233
1613	G125	-8091	107
1614	G127	-8107	233
1615	G129	-8123	107
1616	G131	-8139	233
1617	G133	-8155	107
1618	G135	-8171	233
1619	G137	-8187	107
1620	G139	-8203	233

No.	Text Name	X-axis	Y-axis
1621	G141	-8219	107
1622	G143	-8235	233
1623	G145	-8251	107
1624	G147	-8267	233
1625	G149	-8283	107
1626	G151	-8299	233
1627	G153	-8315	107
1628	G155	-8331	233
1629	G157	-8347	107
1630	G159	-8363	233
1631	G161	-8379	107
1632	G163	-8395	233
1633	G165	-8411	107
1634	G167	-8427	233
1635	G169	-8443	107
1636	G171	-8459	233
1637	G173	-8475	107
1638	G175	-8491	233
1639	G177	-8507	107
1640	G179	-8523	233
1641	G181	-8539	107
1642	G183	-8555	233
1643	G185	-8571	107
1644	G187	-8587	233
1645	G189	-8603	107
1646	G191	-8619	233
1647	G193	-8635	107
1648	G195	-8651	233
1649	G197	-8667	107
1650	G199	-8683	233
1651	G201	-8699	107
1652	G203	-8715	233
1653	G205	-8731	107
1654	G207	-8747	233
1655	G209	-8763	107
1656	G211	-8779	233
1657	G213	-8795	107
1658	G215	-8811	233
1659	G217	-8827	107
1660	G219	-8843	233
1661	G221	-8859	107
1662	G223	-8875	233
1663	G225	-8891	107
1664	G227	-8907	233
1665	G229	-8923	107
1666	G231	-8939	233
1667	G233	-8955	107
1668	G235	-8971	233
1669	G237	-8987	107
1670	G239	-9003	233
1671	DUMMY	-9019	107
1672	DUMMY	-9035	233

Alignment mark	X	Y
A1	-9200	225
A2	9200	225

3.7. Block Function Description

System Interface

The interface operating mode (DBI, DPI or DSI) is selected by hardware pins IM [3:0], as shown in Table 2 below：

IM3	IM2	IM1	IM0	Interface Mode	DB Pin in use	
					Register/Content	GRAM
0	1	0	0	80 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0]
0	1	1	0	80 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0]
0	1	0	1	80 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0]
0	1	1	1	80 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0]
1	1	0	1	3-wire 9-bit data serial interface Ⅰ	SDA: In/OUT	
1	1	1	1	4-wire 8-bit data serial interface Ⅰ	SDA: In/OUT	
0	0	1	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10] D[8:1]
0	0	0	0	80 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10],
0	0	1	1	80 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0]
0	0	0	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]
1	0	0	0	MIPI 1 lane	MIPI Data/Clock	
1	0	0	1	MIPI 1 lane – P/N swap	MIPI Data/Clock	

Table 2: System Interface Mode

External Pad Set				Configuration of MIPI Lane			
IM3	IM2	IM1	IM0	D0P	D0N	CLKP	CLKN
1	0	0	0	D0P	D0N	CLKP	CLKN
1	0	0	1	D0N	D0P	CLKN	CLKP

Parallel RGB Interface

ILI9342E also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 320(RGB) x240 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9342E can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as VSP, VSN, VGH, VGL for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9342E incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 960-output source driver (S1~S960), and 240-output gate driver (G1~G240).

CABC(Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

4. Function Description

4.1. MCU interfaces

ILI9342E provides the 8-/9-/16-/18-bit parallel system interface for 8080-Ⅰ/8080-Ⅱ series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use	
					Register/Content	GRAM
0	1	0	0	80 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0]
0	1	1	0	80 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0]
0	1	0	1	80 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0]
0	1	1	1	80 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0]
1	1	0	1	3-wire 9-bit data serial interface Ⅰ	SDA: In/OUT	
1	1	1	1	4-wire 8-bit data serial interface Ⅰ	SDA: In/OUT	
0	0	1	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10] D[8:1]
0	0	0	0	80 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10],
0	0	1	1	80 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0]
0	0	0	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]

4.1.2. 8080-Ⅰ Series Parallel Interface

ILI9342E can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅰ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9342E chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9342E latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-Ⅰ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. Interface bus width can be selected by IM [3:0] bits.

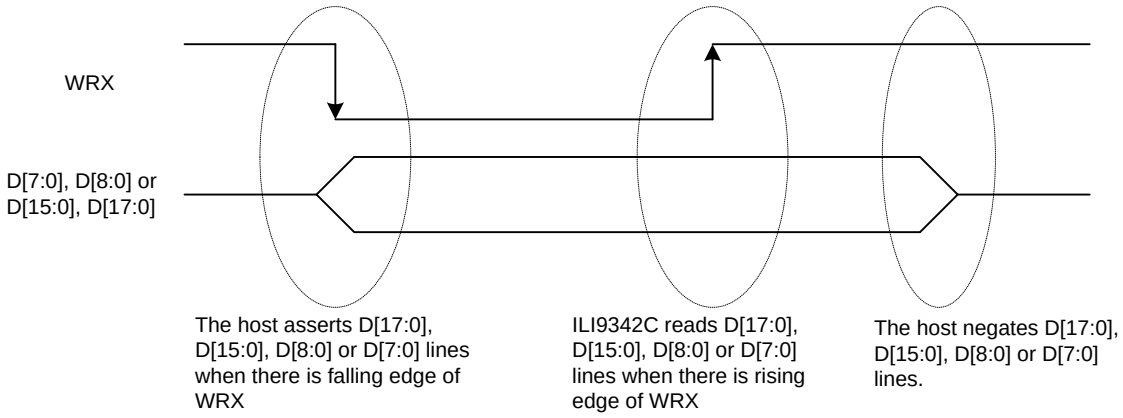
The selection of 8080-Ⅰ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8080 MCU 8-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	0	8080 MCU 16-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	0	1	8080 MCU 9-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	1	8080 MCU 18-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

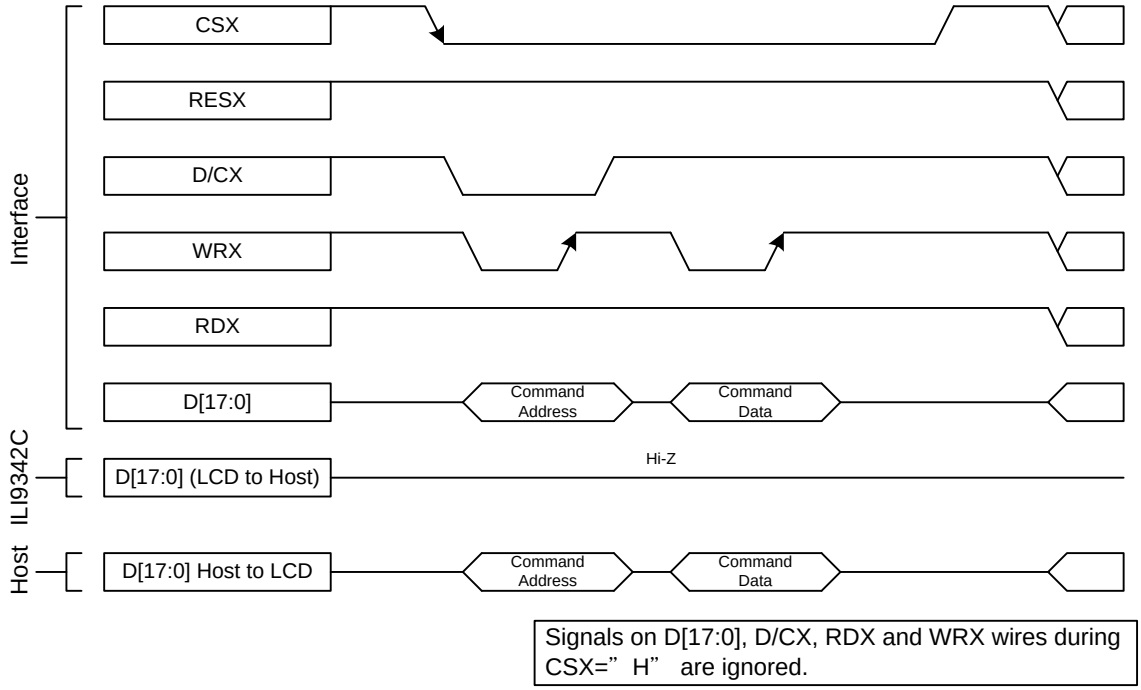
4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅰ MCU interface.



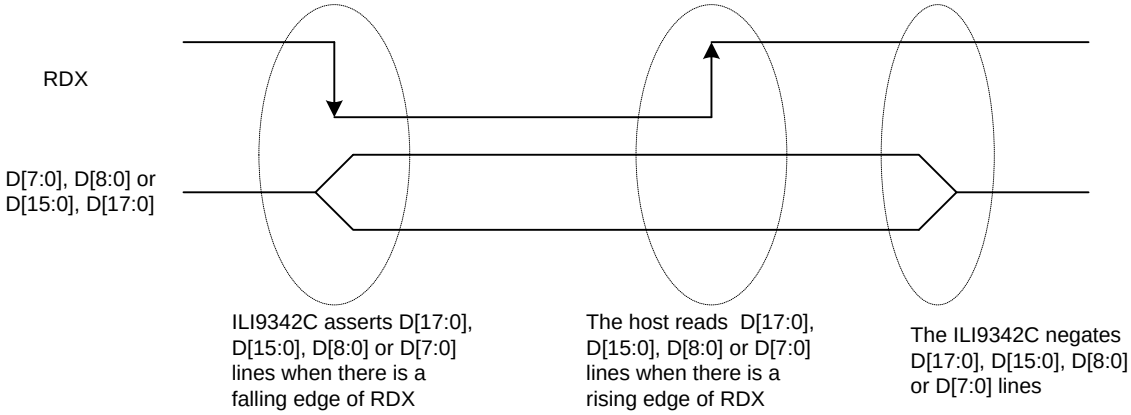
Note: WRX is an unsynchronized signal (It can be stopped)



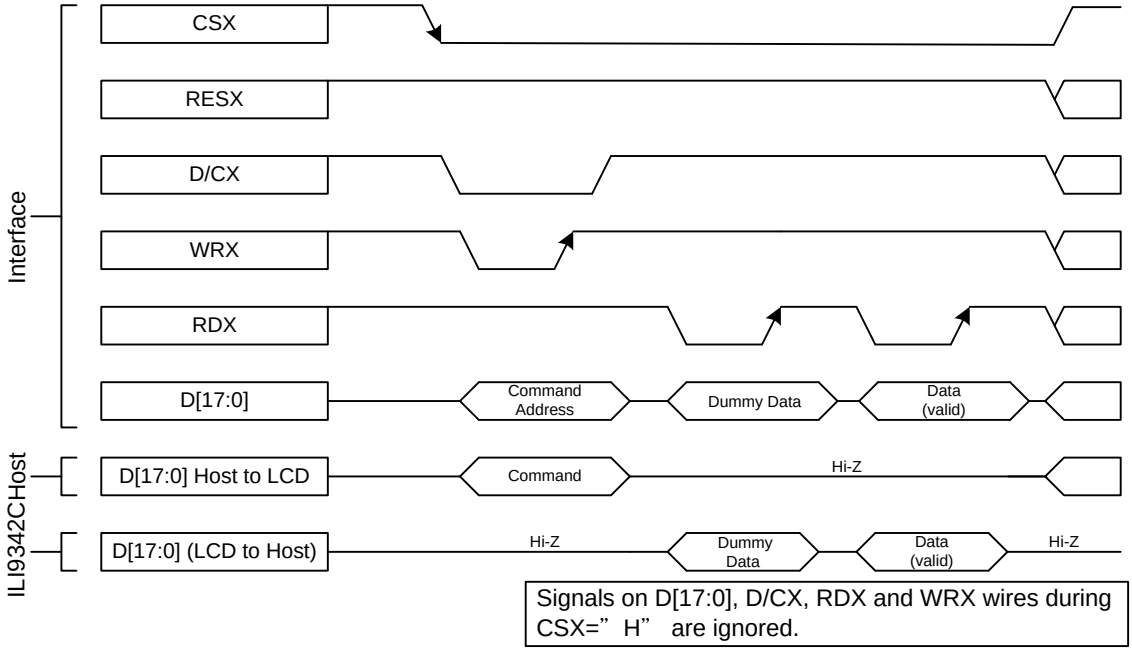
4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅰ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 8080-Ⅱ Parallel Interface

ILI9342E can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9342E chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9342E latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-Ⅱ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. Interface bus width can be selected by IM [3:0] bits.

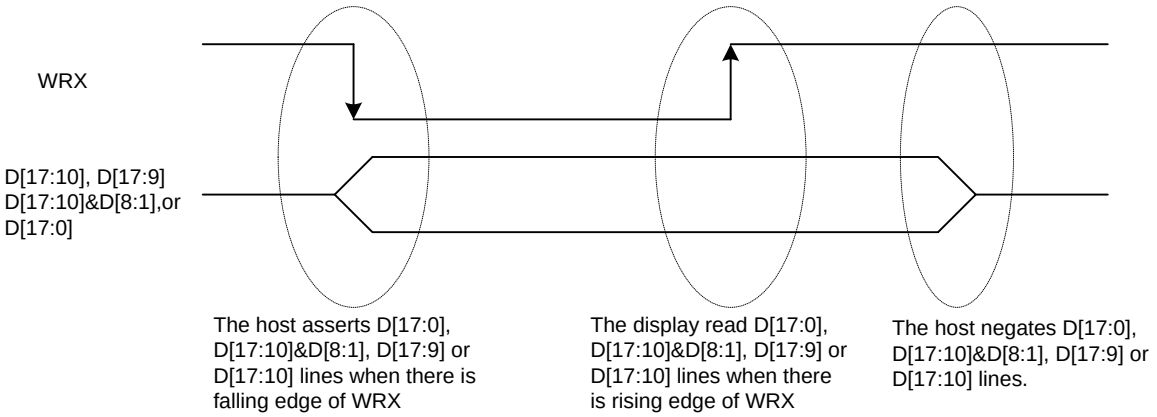
The selection of 8080-Ⅱ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	0	1	0	8080 MCU 16-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	0	8080 MCU 8-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 9-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

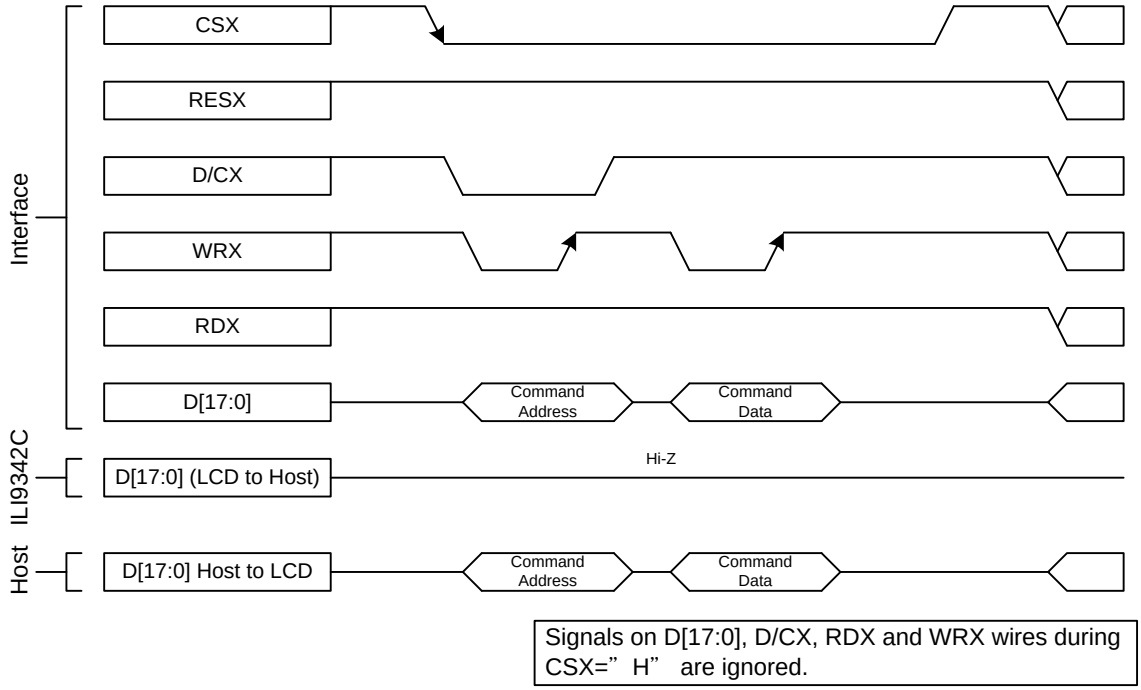
4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅱ MCU interface.



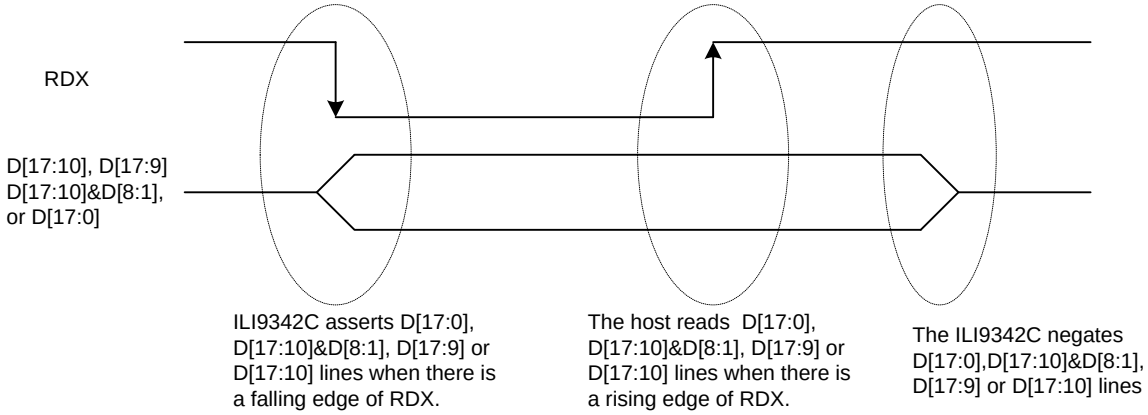
Note: WRX is an unsynchronized signal (It can be stopped)



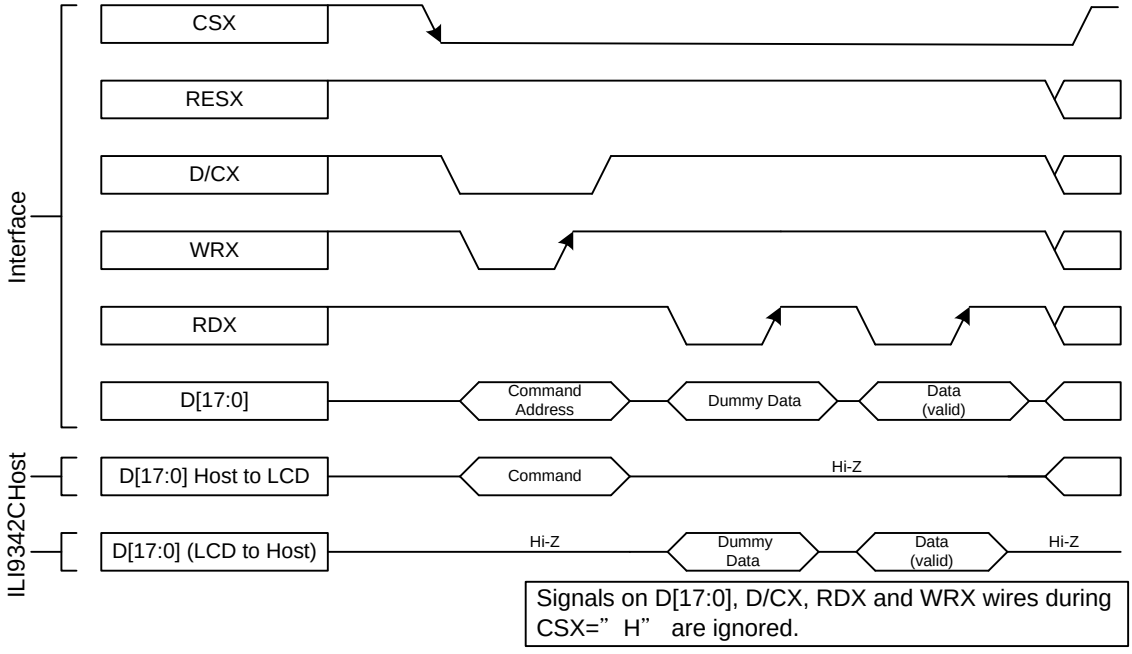
4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅱ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	1	0	1	3-line serial interface	"L"	-	↑	Read/Write command, parameter or display data.
1	1	1	1	4-line serial interface	"L"	'H/L"	↑	Read/Write command, parameter or display data.

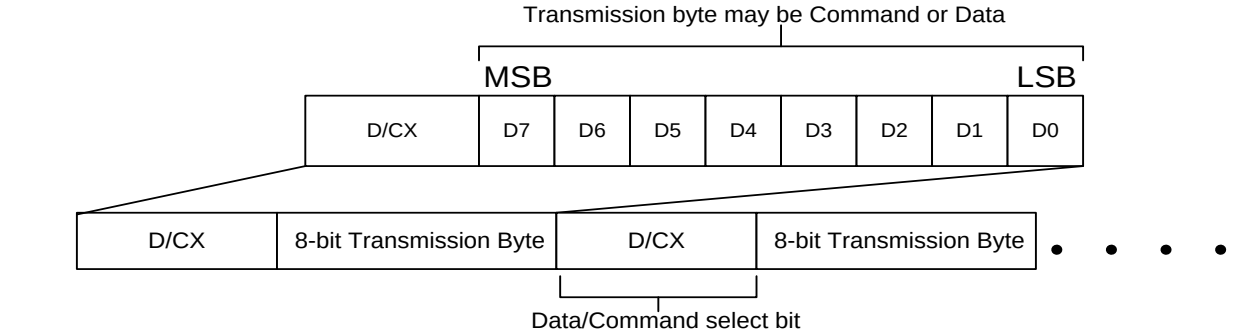
ILI9342E supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9342E. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to ILI9342E. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

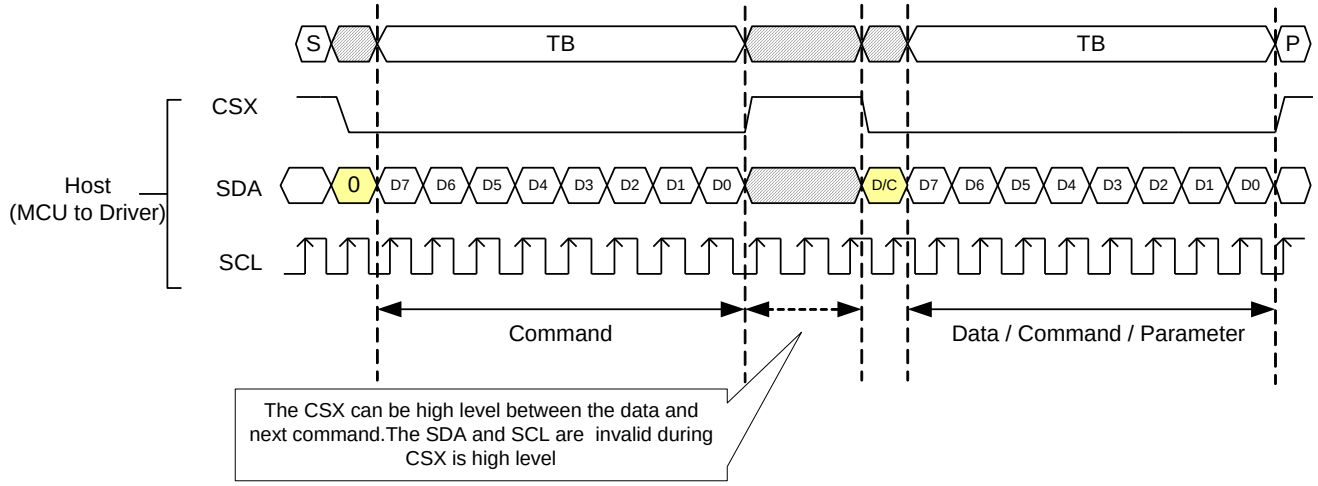
Any instruction can be sent in any order to ILI9342E and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

3-line Serial Interface Data Format

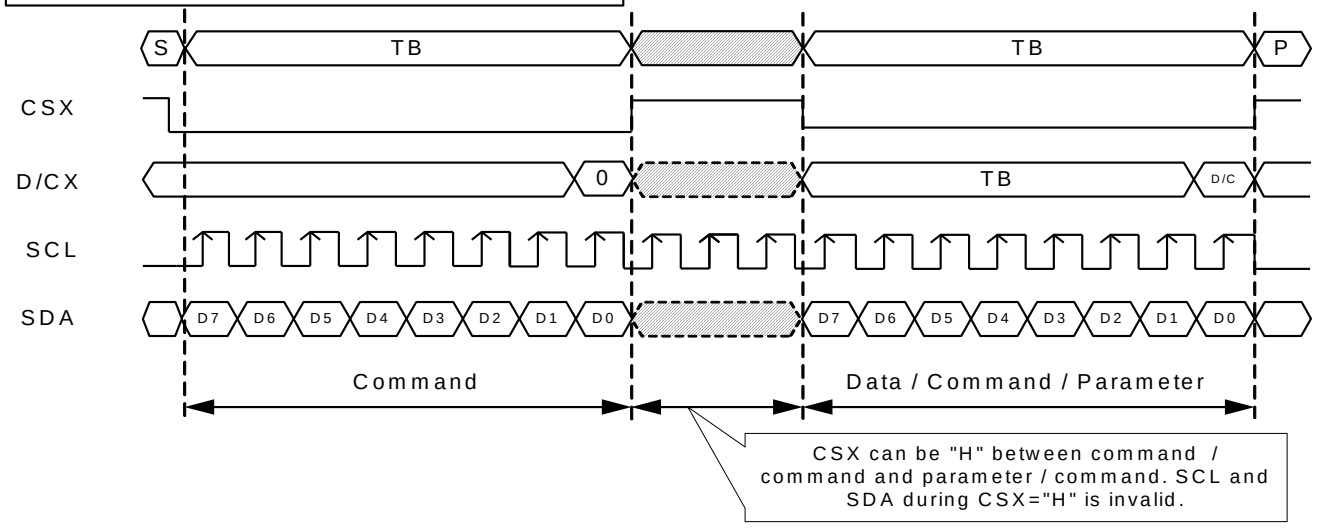


Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9342E on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



4-line Serial Interface Protocol



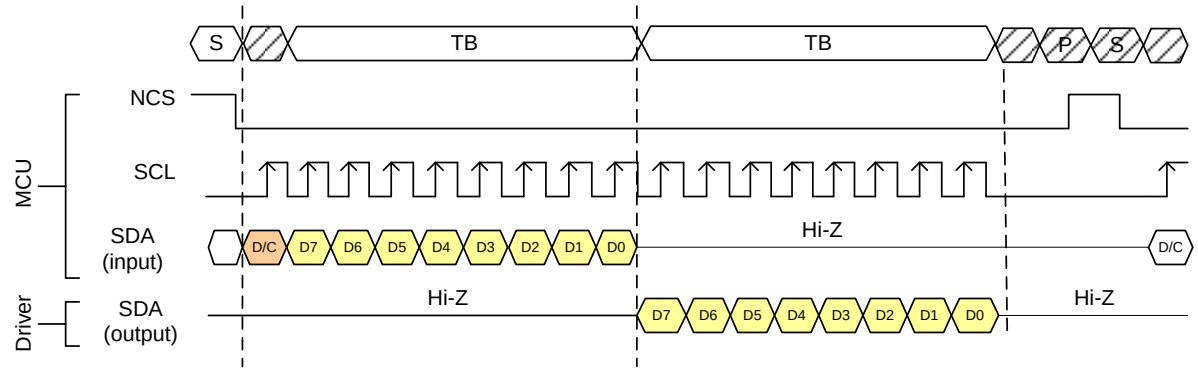
4.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from ILI9342E. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9342E latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

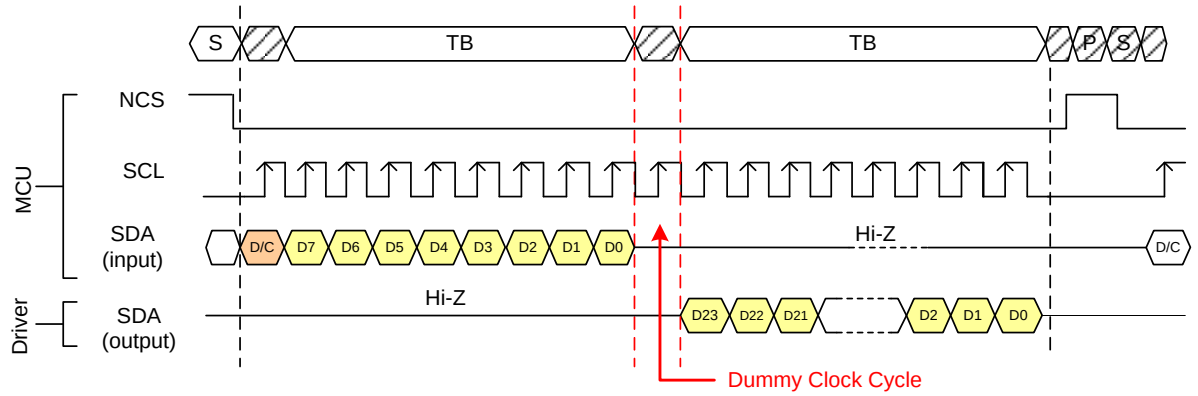
The host read the n-th parameter of the level 2 command by SPI interface need set additional command RD9h at first. Only the first 8-bit parameter will be read out by the serial interface protocol at a time and it will be necessary set RD9h command again for another ordinal number parameter.

3-wire Serial Interface Protocol

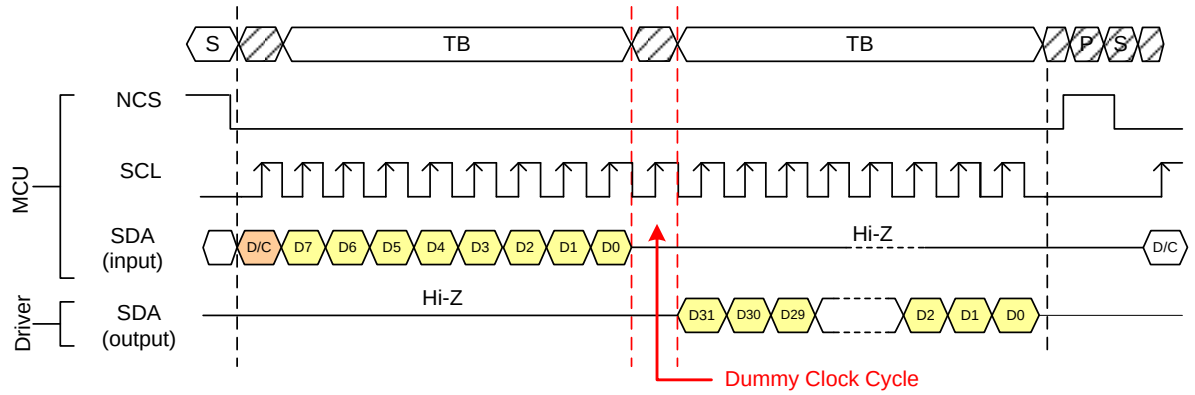
3-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



3-line Serial Protocol (for RDDID command: 24-bit read)

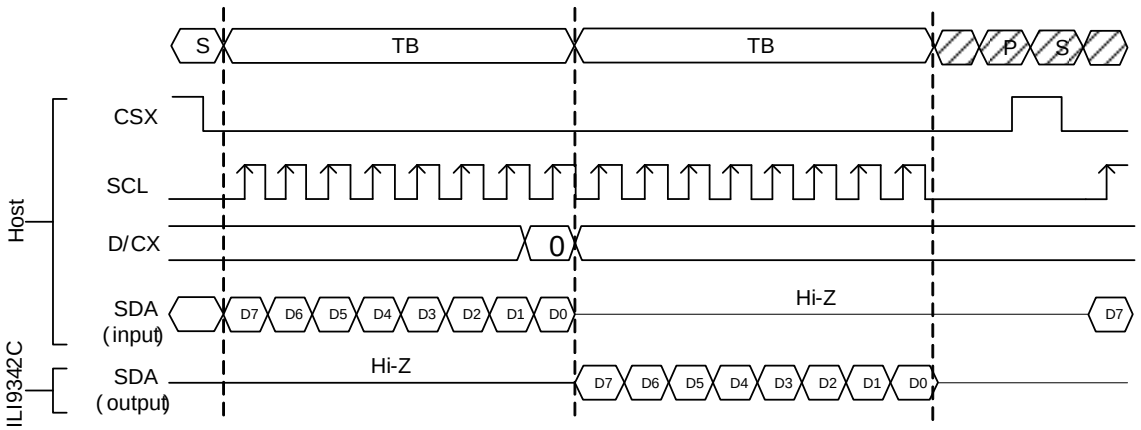


3-line Serial Protocol (for RDDST command: 32-bit read)

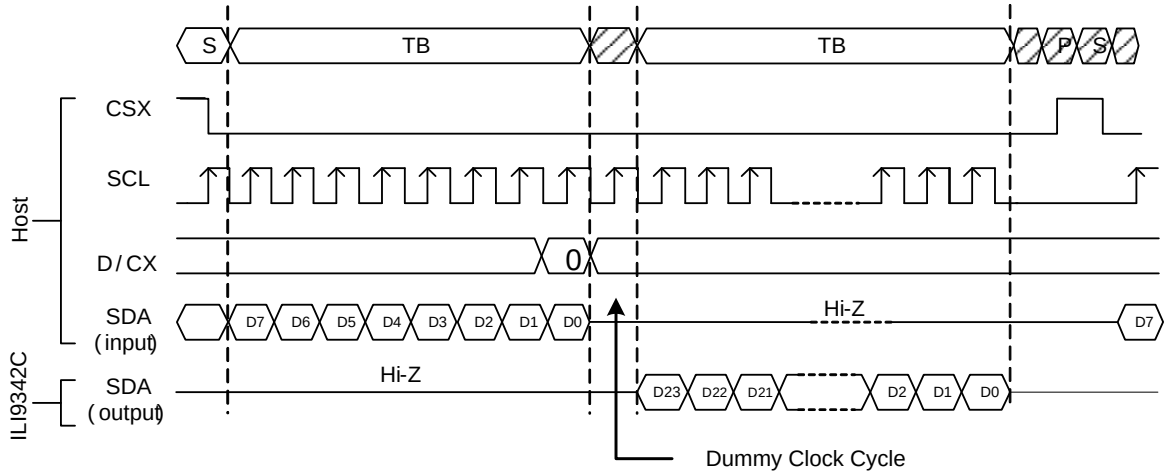


4-wire Serial Interface Protocol

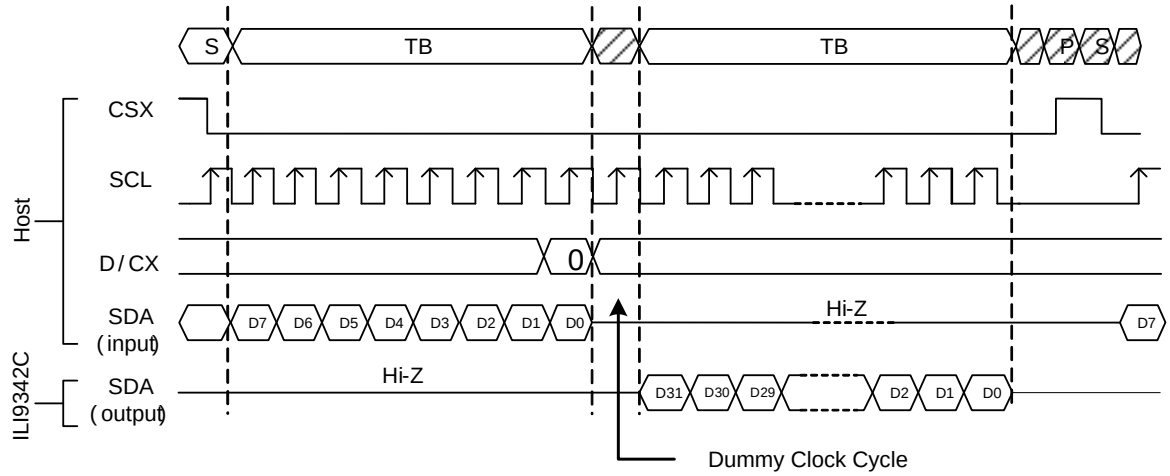
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command 24-bit read)

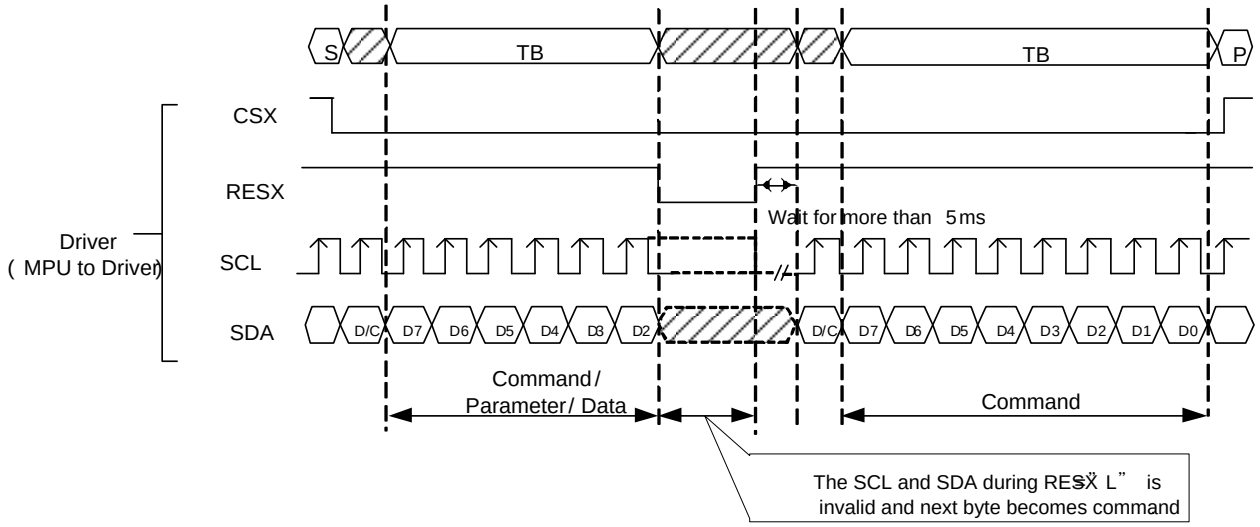


4-line Serial Protocol (for RDDST command 32-bit read)

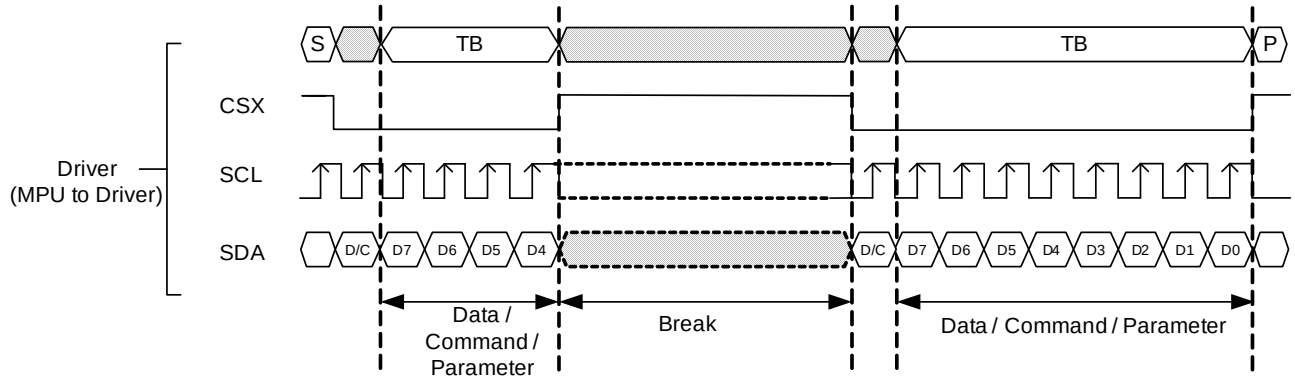


4.1.11. Data Transfer Break and Recovery

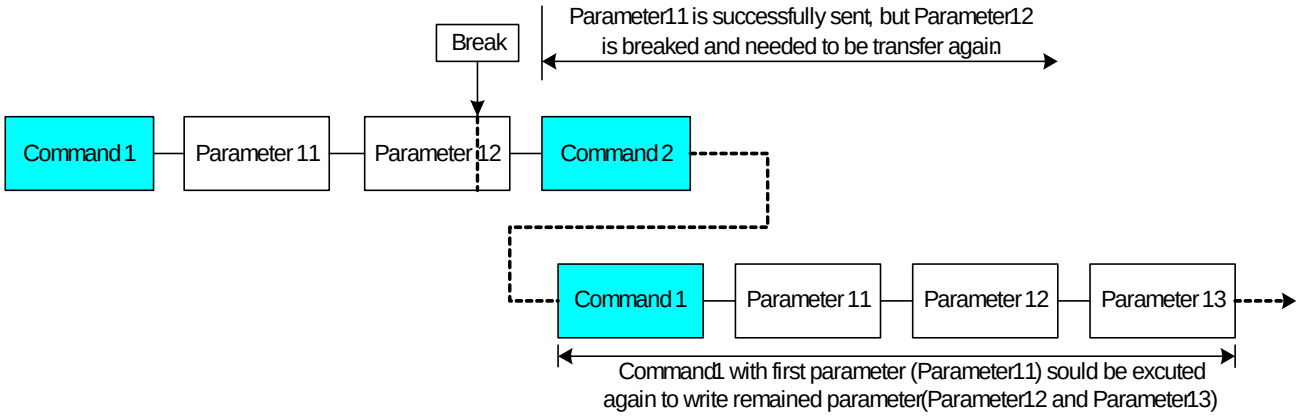
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



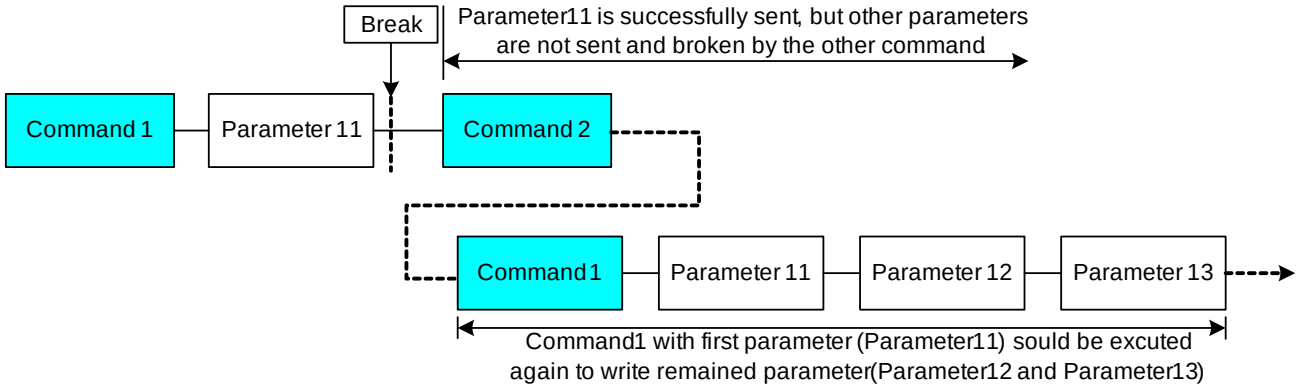
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

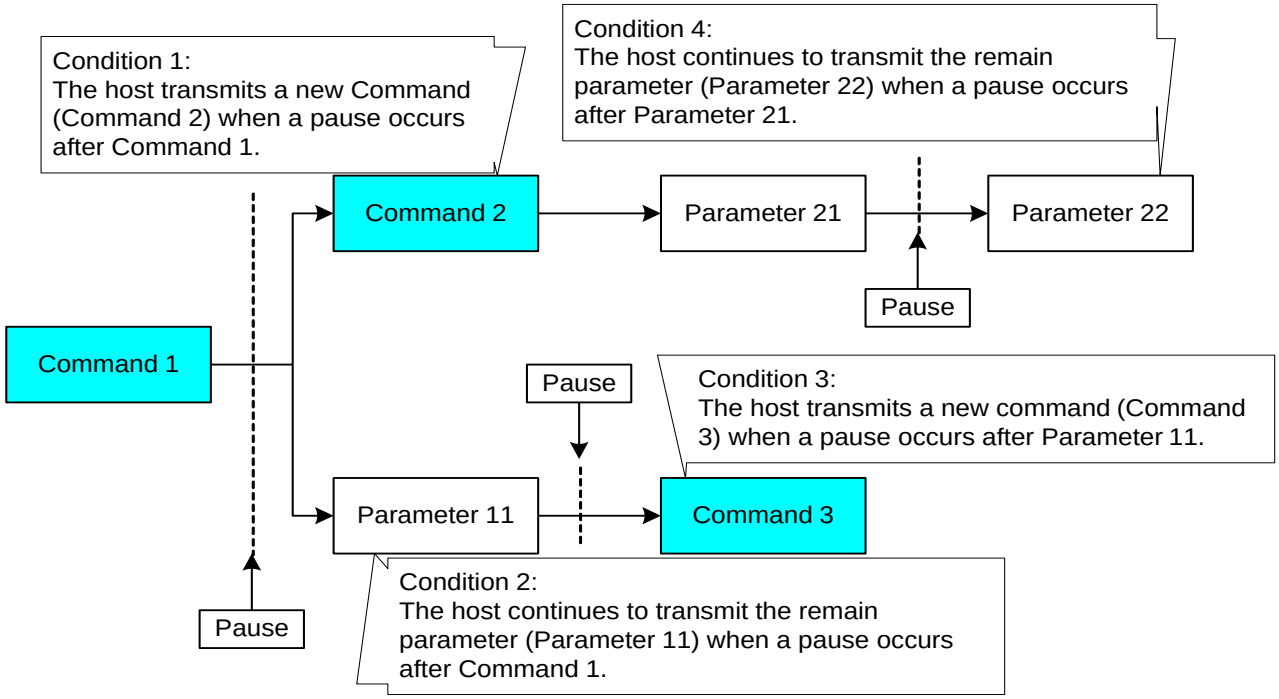


4.1.12. Data Transfer Pause

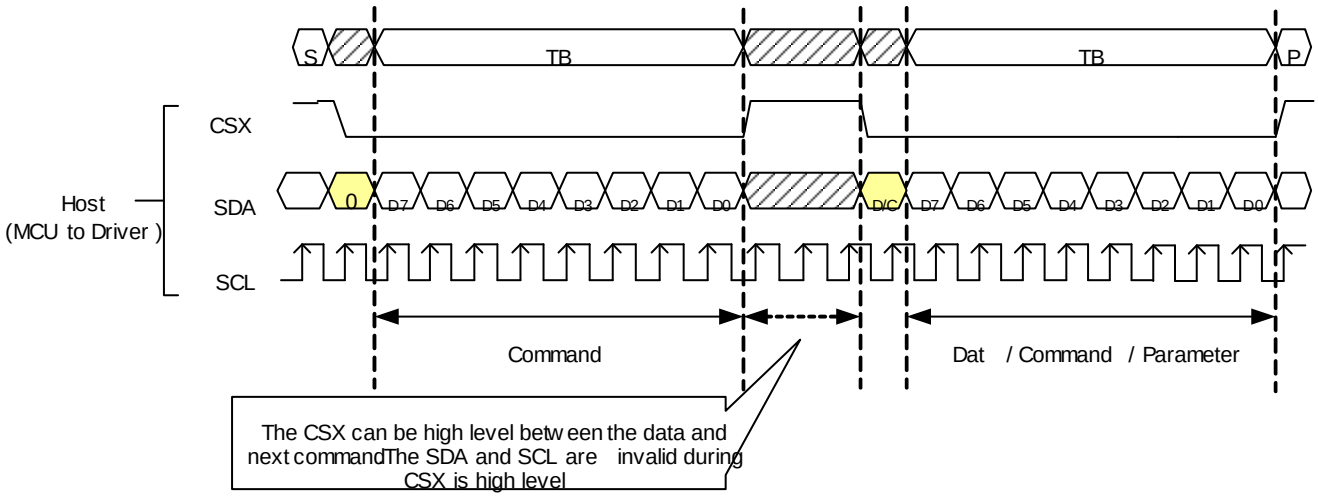
It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9342E will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

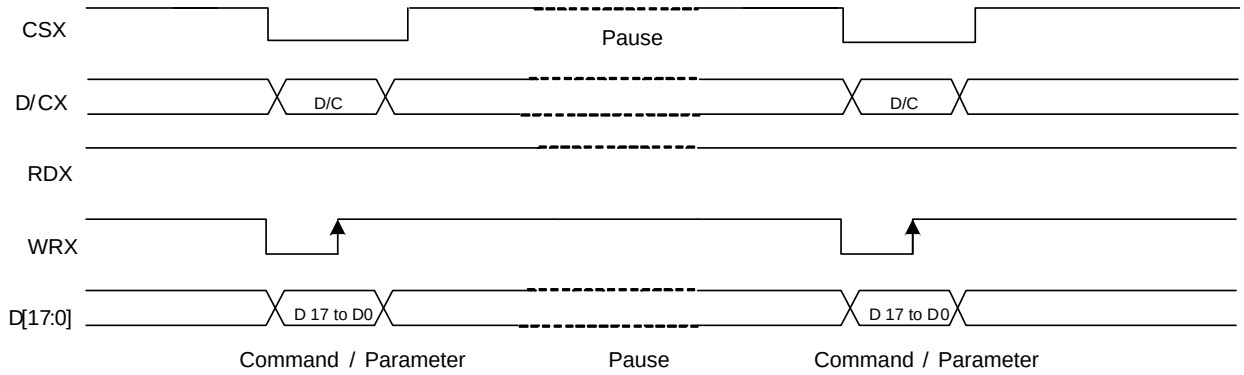
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter



4.1.13. Serial Interface Pause (3_wire)



4.1.14. Parallel Interface Pause

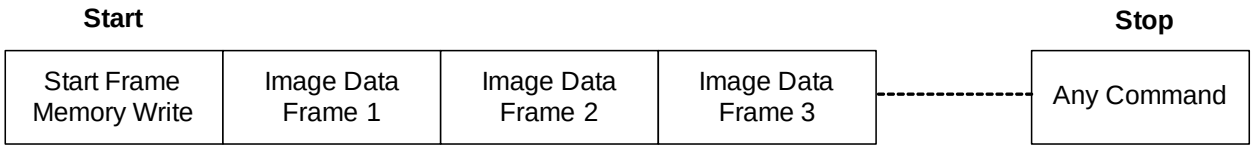


4.1.15. Data Transfer Mode

ILI9342E can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

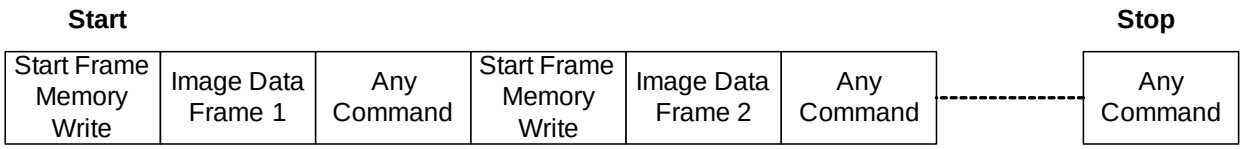
4.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



4.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2. RGB Interface

4.2.1. RGB Interface Selection

ILI9342E has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9342E supports several pixel formats that can be selected by DPI [2:0] bits of “Pixel Format Set (3Ah)” and RIM bit of RD8h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]		RIM	DPI[2:0]			RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	**DE Mode** Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, DB[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[15:0]
1	0	1	1	1	1	8-bit RGB interface (16.77M colors)		VSYNC, HSYNC, DE, DOTCLK, DB[7:0]
1	0	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	**SYNC Mode** In SYNC mode, DE signal is ignored; blanking porch is determined by D1h command.	VSYNC, HSYNC, DOTCLK, DB[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[15:0]
1	1	1	1	1	1	8-bit RGB interface (16.77M colors)		VSYNC, HSYNC, DE, DOTCLK, DB[7:0]
1	1	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]

18-bit data interface (DB[17:0] is used) , DPI[2:0] = 110 , and RIM = 0

DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data interface (DB[15:0] is used) , DPI[2:0] = 101 , and RIM = 0

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

8-bit data interface (DB[7:0] is used) , DPI[2:0] = 111 , and RIM = 1

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data interface (DB[5:0] is used) , DPI[2:0] = 110 , and RIM = 1

DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0
R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

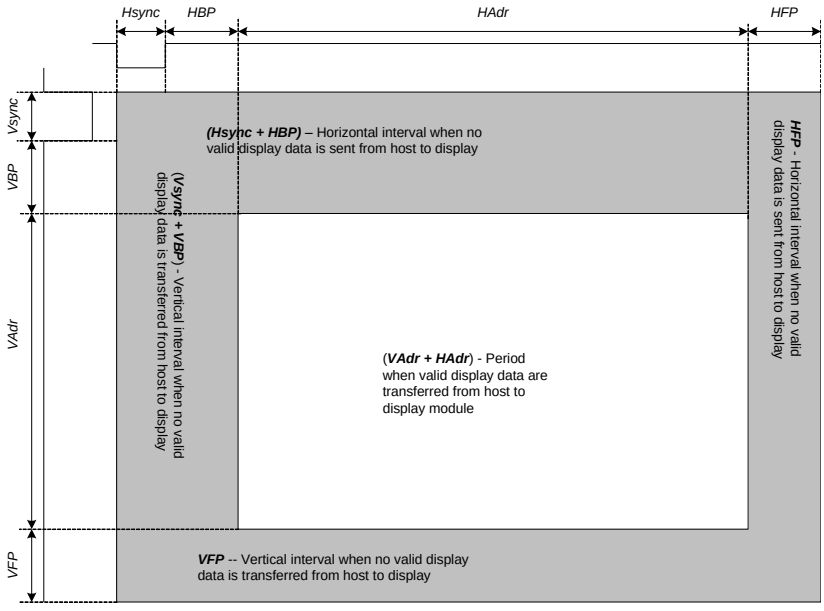
6-bit data interface (DB[5:0] is used) , DPI[2:0] = 101 , and RIM = 1

DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0	DB5	DB4	DB3	DB2	DB1	DB0
R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as continues internal clock for other functions of the display module. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.

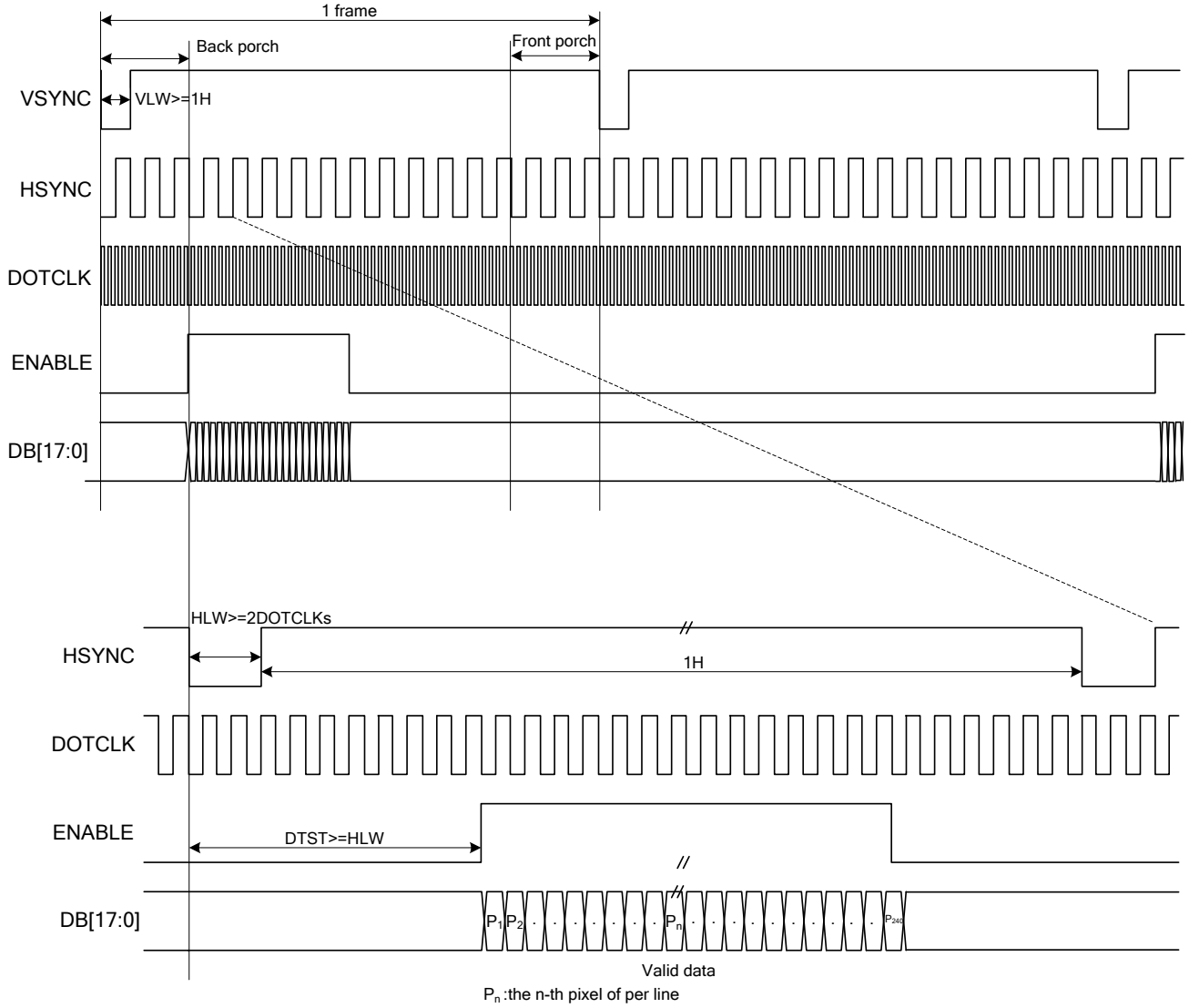


Parameters	Symbols	Condition	Min.	Typ.	Units
DOTCLK Frequency	DCLK		-	10	MHz
Frame Rate	FR		-	60	fps
Horizontal Synchronization	Hsync		2	10	DOTCLK
Horizontal Back Porch	HBP		58	318	DOTCLK
Horizontal Address	HAdr		-	320	DOTCLK
Horizontal Front Porch	HFP		2	10	DOTCLK
Vertical Synchronization	Vsync		1	2	Line
Vertical Back Porch	VBP		1	6	Line
Vertical Address	VAdr		-	240	Line
Vertical Front Porch	VFP		3	8	Line
Note1：320(RGB)X240 (18-bit RGB interface) reference Note2：VBP+Vsync+VFP ≥ 16 lines Note3：When use RGB Sync mode, Hsync+HBP timing ≥ 3us					

Parameters	Symbols	Condition	Min.	Typ.	Units
DOTCLK Frequency	DCLK		-	10	MHz
Frame Rate	FR		-	60	fps
Horizontal Synchronization	Hsync		2	10	DOTCLK
Horizontal Back Porch	HBP		58	398	DOTCLK
Horizontal Address	HAdr		-	320	DOTCLK
Horizontal Front Porch	HFP		2	10	DOTCLK
Vertical Synchronization	Vsync		1	2	Line
Vertical Back Porch	VBP		1	6	Line
Vertical Address	VAdr		-	240	Line
Vertical Front Porch	VFP		3	8	Line
Note1：240(RGB)X240 (18-bit RGB interface) reference Note2：VBP+Vsync+VFP ≥ 16 lines					

4.2.2. RGB Interface Timing

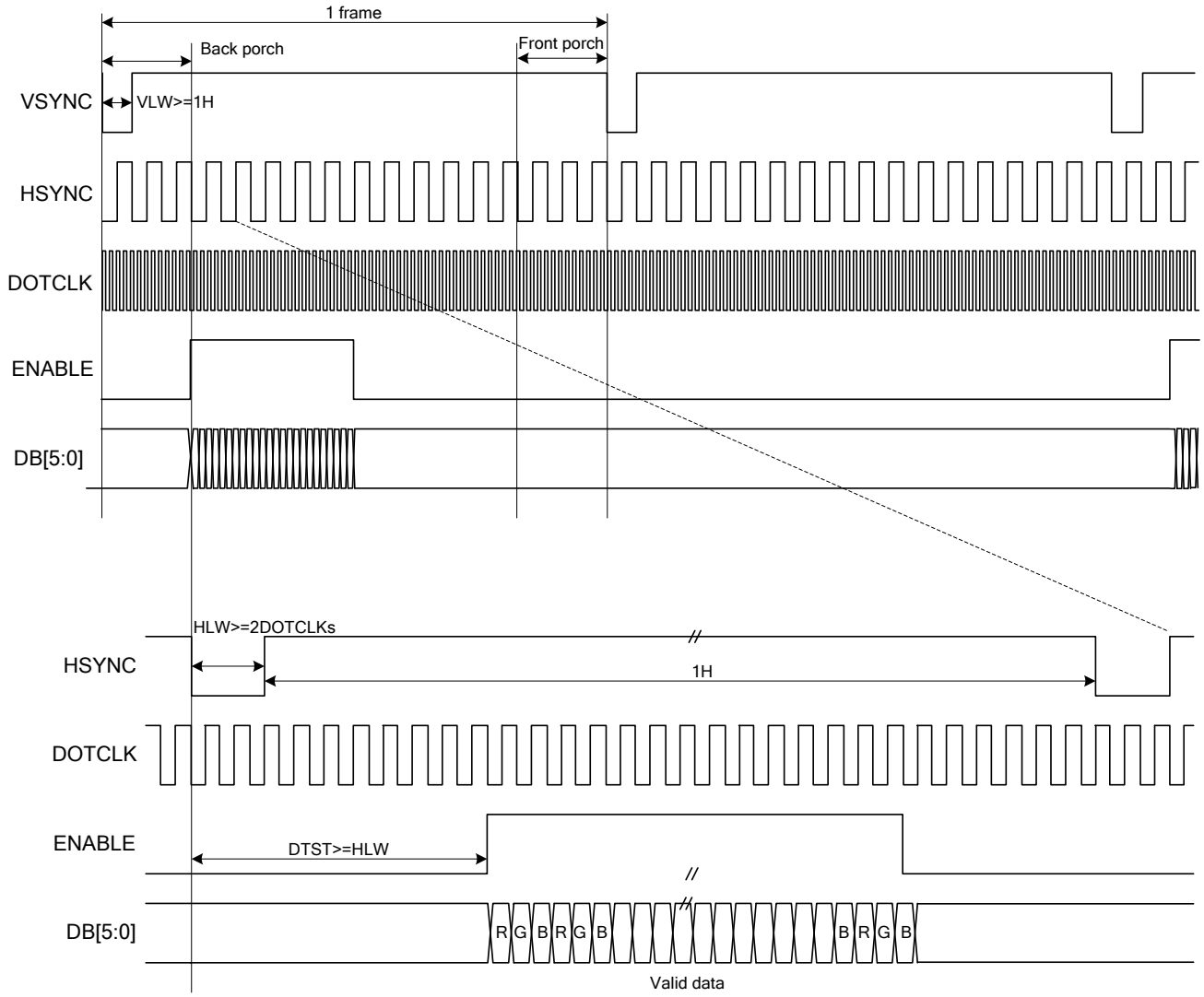
The timing chart of 18-/16-bit RGB interface mode is shown as below.



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (D0h)" command.

The timing chart of 8/6-bit RGB interface mode is shown as below:



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

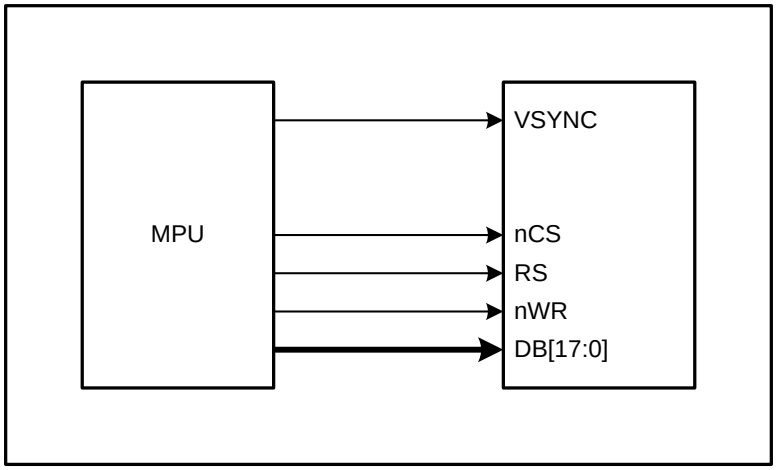
Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (D0h)" command.

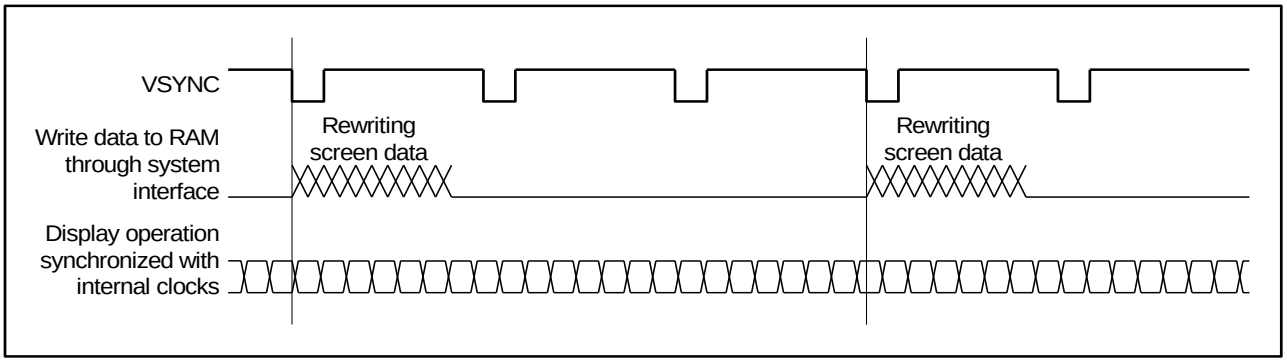
Note 3: In 8/6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

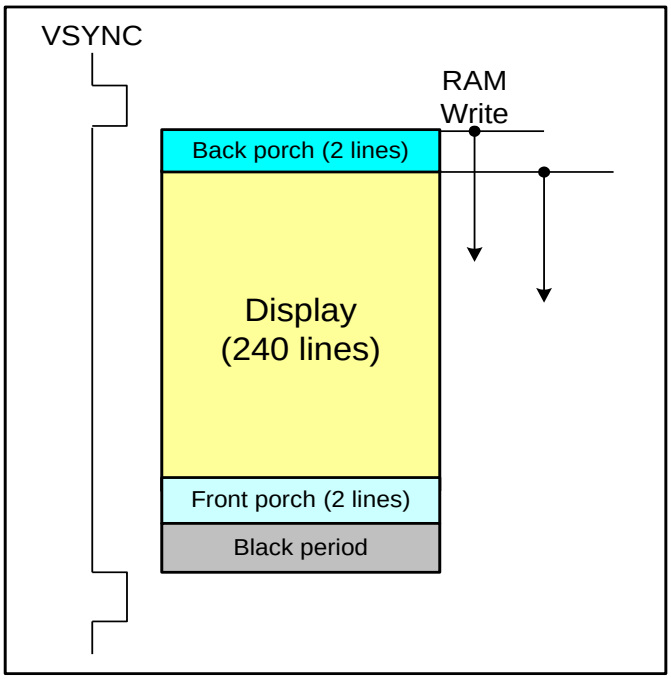
4.3. VSYNC Interface

ILI9342E supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{320 \times \text{DisplayLines(NL)}}{[\text{BackPorch(VBP)} + \text{DisplayLines(NL)} - \text{margins}] \times \text{Clocks per line} \times (1/\text{fosc})}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 320 RGB × 240 lines

Lines: 240 lines (NL = 1110111)

Back porch: 2 lines (VBP = 0000010)

Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = 70 x [240+ 2 + 2] x 27 clocks x (1.1/0.9) ≒ 748KHz

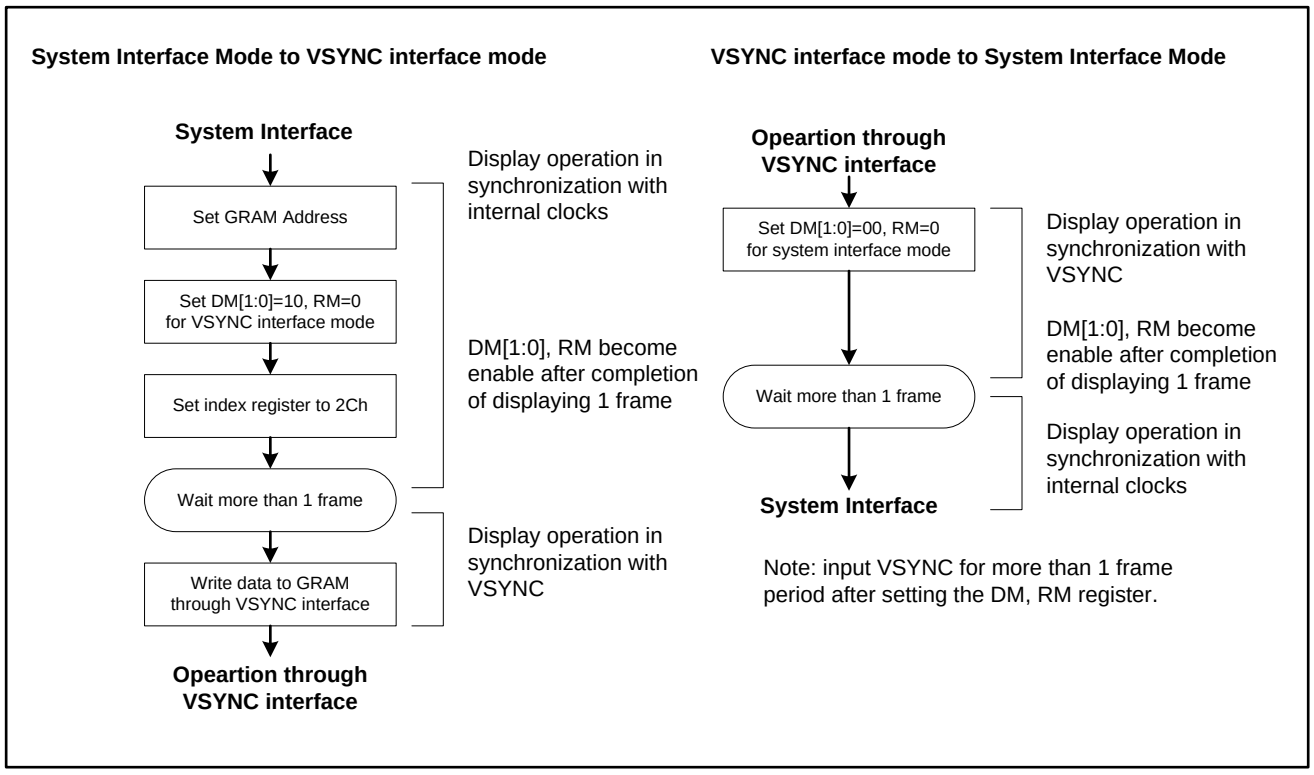
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 320 x 240 x 748K / [(2 + 240 – 2)lines x 27clocks] ≒ 6.65 MHz

The above theoretical value is calculated based on the premise that the ILI9342E starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9342E starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.



4.4. DSI System Interface

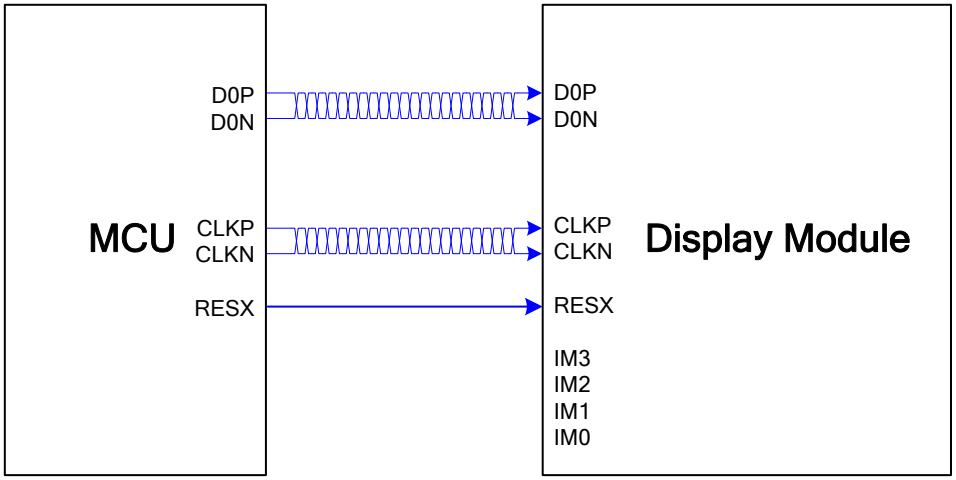
4.4.1. General Description

The pad mapping of MIPI DSI interface is set by IM[3:0] pin (as below table).

Table 3: DSI Interface Lane Mode Selection

External Pad Set				Configuration of MIPI Lane			
IM3	IM2	IM1	IM0	D0P	D0N	CLKP	CLKN
1	0	0	0	D0P	D0N	CLKP	CLKN
1	0	0	1	D0N	D0P	CLKN	CLKP

Figure 2: DSI System Interface Diagram



The communication is separated into two different levels between the MCU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

4.4.2. Interface Level Communication

4.4.2.1. General

The display module uses data and clock lane differential pairs for DSI (DSI-2). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 4: High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

1. *Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.*
2. *If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.*

4.4.2.2. DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane are in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM). These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.

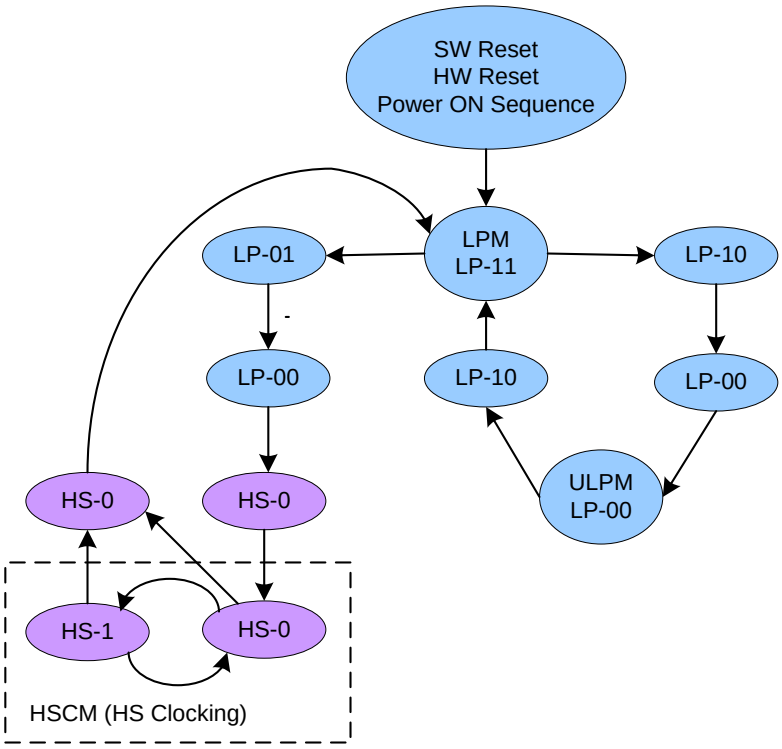


Figure 3: Clock lane Power Modes

4.4.2.2.1. Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11

2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).

This sequence is illustrated below.

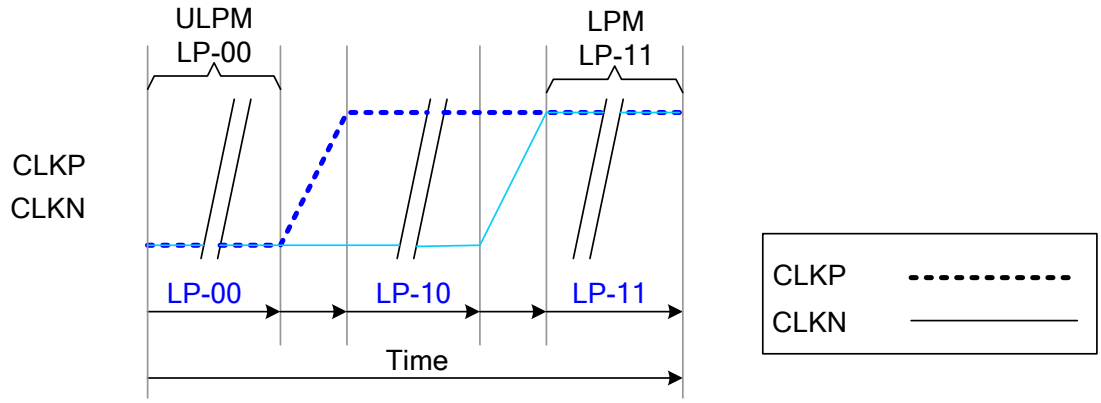


Figure 4: From ULPM to LPM

3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM). This sequence is illustrated below.

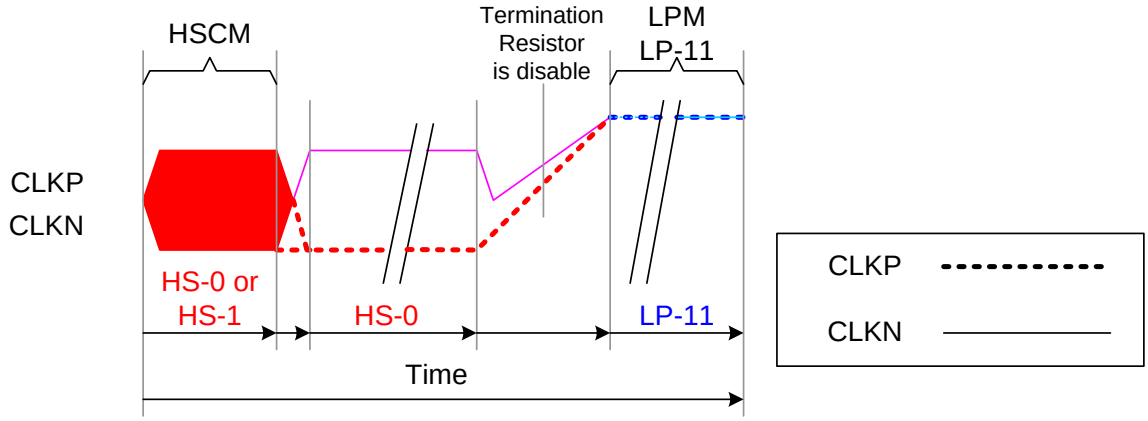


Figure 5: From High Speed Clock Mode (HSCM) to LPM

The changes of all the three modes are illustrated in the flow chart below.

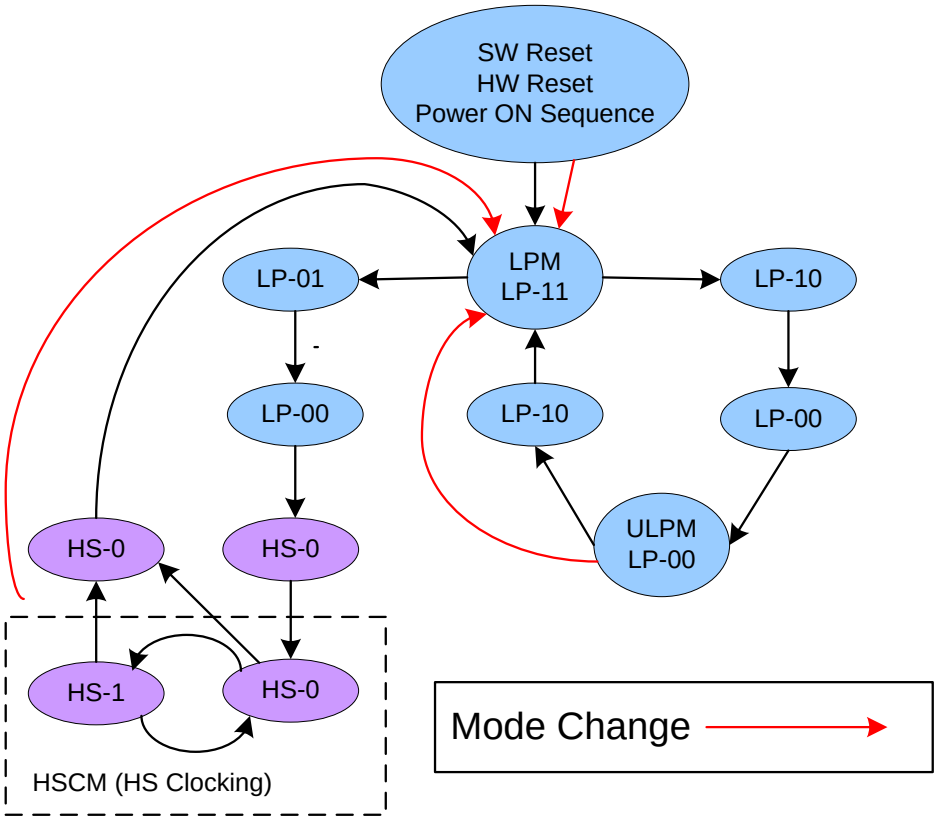


Figure 6: All Three Mode Changes to LPM

4.4.2.2.2. Ultra-Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Ultra-Low power Mode (ULPM) when CLK lanes enter the LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.

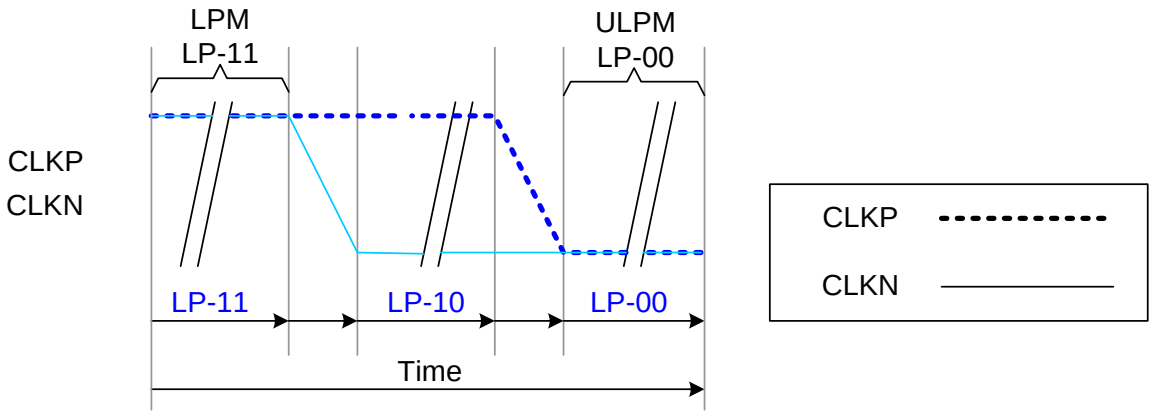


Figure 7: From LPM to ULPM

The mode change is also illustrated below.

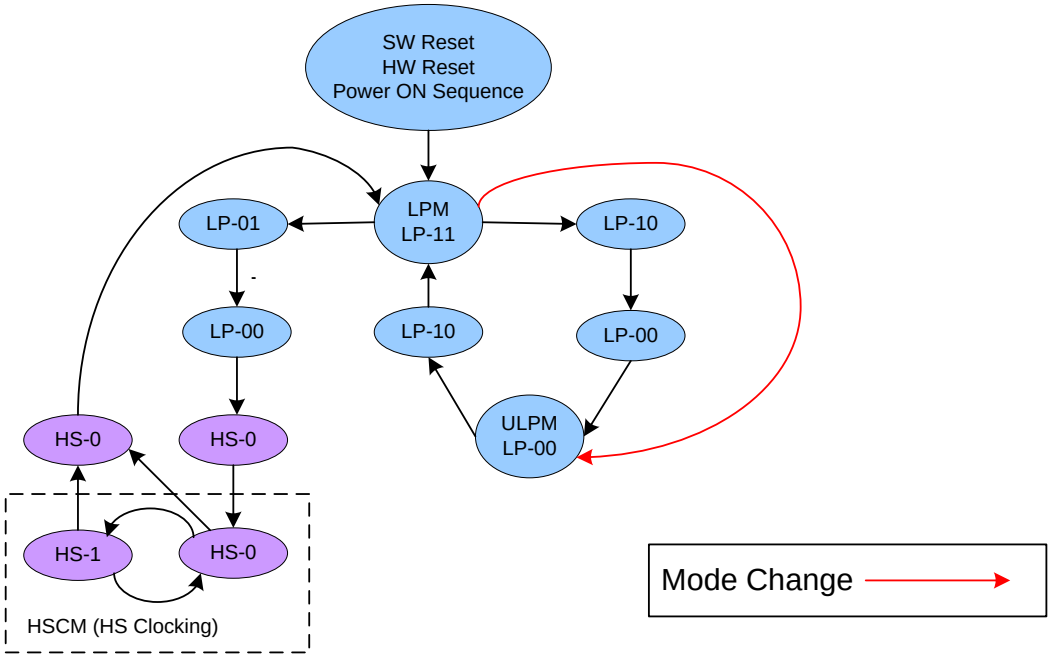


Figure 8: Mode Change from LPM to ULPM

4.4.2.2.3. High-Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

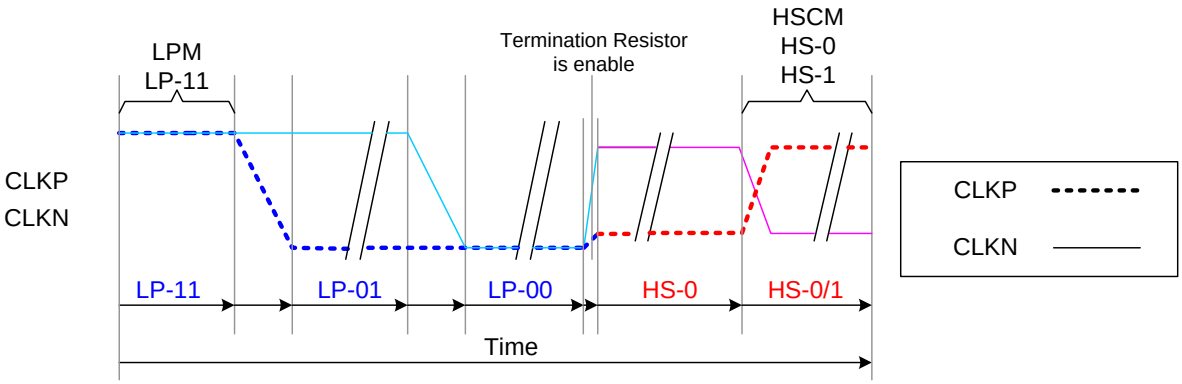


Figure 9: From LPM to HSCM

The mode change is also illustrated below.

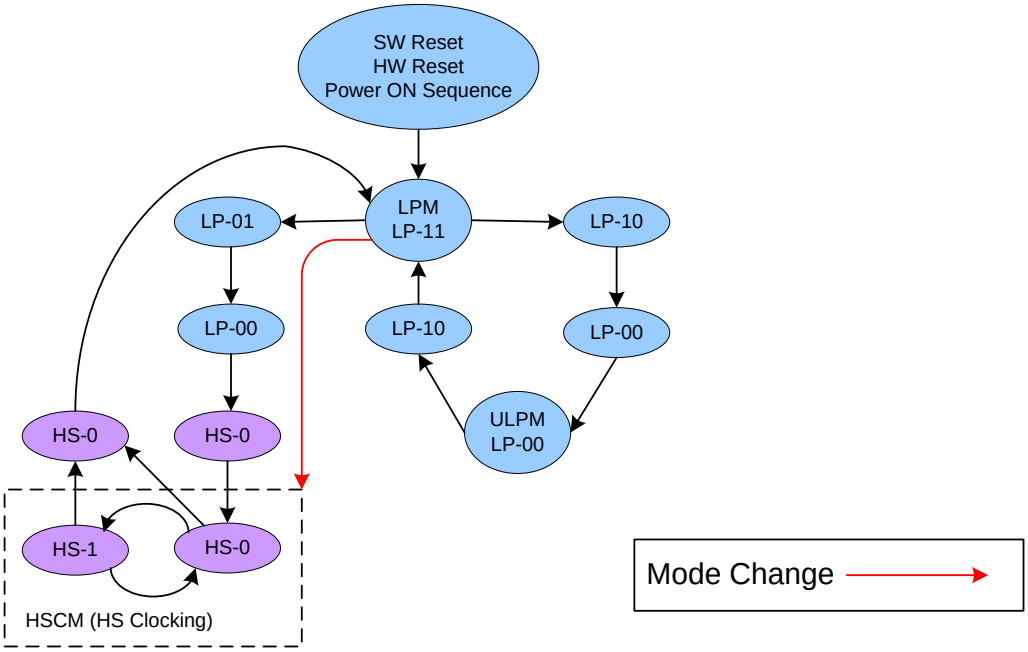


Figure 10: Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

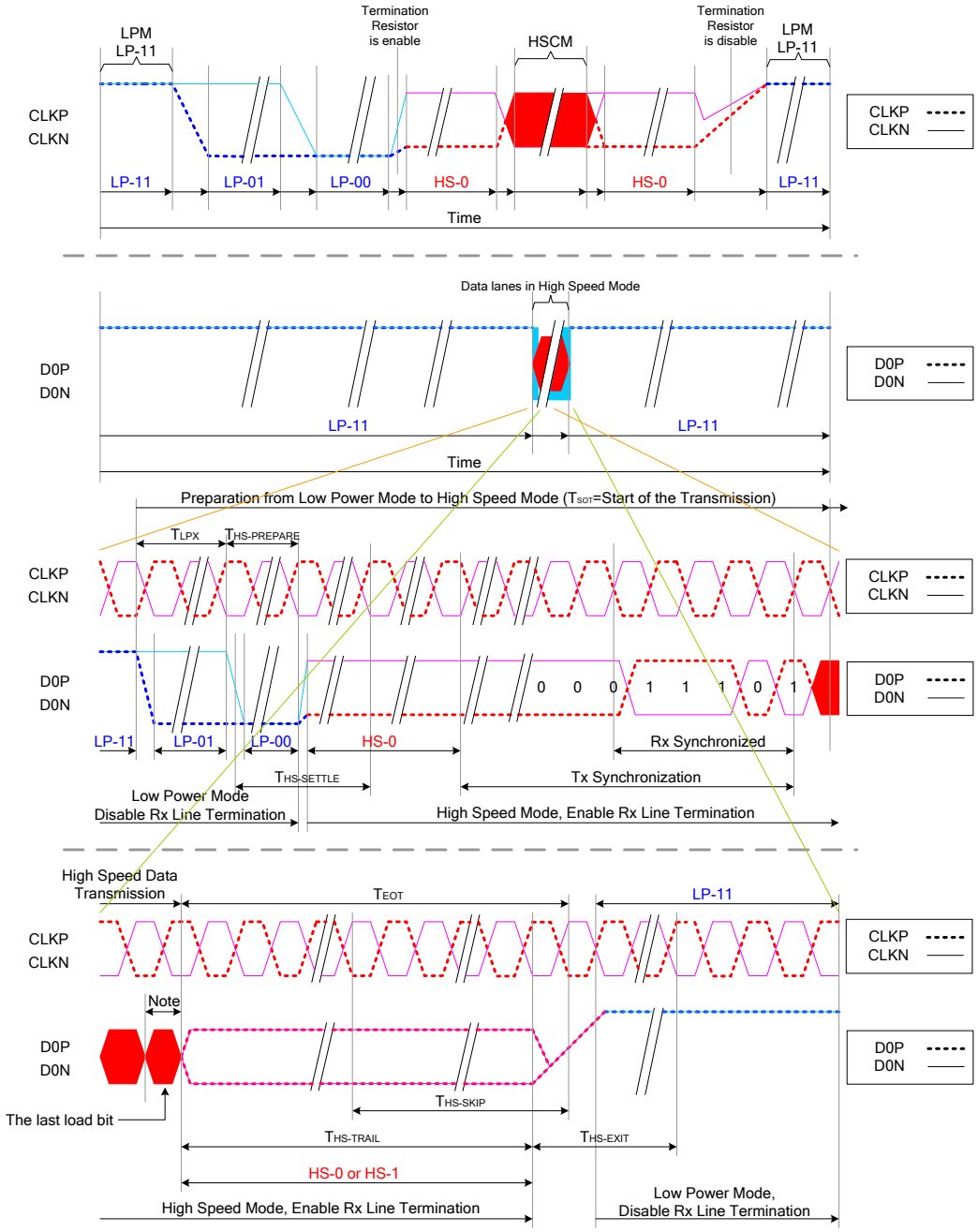


Figure 11: High Speed Clock Burst

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.4.2.3. DSI Data Lanes

4.4.2.3.1. General

D0P/N Data Lanes can be driven into different modes:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined in the following table.

Table 5: Entering and Leaving Sequences

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode[1]	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission[2]	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request[3]	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

4.4.2.3.2. Escape Modes

D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which can reset the display module,
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction is illustrated below:

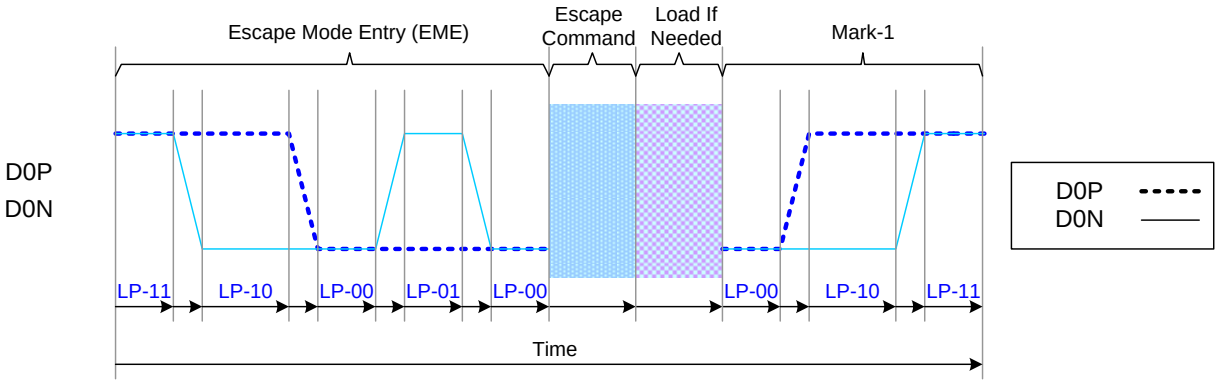


Figure 12 General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in Table 6: Escape Commands.

An example of the Mode type Escape Command is 'Ultra-Low Power Mode', where the MCU instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Table 6: Escape Commands

Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	D0
Low-Power Data Transmission	Mode	1110 0001 b	X
Ultra-Low Power Mode	Mode	0001 1110 b	X
Undefined-1, Note 1	Mode	1001 1111 b	-
Undefined-2, Note 1	Mode	1101 1110 b	-
Remote Application Reset	Trigger	0110 0010 b	X
Acknowledge	Trigger	0010 0001 b	X
Unknown-5, Note 1	Trigger	1010 0000 b	-

Notes:

1. This Escape command support is not implemented on the display module.

2. x = Supported

3. - = Not Supported

4.4.2.3.2.1. Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module. The display module also uses the same sequence when it sends data to the MCU. The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
  - ✧ One or more bytes (one byte = 8 bit)
  - ✧ Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (LP-11 timing≧300ns)

This sequence is illustrated for reference purposes below:

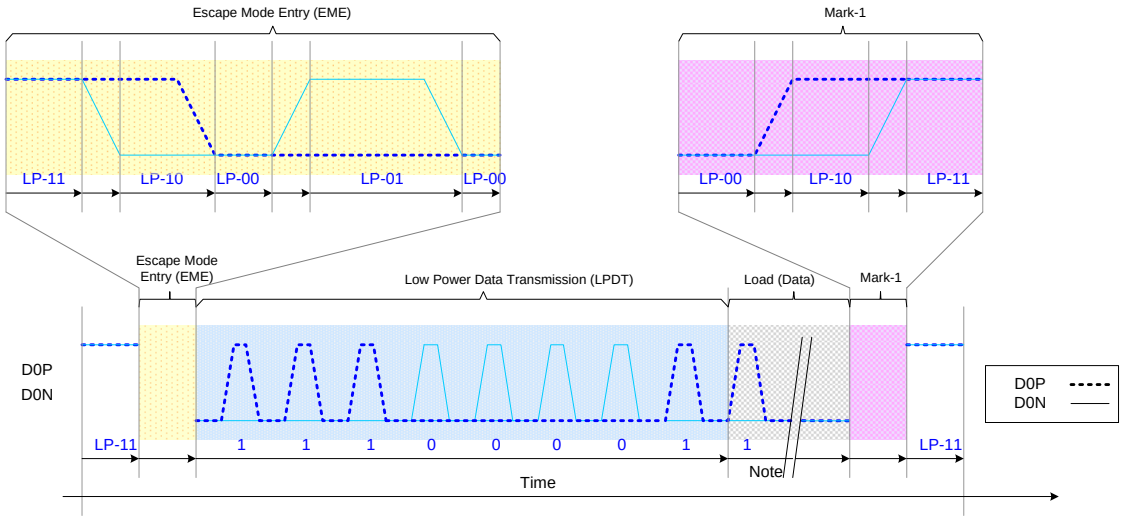


Figure 13: Low-Power Data Transmission (LPDT)

Note 1: *Load (Data) presents that the first bit is the logical 1 in this example.*

Note 2 *：End LP-11 timing≧300ns*

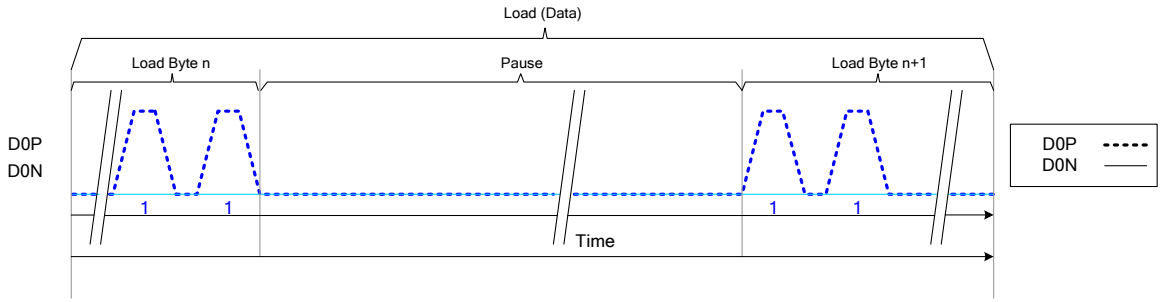


Figure 14: Pause (Example)

4.4.2.3.2.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS)

This sequence is illustrated for reference purposes below:

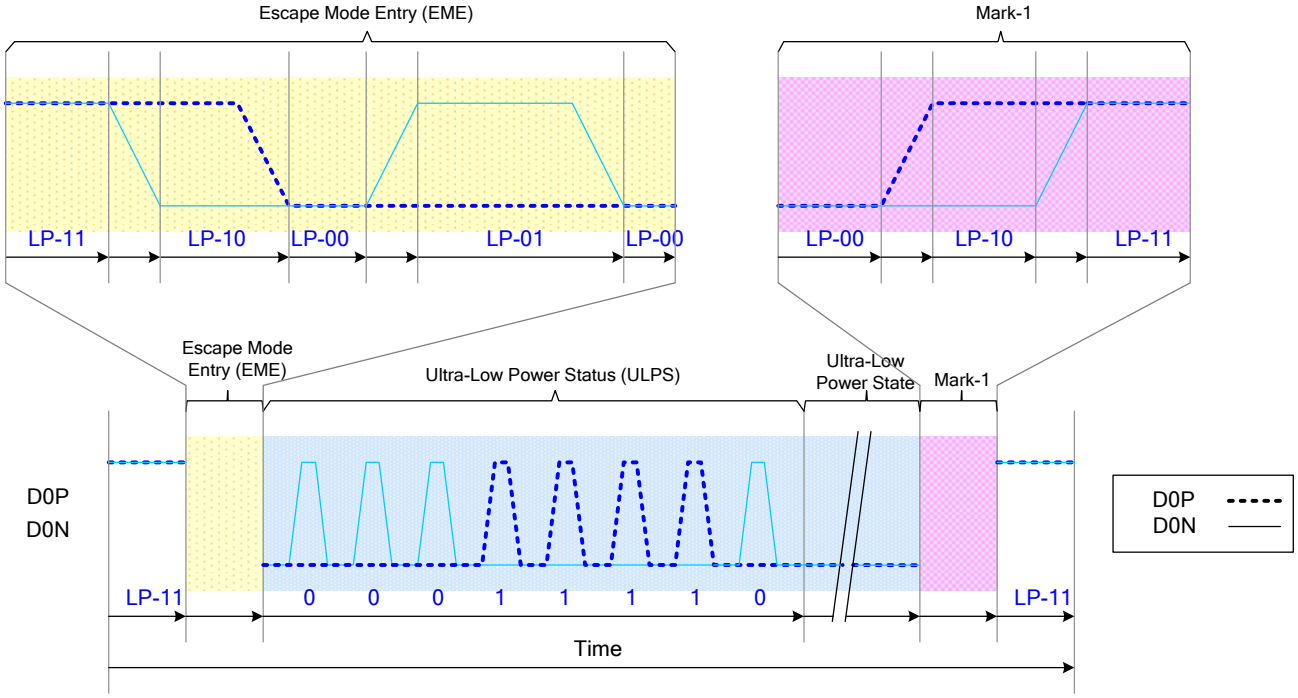


Figure 15: Ultra-Low Power State (ULPS)

4.4.2.3.2.3. Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

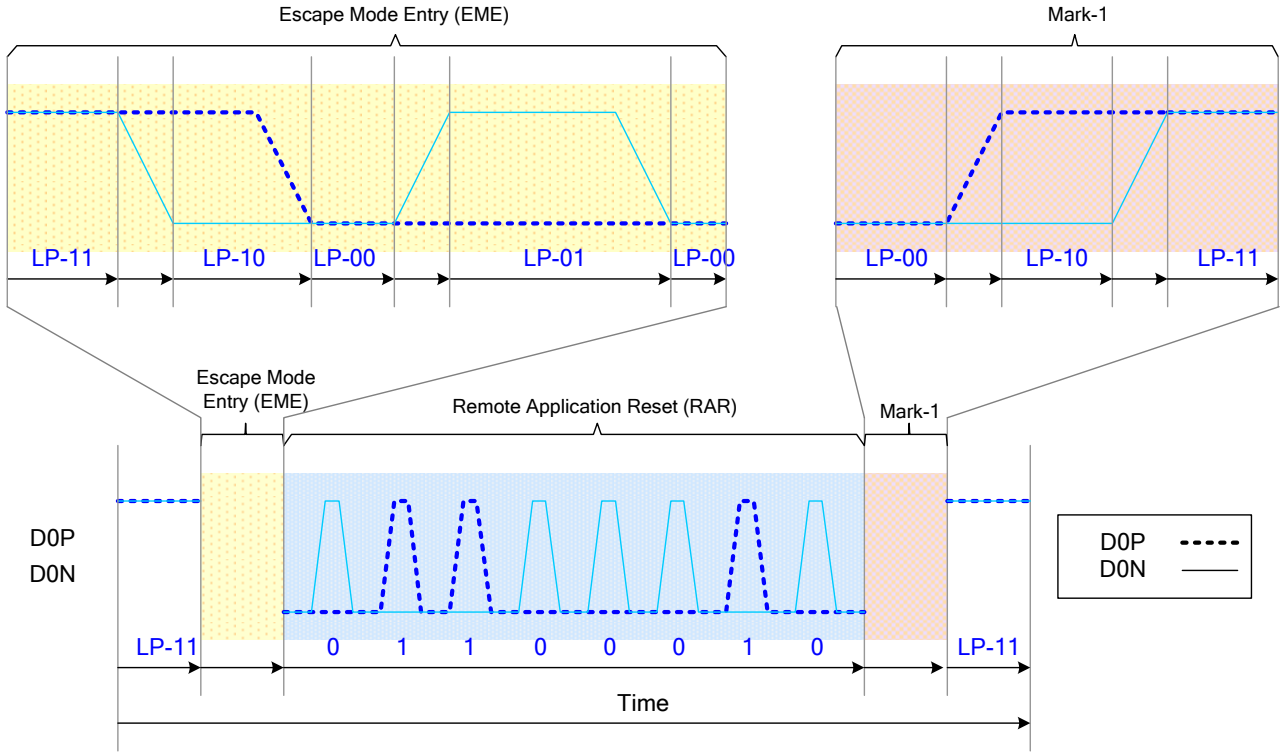


Figure 16: Remote Application Reset (RAR)

4.4.2.3.2.4. Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

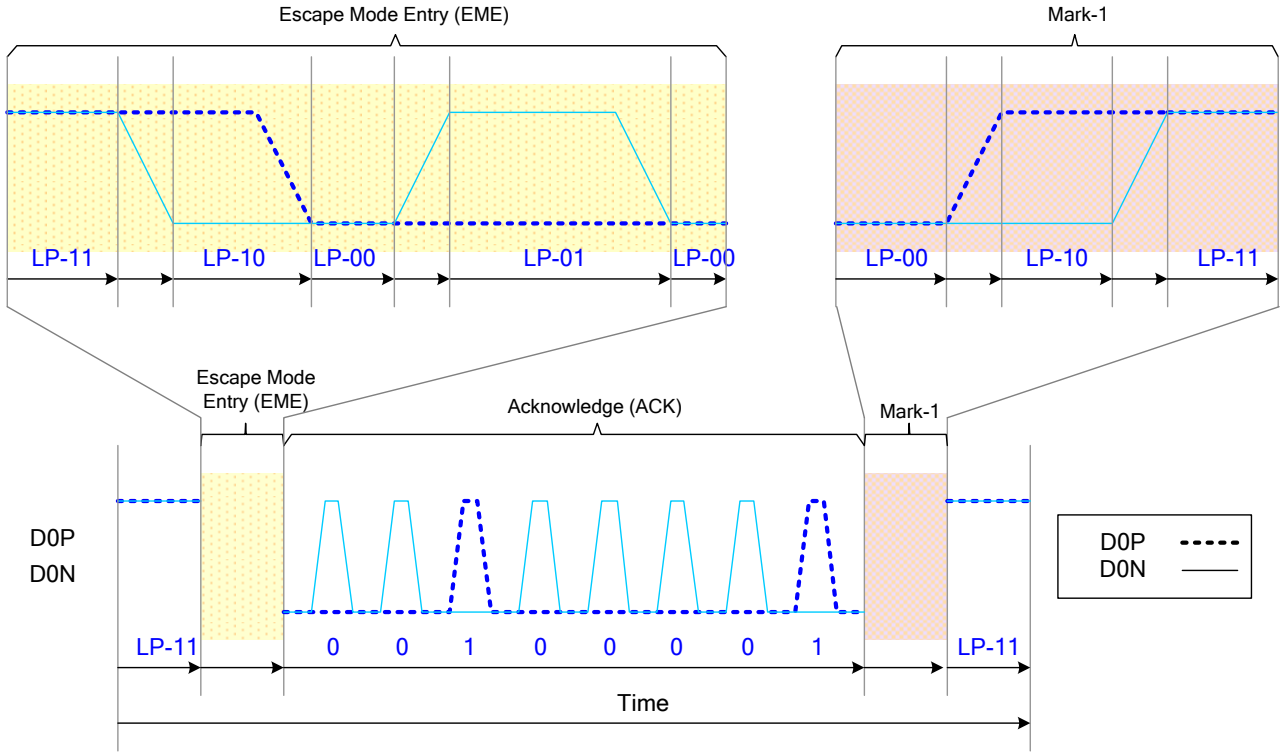


Figure 17: Acknowledge (ACK)

4.4.2.3.3. High-Speed Data Transmission (HSDT)

4.4.2.3.3.1. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section "4.4.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes D0P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

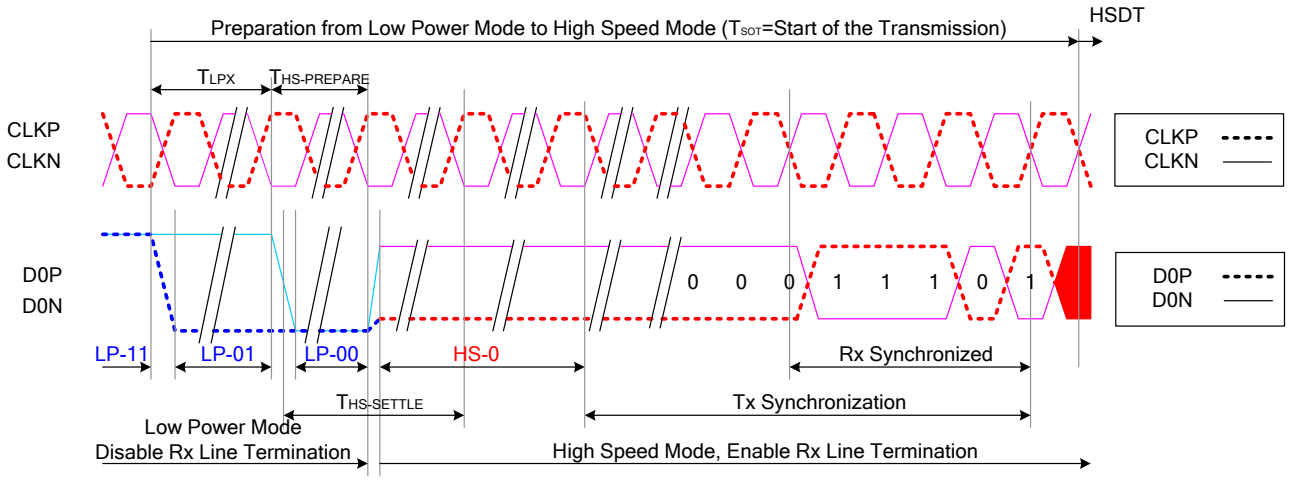


Figure 18: Entering High-Speed Data Transmission (TSOT of HSDT)

4.4.2.3.3.2. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lanes D0P/N are in the LP-11 mode. See more information in the section "4.4.2.2.3 High-Speed Clock Mode (HSCM)". Data lanes D0P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - ✧ MCU changes to HS-1, if the last load bit is HS-0
  - ✧ MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:

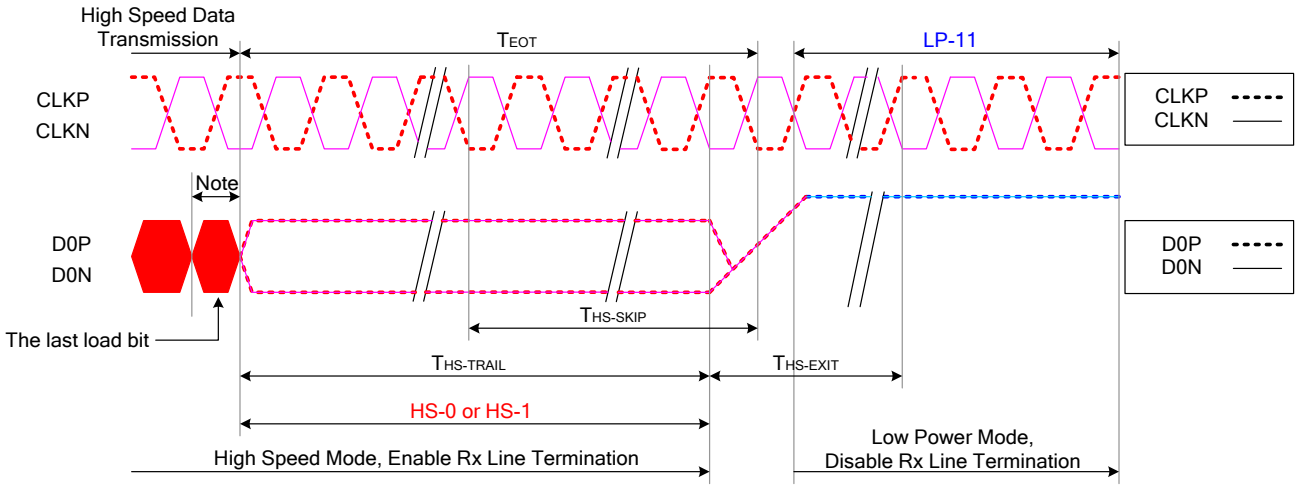


Figure 19: Leaving High-Speed Data Transmission (TEOT of HSDT)

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.4.2.3.3.3. Burst of the High-Speed Data Transmission (HSDT)

The burst of the "High-Speed Data Transmission" (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section "4.4.3.1 Short Packet (SPa) and Long Packet (LPa) Structures". These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

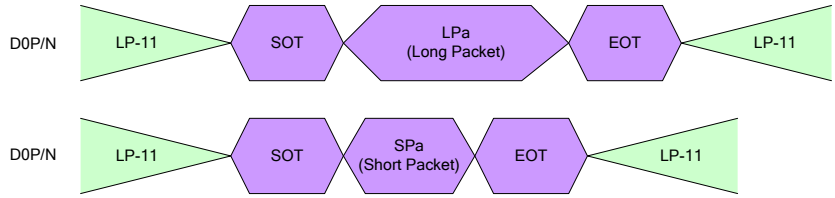


Figure 20: Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:

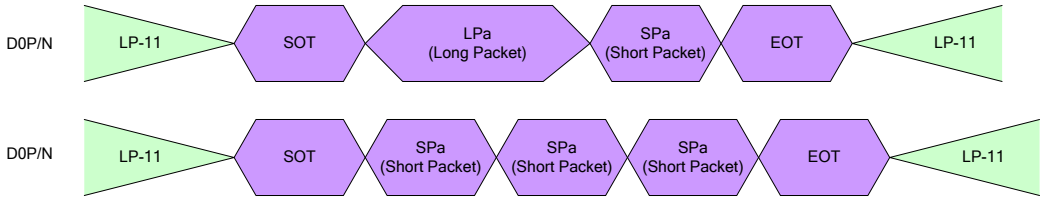


Figure 21: Multiple Packets in High-Speed Data Transmission – Examples

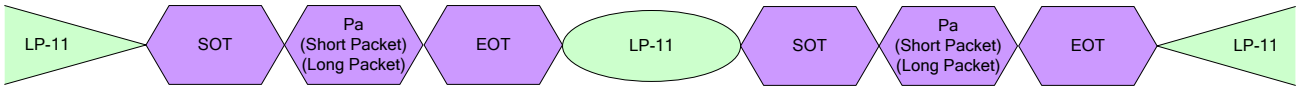


Figure 22: Continuous Packets in High-Speed Data Transmission – Examples

Note：LP-11 keep timing≧300ns

Table 7: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are '1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

4.4.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module.

The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

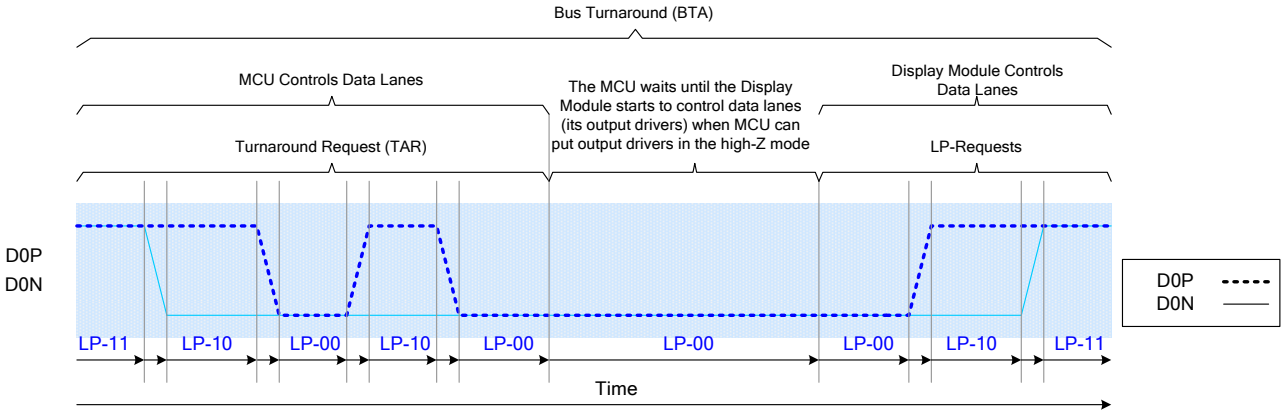


Figure 23: Bus Turnaround Procedure

MCU and display module terms can be switched in Figure 23 if the Bus Turnaround (BTA) is from the display module to the MCU.

4.4.3. Packet Level Communication

4.4.3.1. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

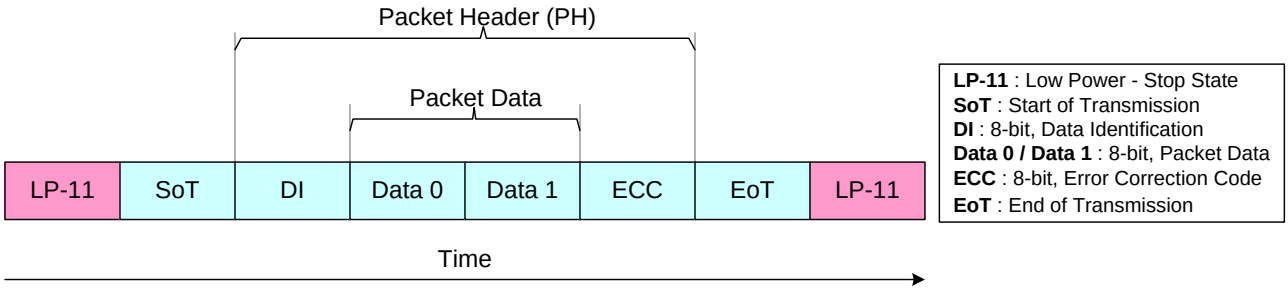


Figure 24: Short Packet (SPa) Structure

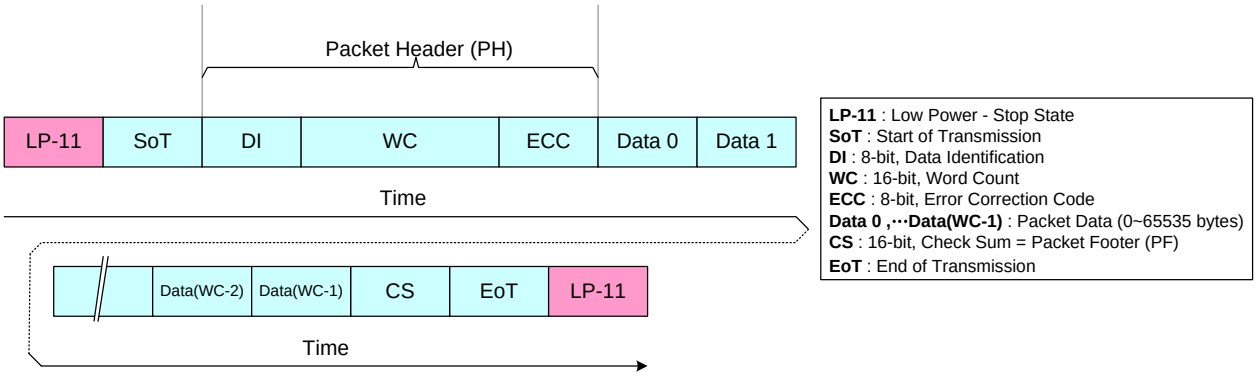


Figure 25: Long Packet (LPa) Structure

Notes:

1. *Figure 24 and Figure 25 present a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).*
2. *The other possibility is that SoT, EoT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g.*
   - *LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11*
   - *LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11*
   - *LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11*

4.4.3.1.1. Bit Order of the Byte on Packets

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

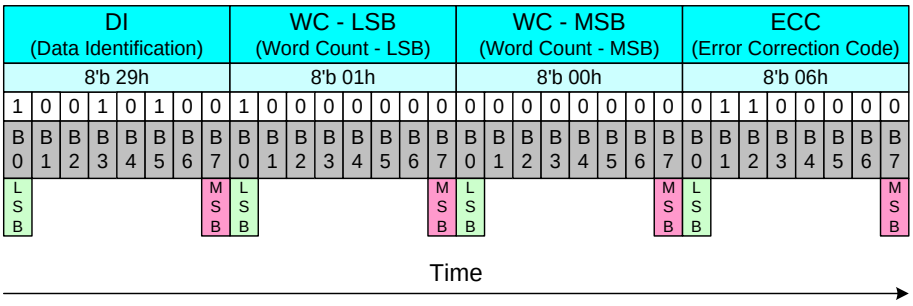


Figure 26: Bit Order of the Byte on Packets

4.4.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

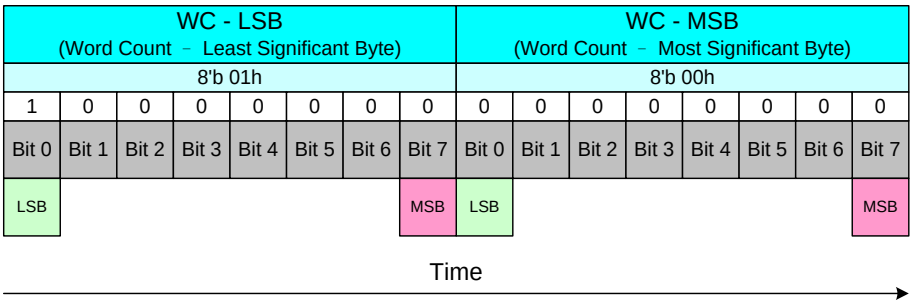


Figure 27: Byte Order of the Multiple Byte Information on Packets

4.4.3.1.3. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

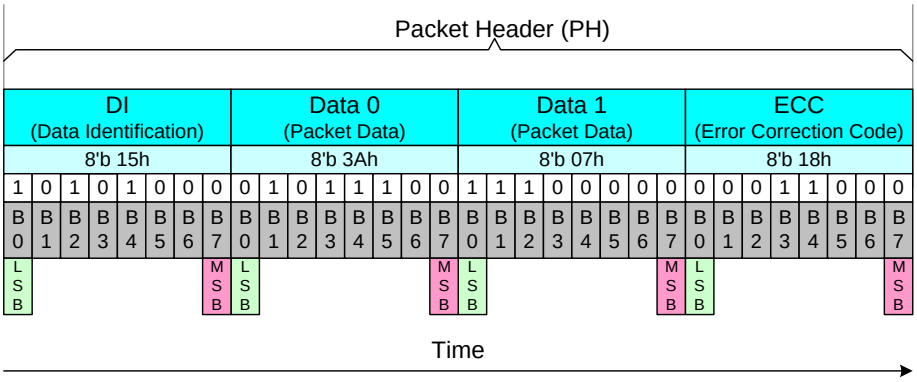


Figure 28: Packet Header (PH) in a Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

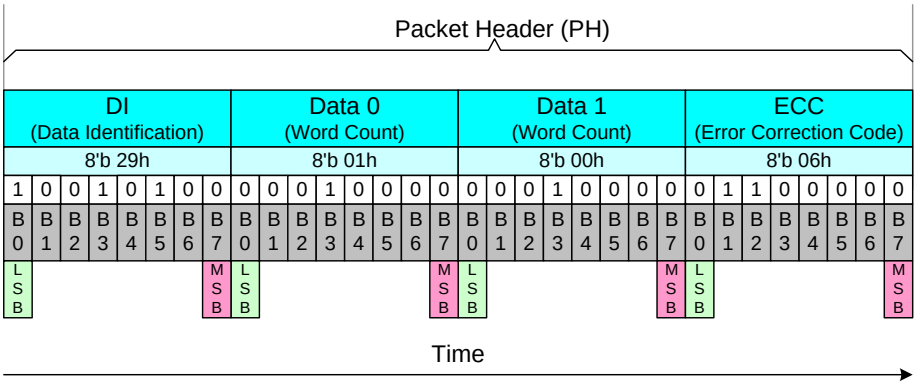


Figure 29: Packet Header (PH) in a Long Packet (LPa)

4.4.3.1.3.1. Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7…6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated, see the figure below.

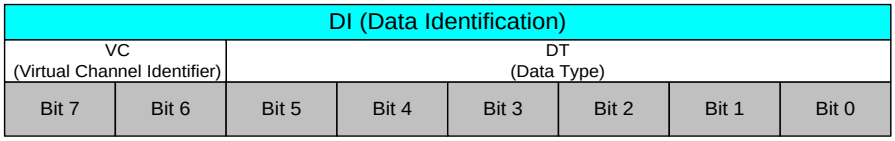


Figure 30: Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

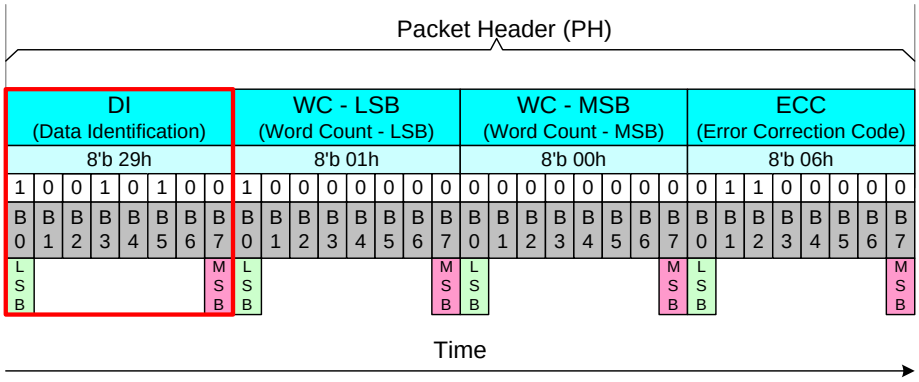


Figure 31: Data Identification (DI) on the Packet Header (PH)

4.4.3.1.3.1.1. Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

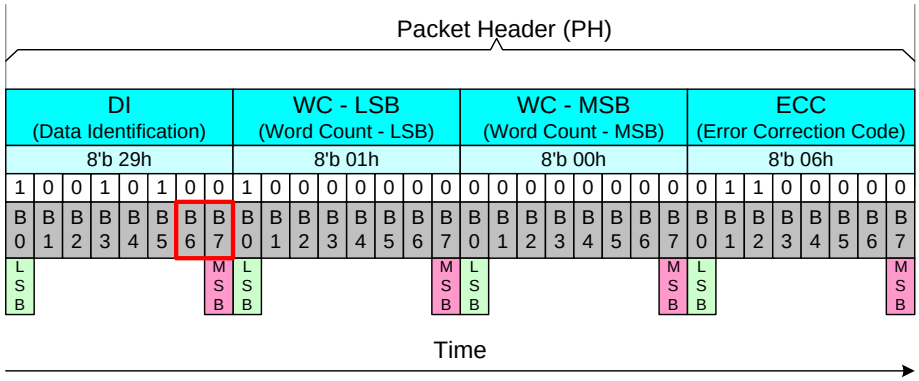


Figure 32: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

- The MCU uses the virtual channel 0 when it sends packets to the ILI9342E
- The ILI9342E also uses the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

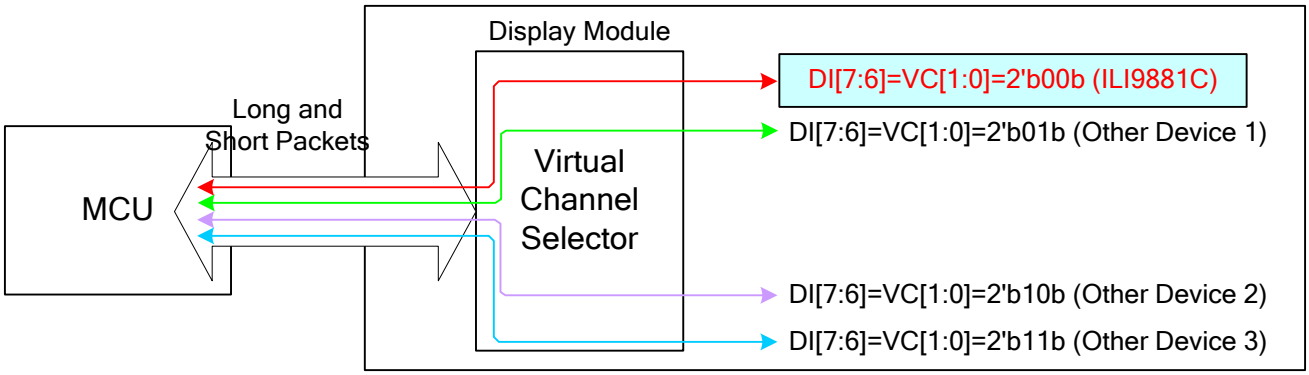


Figure 33: Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI [7..6] = VC [1..0] = 00b) when the MCU sends "End of Transmission Packet" to the display module. See the section "4.4.3.2.1.7 End of Transmission Packet (EoTP)".

This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1..0]) is 00b for the ILI9342E.

4.4.3.1.3.1.2. Data Type (DT)

Data Type (DT) is a part of Data Identification (DI [5…0]) structure, and it is used to define the type of the used data in a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.

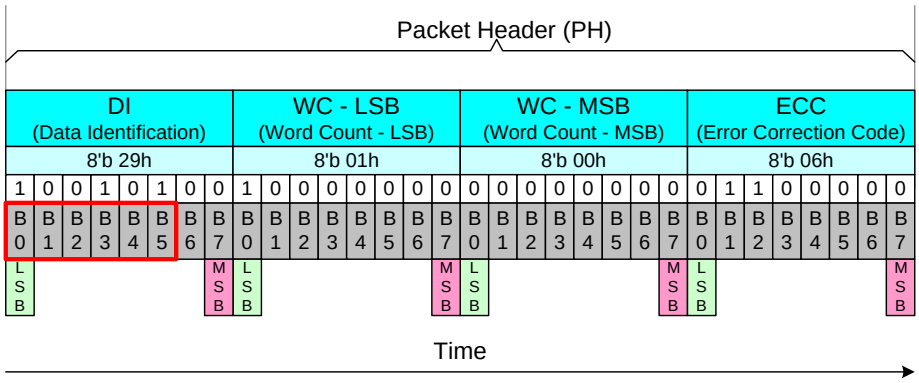


Figure 34: Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables below.

Table 8: Data Type (DT) from the MCU to the Display Module

From the MCU to the Display Module								
Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Hex**	**Description**	**Short/Long Packet**
0	0	0	0	0	1	01	Sync Event, V Sync Start	SPa (Short Packet)
0	1	0	0	0	1	11	Sync Event, V Sync End	SPa (Short Packet)
1	0	0	0	0	1	21	Sync Event, H Sync Start	SPa (Short Packet)
1	1	0	0	0	1	31	Sync Event, H Sync End	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP) Note1	SPa (Short Packet)
0	0	0	0	1	0	02	Color Mode Off Command	SPa (Short Packet)
0	1	0	0	1	0	12	Color Mode On Command	SPa (Short Packet)
1	0	0	0	1	0	22	Shut Down Peripheral Command	SPa (Short Packet)
1	1	0	0	1	0	32	Turn On Peripheral Command	SPa (Short Packet)
0	0	0	0	1	1	03	Generic Short WRITE, no parameters	SPa (Short Packet)
0	1	0	0	1	1	13	Generic Short WRITE, 1 parameters	SPa (Short Packet)
1	0	0	0	1	1	23	Generic Short WRITE, 2 parameters	SPa (Short Packet)
0	0	0	1	0	0	04	Generic Short READ, no parameters	SPa (Short Packet)
0	1	0	1	0	0	14	Generic Short READ, 1 parameters	SPa (Short Packet)
1	0	0	1	0	0	24	Generic Short READ, 2 parameters	SPa (Short Packet)
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)
0	0	1	0	0	1	09	Null Packet, No Data, Note2	LPa (Long Packet)
0	1	1	0	0	1	19	Blanking Packet, no data	LPa (Long Packet)
1	0	1	0	0	1	29	Generic Long Write	LPa (Long Packet)
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)
0	0	1	1	1	0	0E	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	LPa (Long Packet)
0	1	1	1	1	0	1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	0	1	1	1	0	2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	1	1	1	1	0	3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
x	x	0	0	0	0	x0	DO NOT USE	
x	x	1	1	1	1	xF	All unspecified codes are reserved	

Notes:

1. *This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.*
2. *This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.*

Table 9: Data Type (DT) from the Display Module to the MCU

From the Display Module to the MCU								
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP)	SPa (Short Packet)
0	1	0	0	0	1	11	Generic Short READ Response, 1 byte returned	SPa (Short Packet)
0	1	0	0	1	0	12	Generic Short READ Response, 2 byte returned	SPa (Short Packet)
0	1	1	0	1	0	1A	Generic Long READ Response	LPa (Long Packet)
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)

The receiver will ignore other Data Types (DT) if they are not defined in Table 8 and Table 9.

4.4.3.1.3.2. Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

Packet Data (PD) information:

• Data 0: 26hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

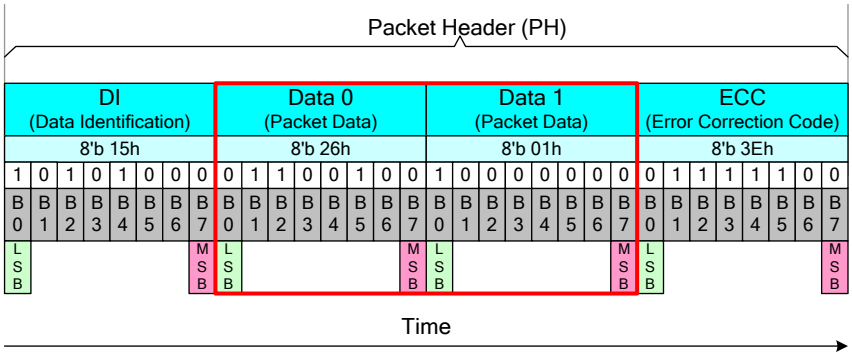


Figure 35: Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

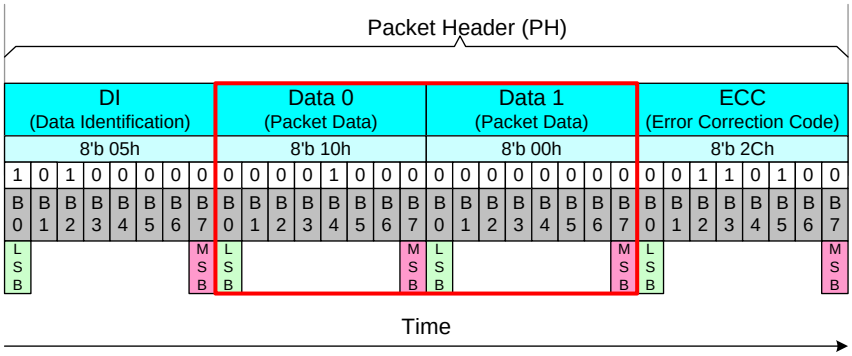


Figure 36: Packet Data (PD) for Short Packet (SPa), 1 Byte Information

4.4.3.1.3.3. Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 38. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

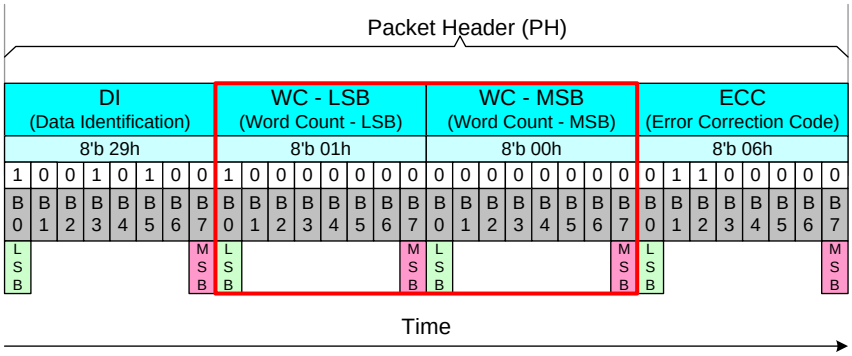


Figure 37: Word Count (WC) in a Long Packet (LPa)

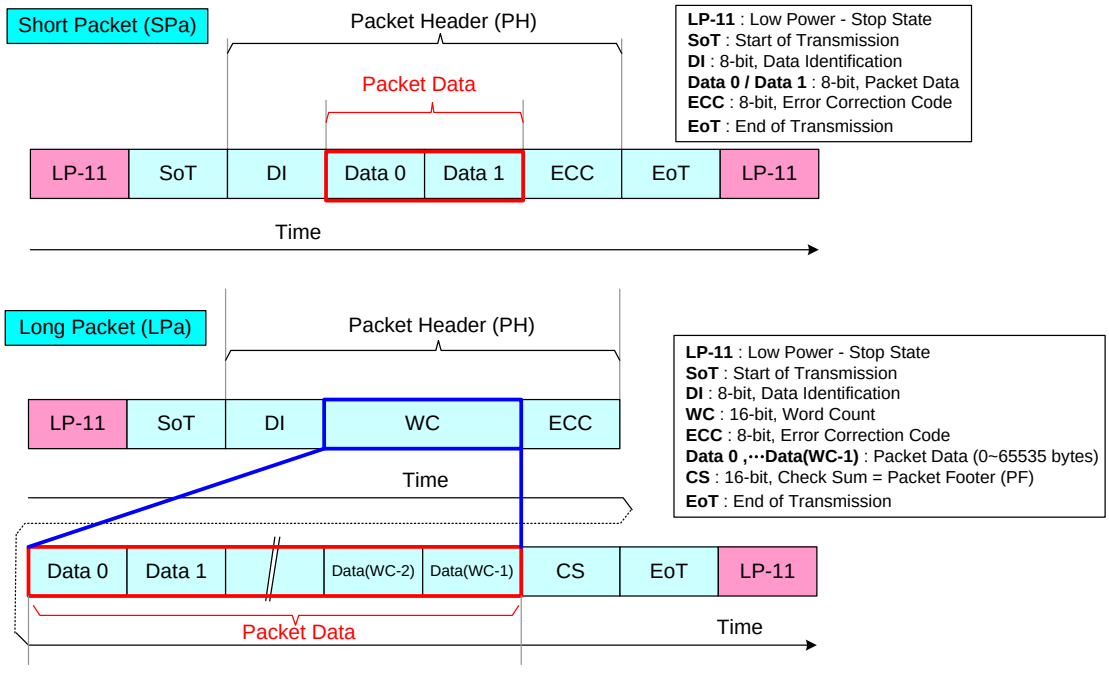


Figure 38: Packet Data in Short and Long Packets

4.4.3.1.3.4. Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0…7]), Packet Data (PD) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0…7]), Word Count (WC) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])

D [23…0] and P [7…0] are illustrated for reference purposes below.

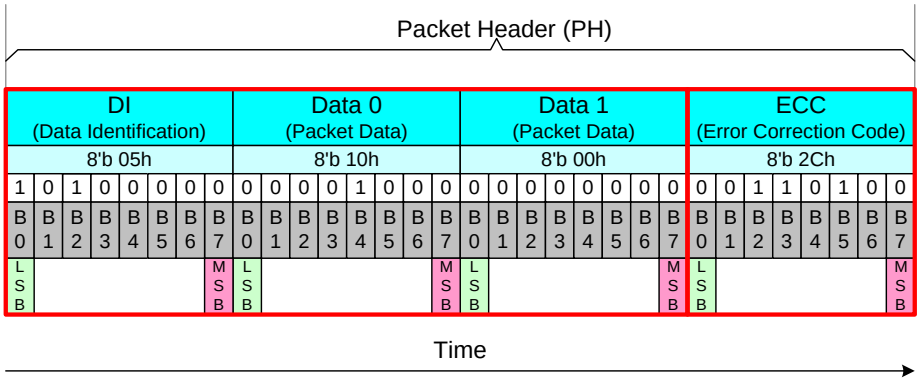


Figure 39: D [23…0] and P [7…0] in a Short Packet (SPa)

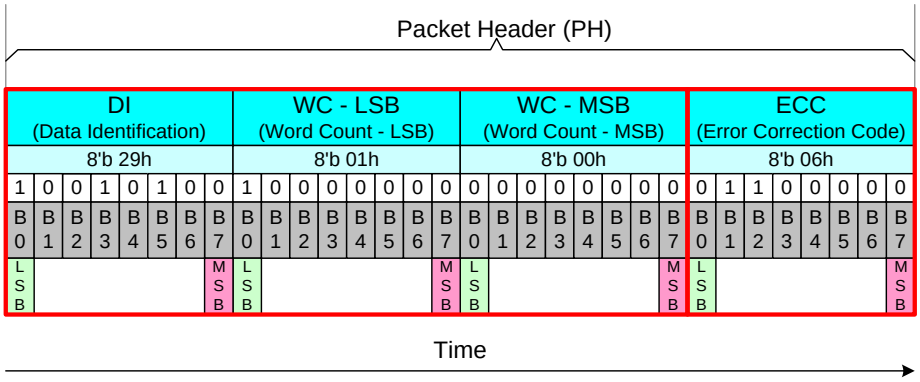


Figure 40: D [23…0] and P [7…0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits are needed (P [5…0]) for Error Correction Code (ECC).

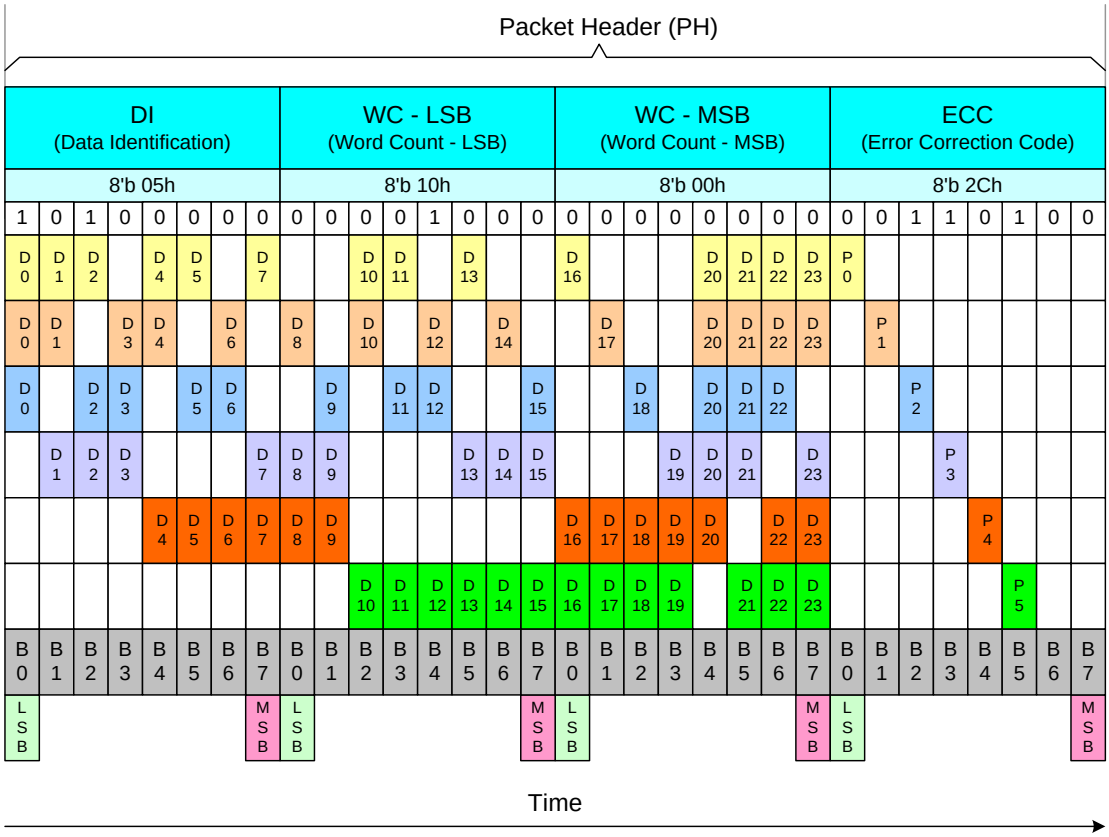


Figure 41: XOR Function on a Short Packet (SPa)

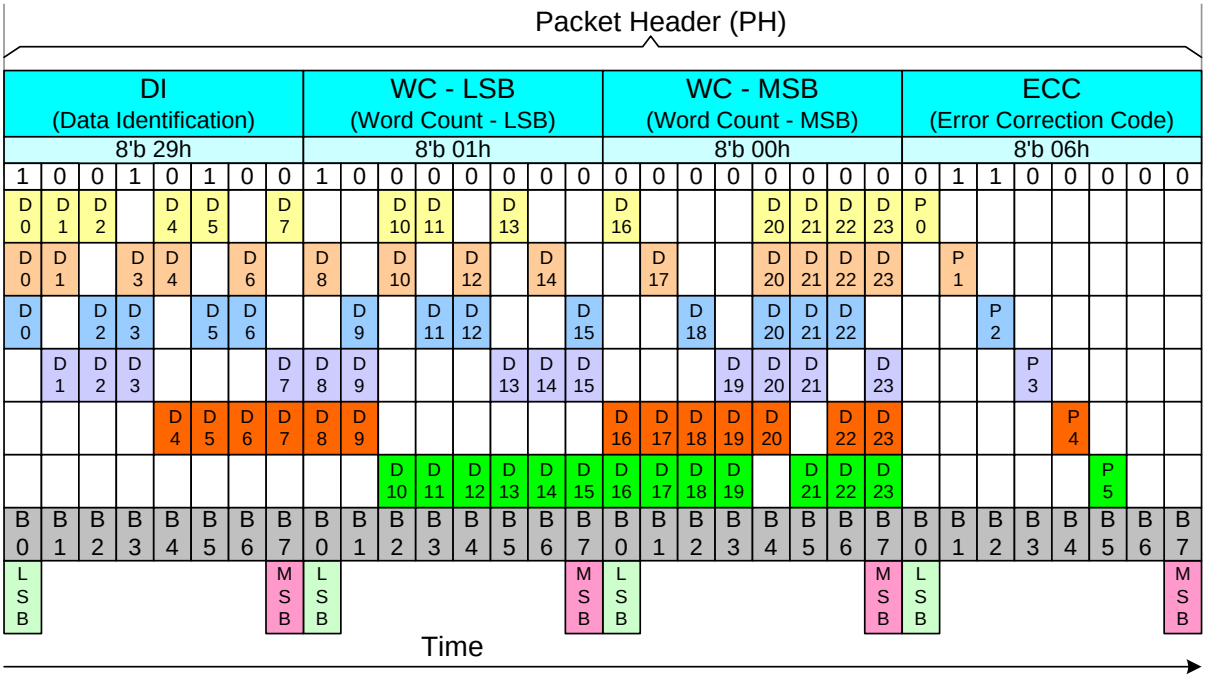


Figure 42: XOR Function on a Long Packet (LPa)

The transmitter (= the MCU or the Display Module) will send data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (= the Display module or the MCU) will calculate the Internal Error Correction Code (IECC) and compare the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

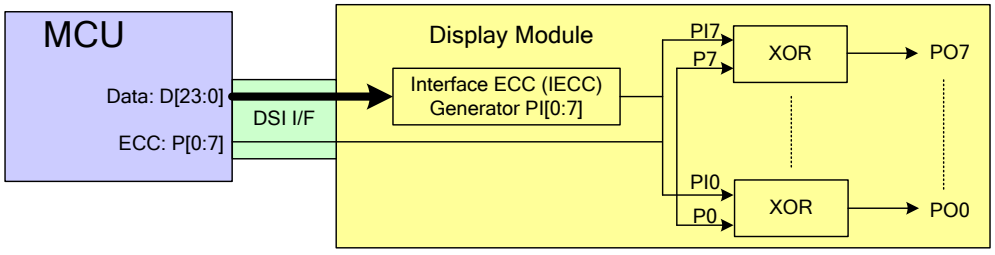


Figure 43: Internal Error Correction Code (IECC) on the Display Module (= the Receiver)

The sent data bits (D [23…0]) and ECC (P [7…0]) are correctly received if the value of the PO [7…0]) is 00h. The sent data bits (D [23…0]) and ECC (P [7…0]) are not correctly received if the value of the PO [7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 44: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 45: Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D [23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to the values in the following table.

Table 10: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO [7…0] is in Table 10, and the receiver can correct this one bit error because this found value also defines the location of the corrupt bit, e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), that is not correct, is D [3]

More than one error is detected if the value of the PO [7…0] is not in Table 10,for example, PO [7…0] = 0Ch.

4.4.3.1.4. Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section "4.4.3.1.3.3 Word Count (WC) in a Long Packet (LPa)".

4.4.3.1.5. Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial X16+X12+X5+X0, as illustrated below.

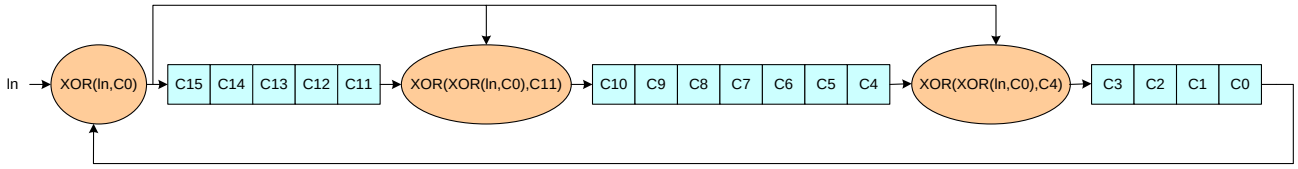
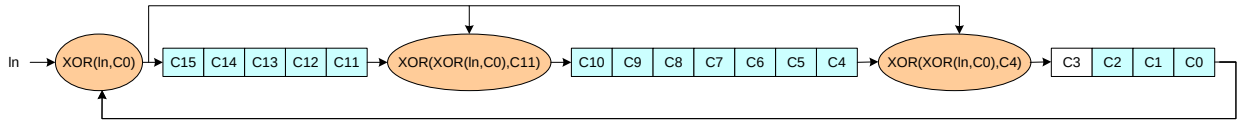


Figure 46: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 47: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated below.

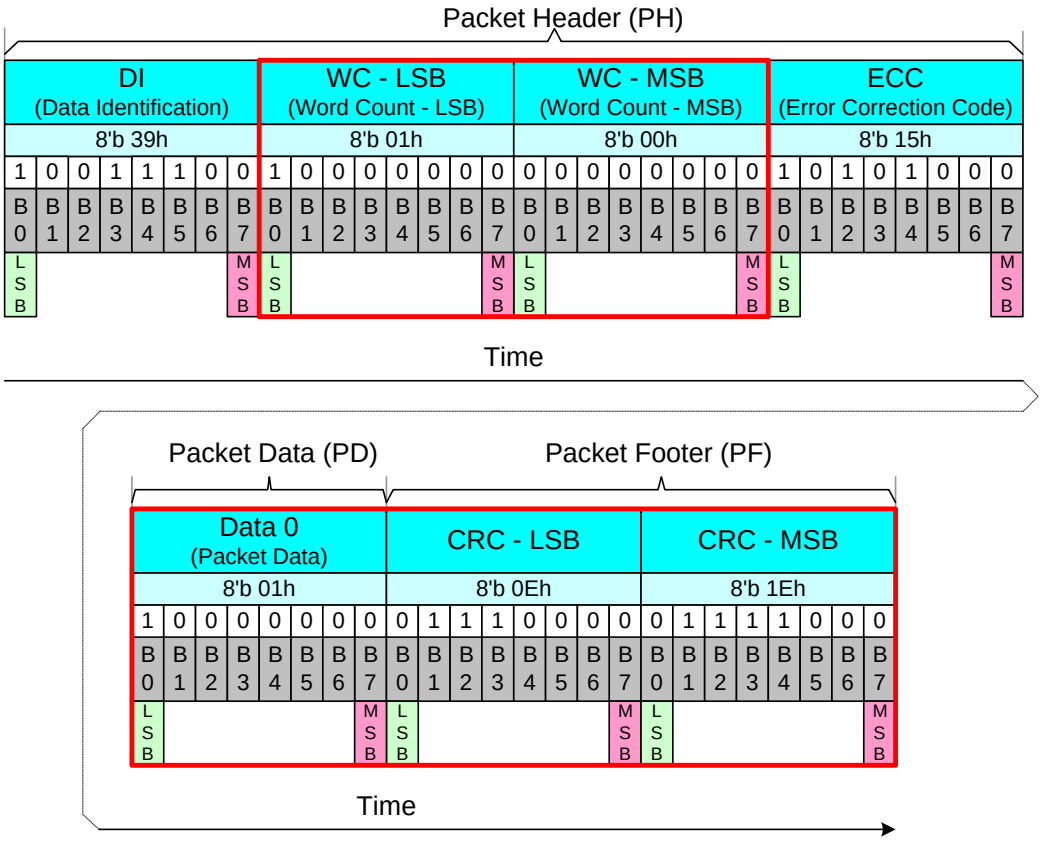


Figure 48: Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

4.4.3.2. Packet Transmissions

4.4.3.2.1. Packet from the MCU to the Display Module

4.4.3.2.1.1. Display Command Set (DCS)

Display Command Set (DCS), defined in the section, is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.

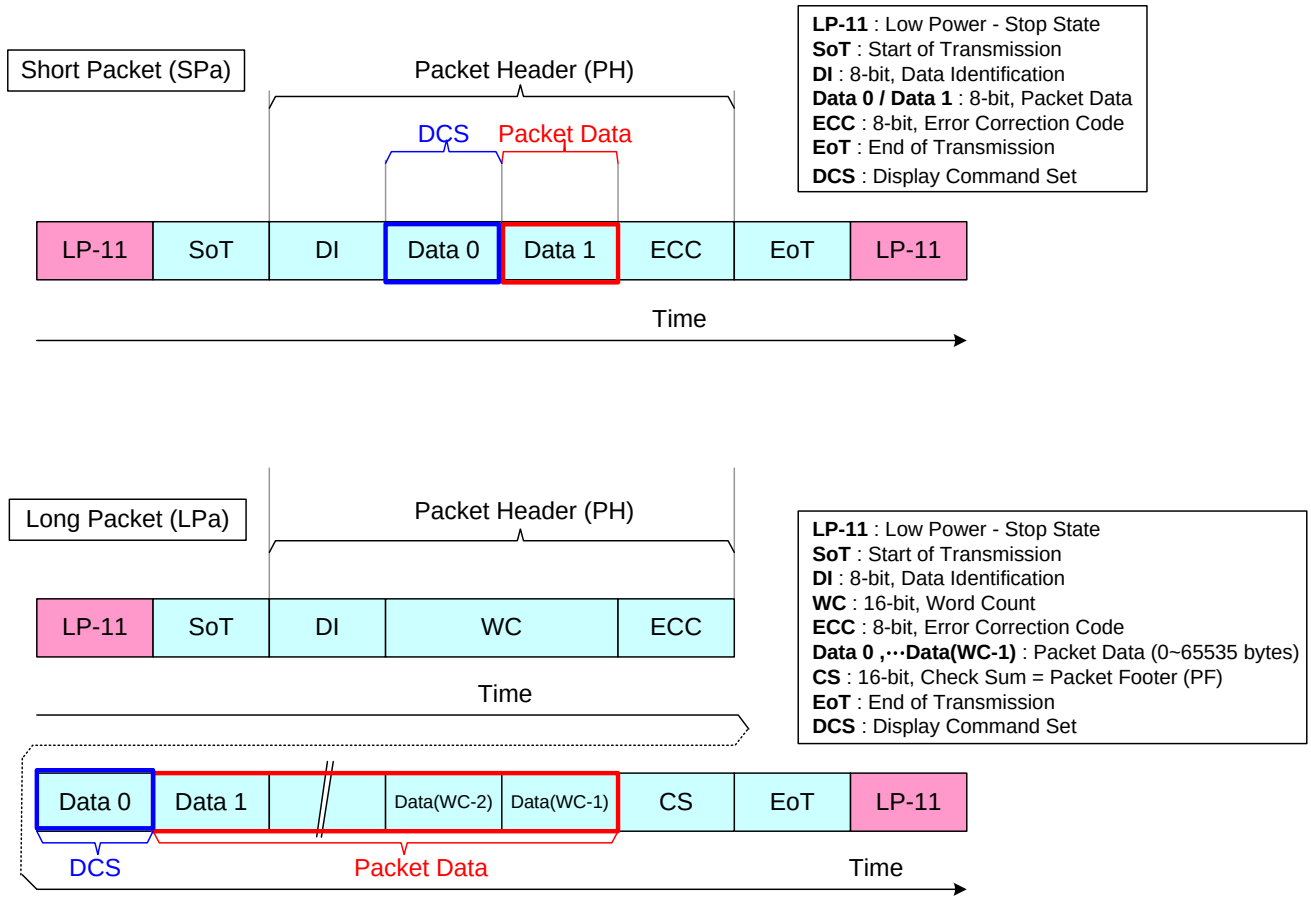


Figure 49: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

4.4.3.2.1.2. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter", which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below.

Table 11: Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
Display Off (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode Off (38h)
Idle Mode On (39h)
Stop Transition (59h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0101b
- Packet Data (PD)
  - ✧ Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

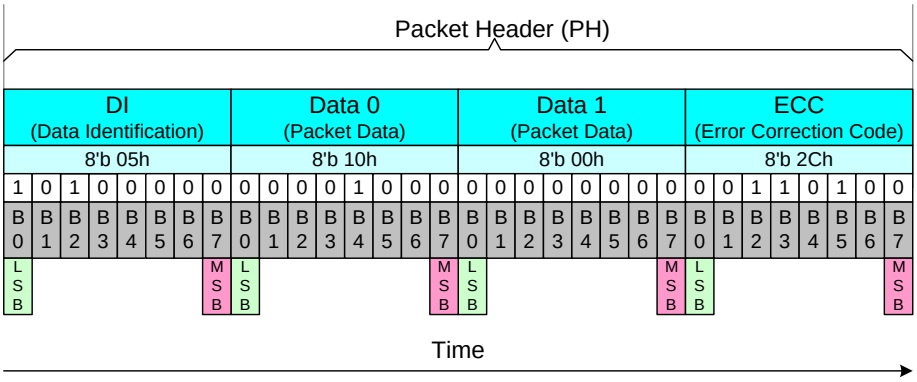


Figure 50: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

4.4.3.2.1.3. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S), which is defined in Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 12: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Command
Gamma Curve Set (26h)
Memory Write (2Ch), Note
Tearing Effect Line ON(35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Power Save (55h)
Write Idle Mode Color (80h)

Note: One Subpixel has been written

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 01 0101b
- Packet Data (PD)
  - ✧ Data 0: "Gamma Set (26h)", Display Command Set (DCS)
  - ✧ Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

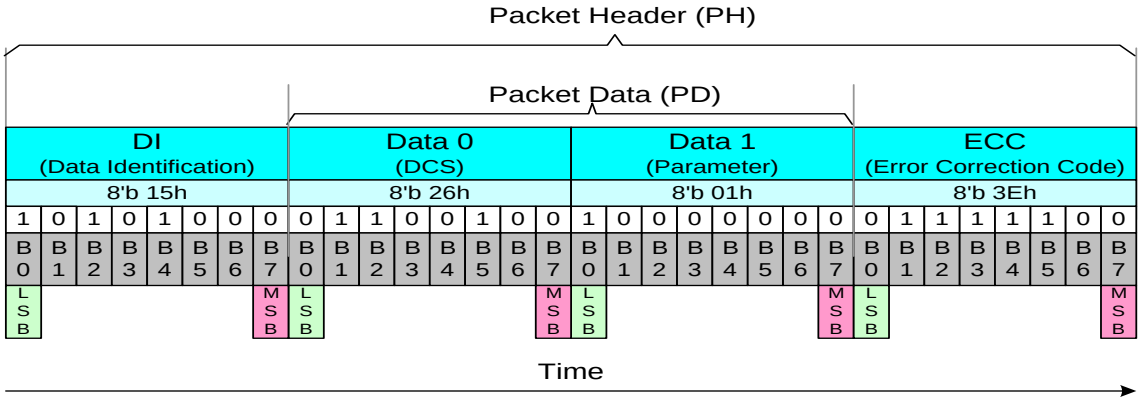


Figure 51: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

4.4.3.2.1.4. Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

Table 13: Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h), Note 1
Software Reset (01h), Note 1
Sleep In(10h), Note 1
Sleep Out (11h), Note 1
Normal Display Mode On (13h), Note 1
Gamma Curve Set (26h), Note 2
Display Off (28h), Note 1
Display ON (29h), Note 1
Memory Write (2Ch), Note 2
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode Off (38h) , Note 1
Idle Mode On (39h) , Note 1
Interface Pixel Format (3Ah), Note 2
Memory Write Continue (3Ch), Note 2
Set Tear Scan Line(44h)
Write Display Brightness (51h), Note 2
Write CTRL Display (53h), Note 2
Write Power Save(55h), Note 2
Stop Transition (59h), Note 1
Write CABC Minimum Brightness (5Eh) , Note 2
Set Transition Time(68h)
Write Idle Mode Color (80h), Note 2

Notes:

1. Short Packet (SPa) can also be used; See the section "4.4.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)".

2. Short Packet (SPa) can also be used; See the section "4.4.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)".

A Long Packet (LPa) with one command (No Parameter) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

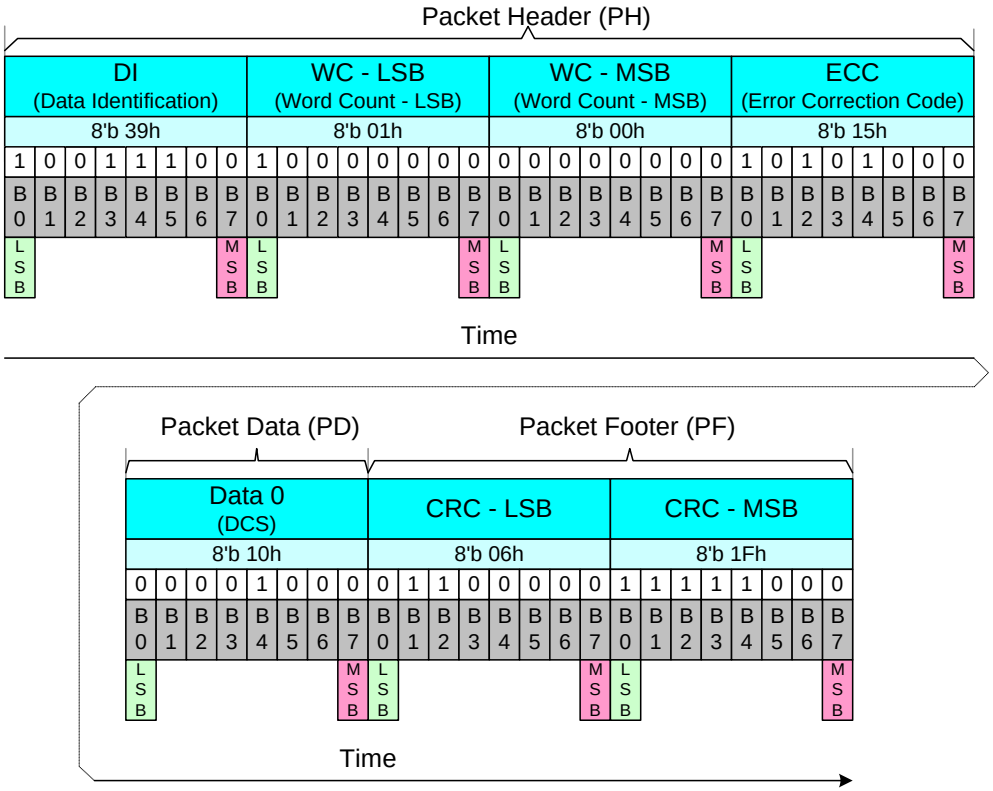


Figure 52: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - ✧ Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

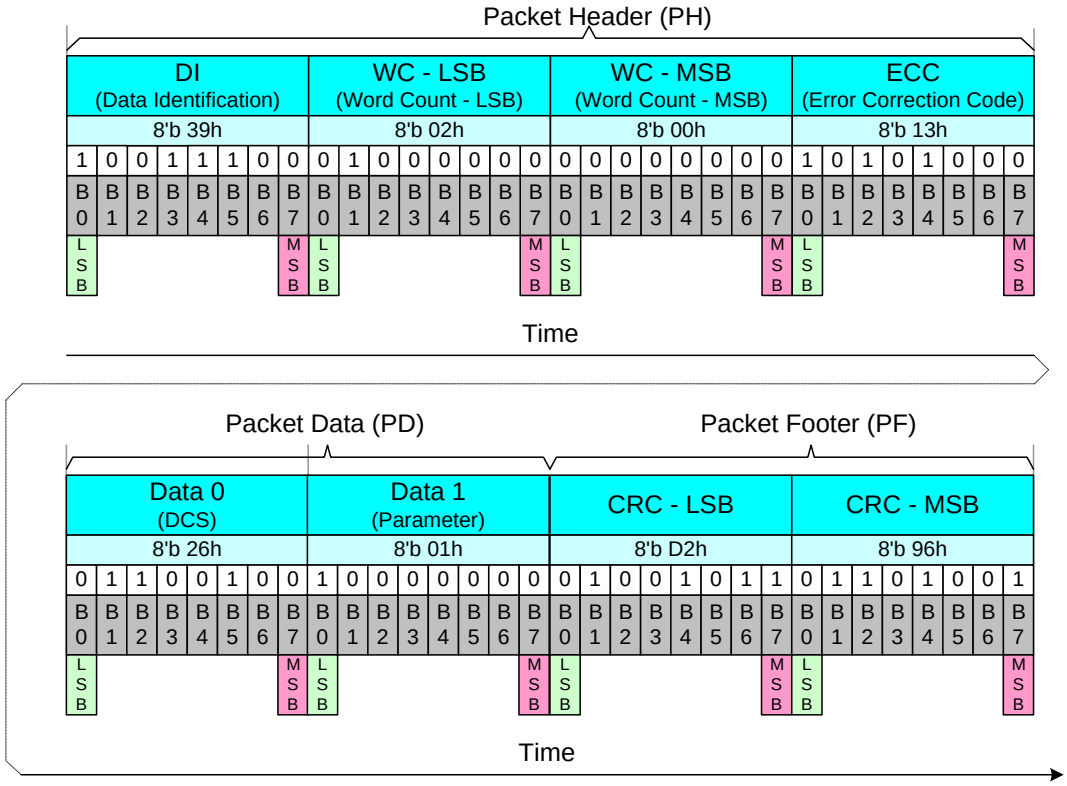


Figure 53: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

A Long Packet (LPa) with one Write (4 parameters) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: “Column Address Set (2Ah)” (For example only), Display Command Set (DCS)
  - ✧ Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
  - ✧ Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
  - ✧ Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
  - ✧ Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]
- Packet Footer (PF)

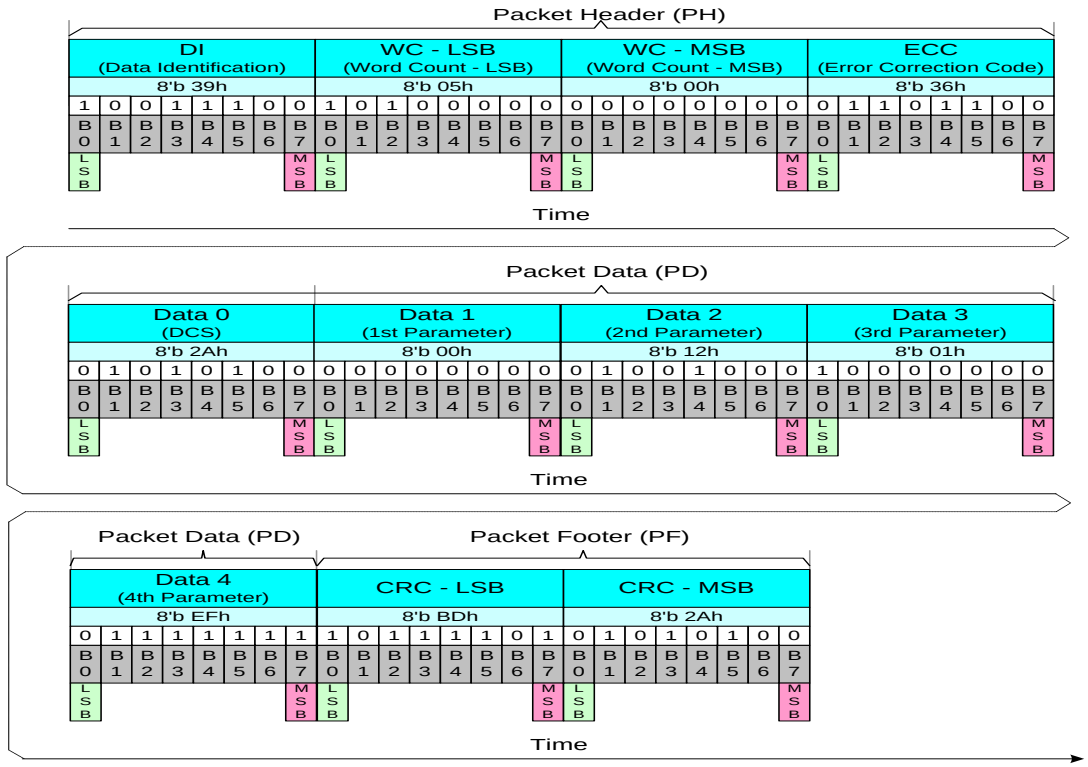


Figure 54: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

4.4.3.2.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 14: Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Get Tear Scan Line(45h)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Power Save (56h)
Read CABC Minimum Brightness (5Fh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This sequence is illustrated for reference purposes below.

Step 1:

The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - ✧ Data 0: 01hex
  - ✧ Data 1: 00hex
- Error Correction Code (ECC)

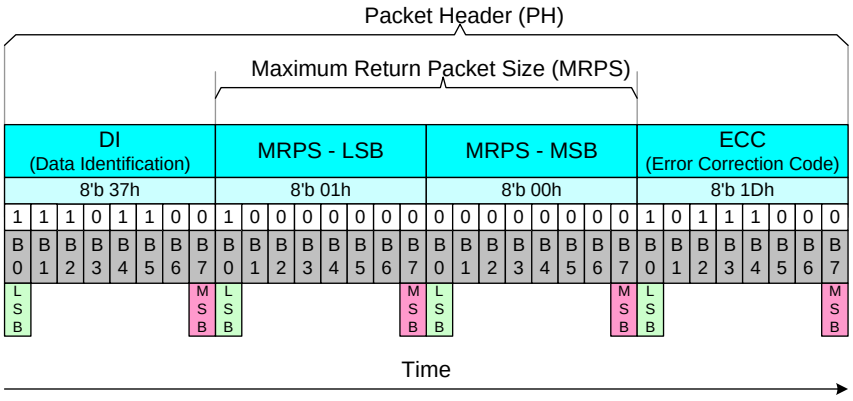


Figure 55: Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MCU wants to receive the value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module.

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0110b
- Packet Data (PD)
  - ✧ Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
  - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

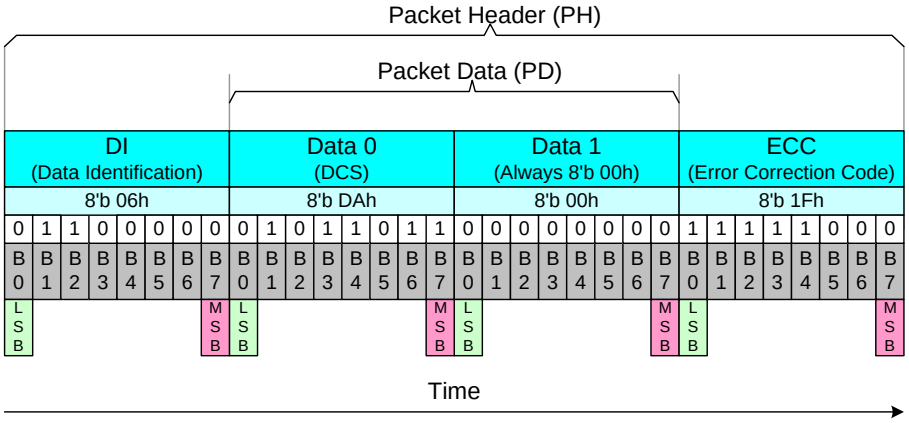


Figure 56: Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1. An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section "4.4.3.2.2.2 Acknowledge with Error Report (AwER)".
2. Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

4.4.3.2.1.6. Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: 89hex (Random data)
  - ✧ Data 1: 23hex (Random data)
  - ✧ Data 2: 12hex (Random data)
  - ✧ Data 3: A2hex (Random data)
  - ✧ Data 4: E2hex (Random data)
- Packet Footer (PF)

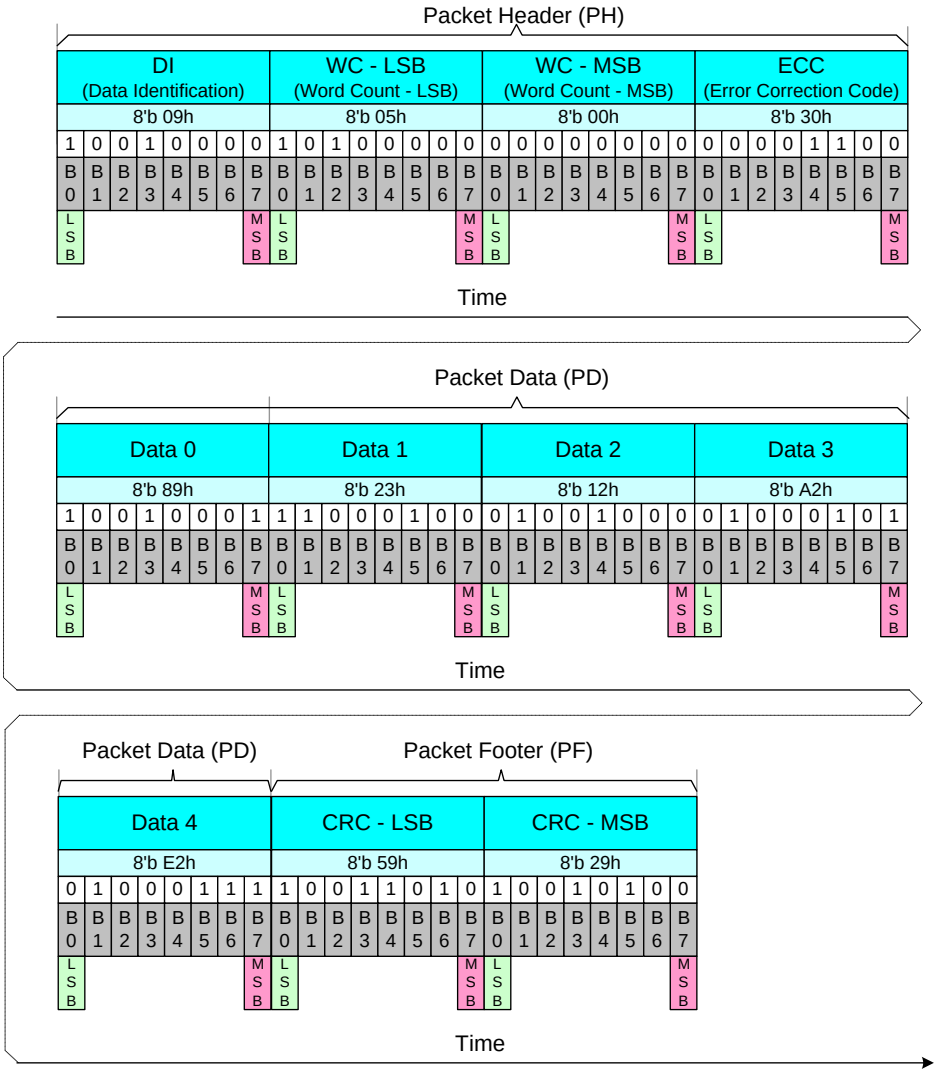


Figure 57: Null Packet, No Data (NP-L) - Example

4.4.3.2.1.7. End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before "End of Transmission" (EoT).

The MCU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module does or does not receive "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Table 15: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	Support With and Without EoTP	Support With and Without EoTP
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - ✧ Data 0: 0Fhex
  - ✧ Data 1: 0Fhex
- Error Correction Code (ECC)
  - ✧ ECC: 01hex

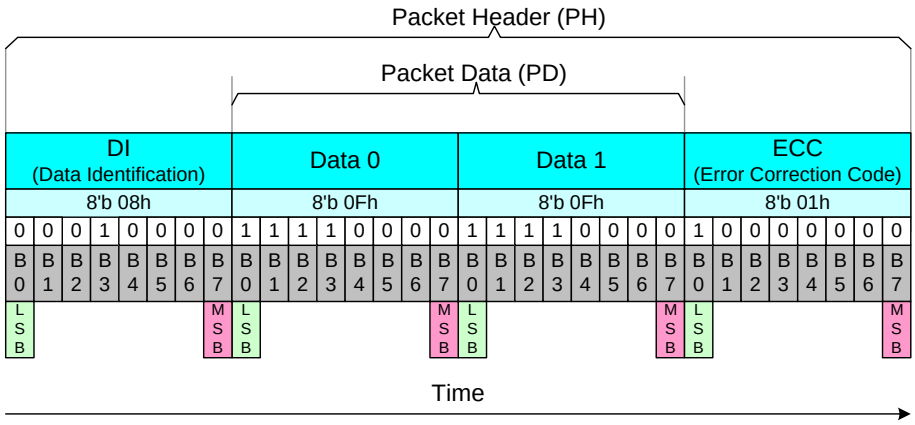


Figure 58: End of Transmission Packet (EoTP)

Some examples of the "End of Transmission Packet" (EoTP) are illustrated for reference purposes below.

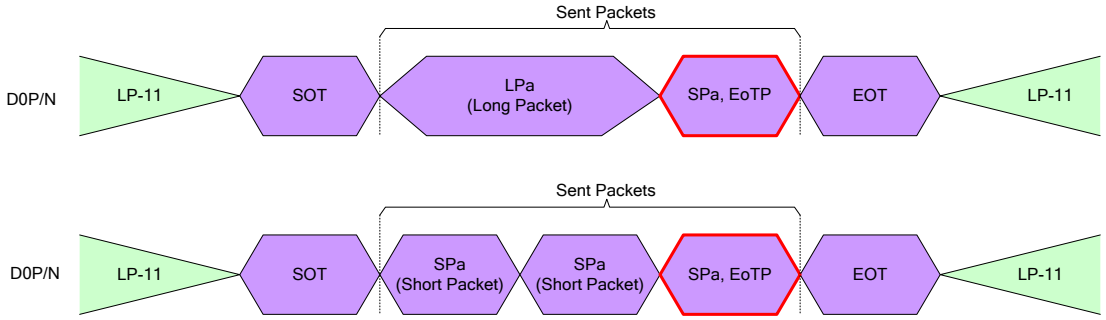


Figure 59: End of Transmission Packet (EoTP)-Examples

4.4.3.2.2. Packet from the Display Module to the MCU

4.4.3.2.2.1. Used Packet types

The display module always uses Short Packets (SPa) or Longs Packet (LPa) when returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See the section "4.4.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)") or an Acknowledge with Error Report (See the section "4.4.3.2.2.2 Acknowledge with Error Report (AwER)").

The used packet type is defined on Data Type (DT). See the section "4.4.3.1.3.1.2 Data Type (DT)". If the maximum size of the Packet Data (PD) could be sent in one packet, the display module should not send returned bytes in several packets. Both cases are illustrated for reference purposes below.

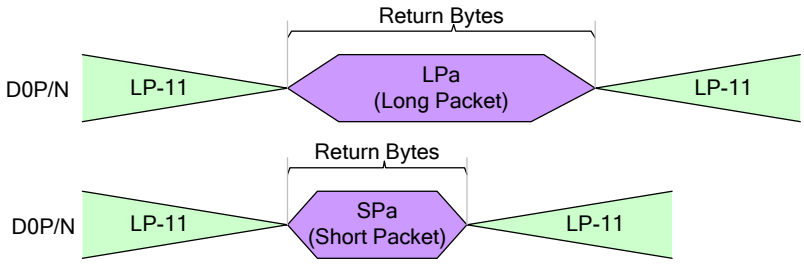


Figure 60: Return Bytes in Single Packet

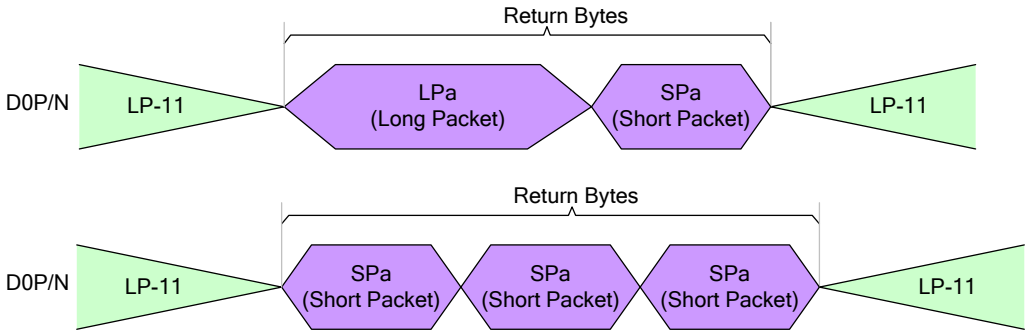


Figure 61: Return Bytes in Several Packets – Not Allowed

EXCEPTION:

The display module will return 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module receives a read command (See section "4.4.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)"), which is detected and corrected a single bit error by the EEC (See bit 8 in Table 16).

These returned packets are illustrated for reference purposes below.

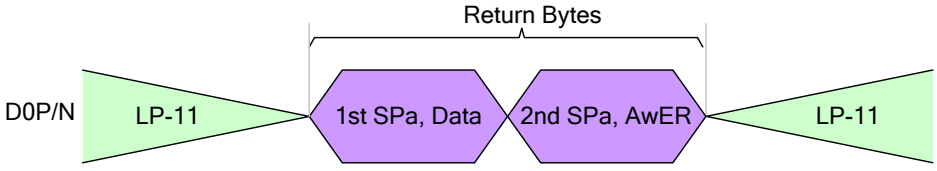


Figure 62: Exception when Returned Bytes in Several Packets

AwER = Acknowledge with Error Report

4.4.3.2.2.2. Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Table 16: Error Report (AwER) Bit Definitions

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0010b
- Packet Data (PD)
  - ✧ Bit 8: ECC Error, single-bit (detected and corrected)
  - ✧ AwER: 0100h
- Error Correction Code (ECC)

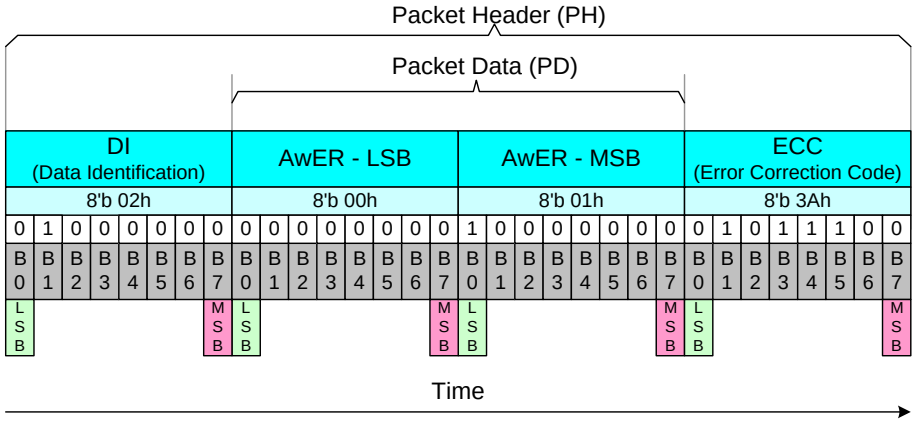


Figure 63: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

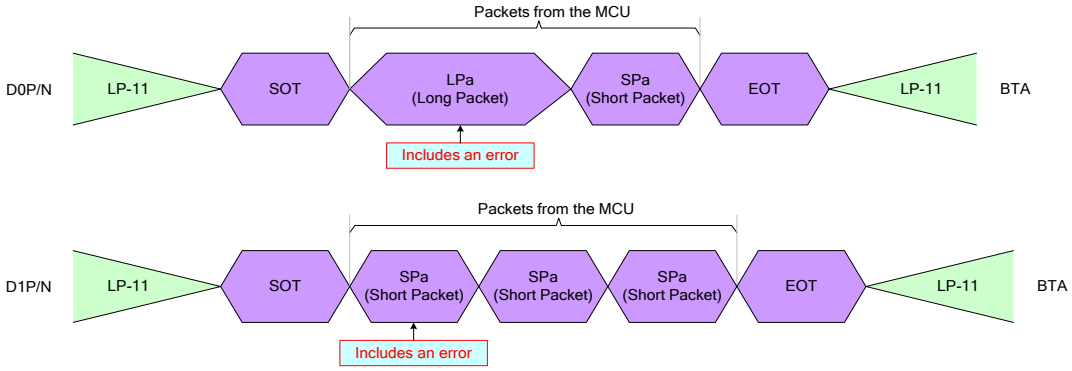


Figure 64: Errors Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1 if a received packet includes an error.

The amount of packets, which include an ***ECC*** *or* ***CRC*** error, is calculated in the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and set the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes below.

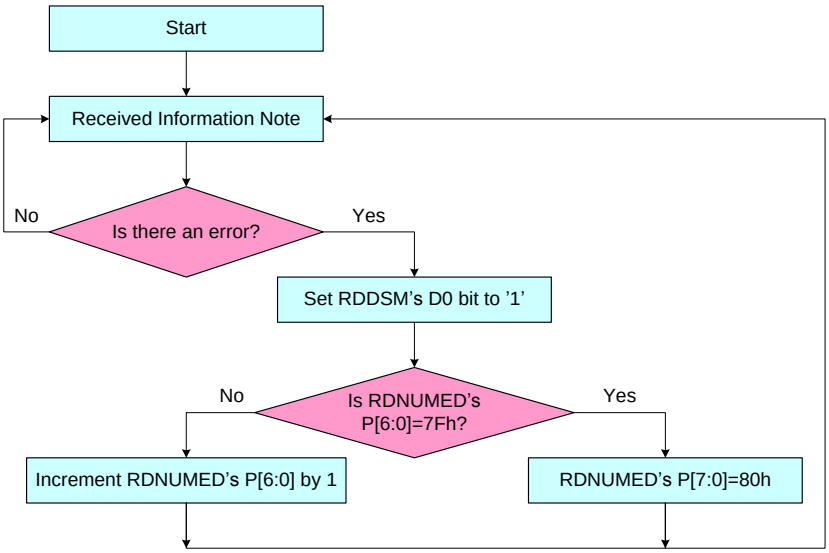


Figure 65: Flow Chart for Errors on DSI

Notes:

1. *This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.*
2. *CRC or ECC error*

4.4.3.2.2.3. DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
  - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: 89hex
  - ✧ Data 1: 23hex
  - ✧ Data 2: 12hex
  - ✧ Data 3: A2hex
  - ✧ Data 4: E2hex
- Packet Footer (PF)

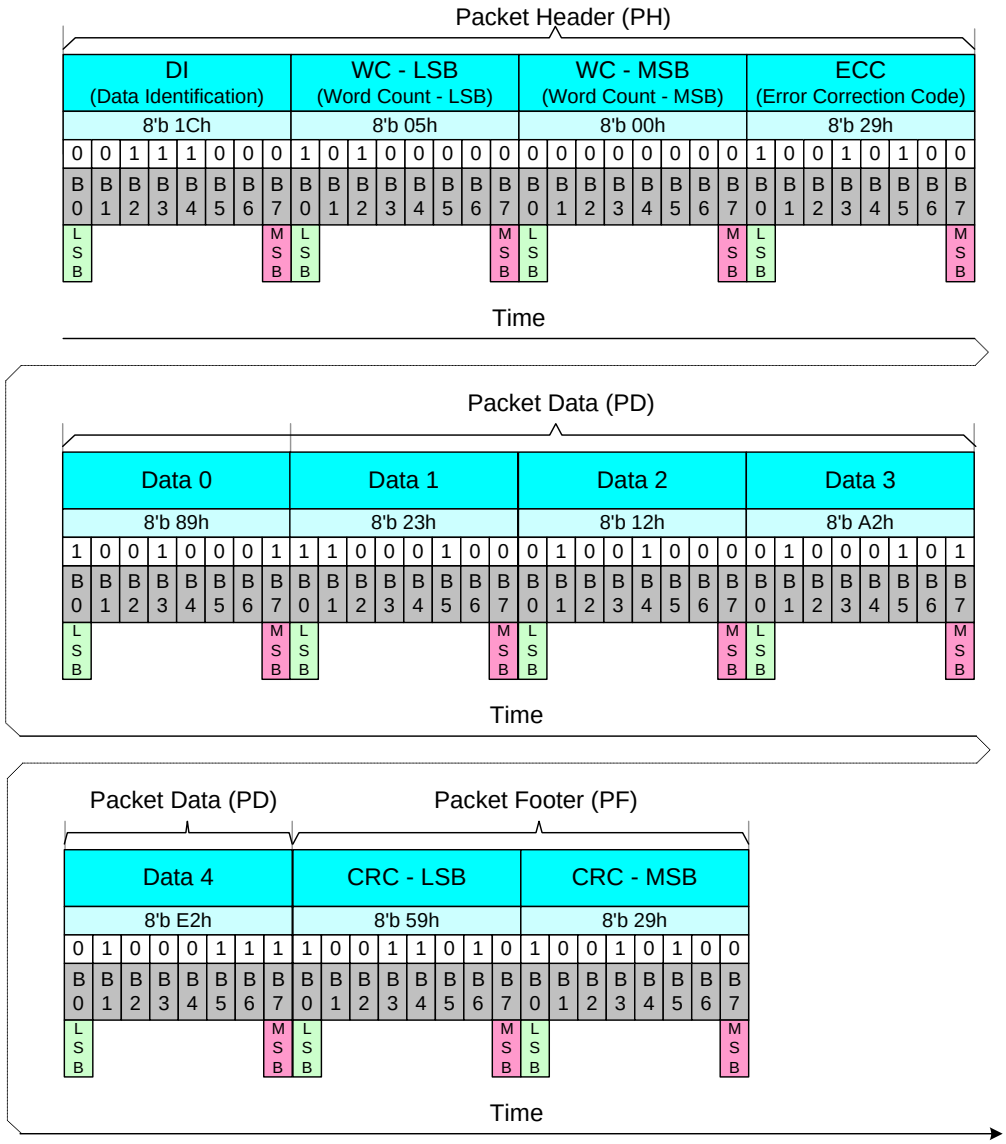


Figure 66: DCS Read Long Response (DCSRR-L) - Example

4.4.3.2.2.4. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - ✧ Data 0: 45hex
  - ✧ Data 1: 00hex (Always)
- Error Correction Code (ECC)

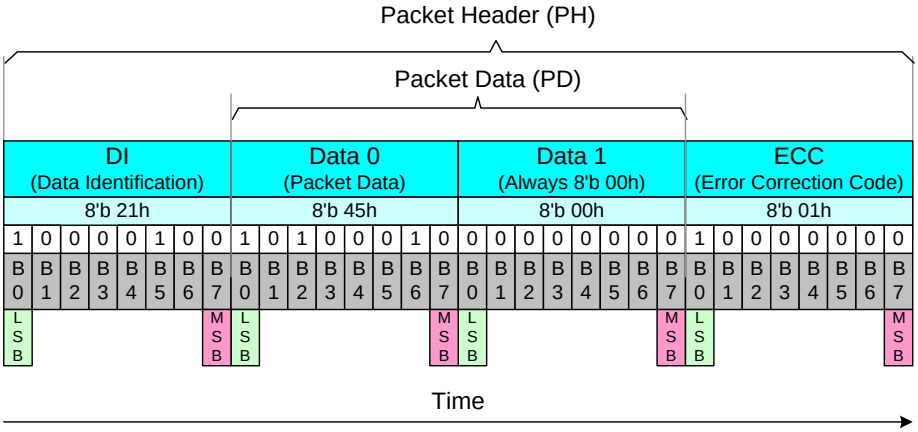


Figure 67: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

4.4.3.2.2.5. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - ✧ Data 0: 45hex
  - ✧ Data 1: 32hex
- Error Correction Code (ECC)

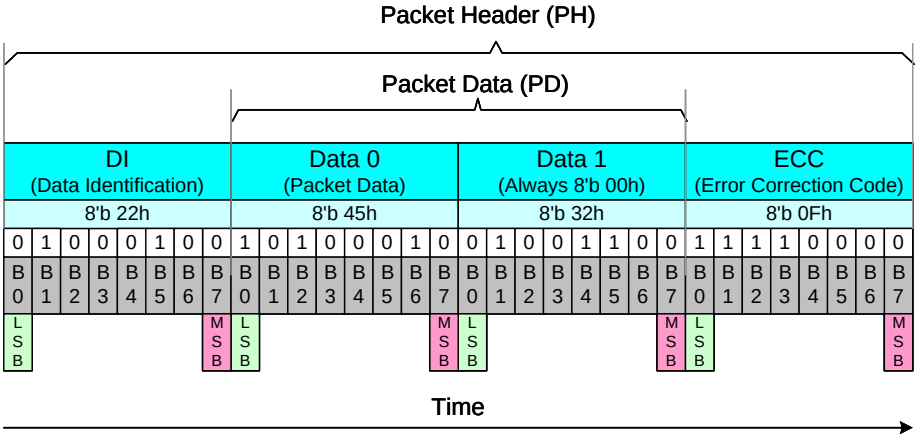


Figure 68: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

4.4.3.3. Communication Sequences

4.4.3.3.1. General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “4.4.2 Interface Level Communication” and “4.4.3 Packet Level Communication”. This communication sequence description is for DSI data lanes (D0P/N), and it is assumed that the needed low level communication is done on DSI Clock lane (CLKP/N) automatically. See the section “4.4.2.2 DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

Table 17: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 18: Packet Level Communication for MCU-sourced Packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	VSS	Short Packet	Sync Event, V Sync Start
	VSE	Short Packet	Sync Event, V Sync End
	HSS	Short Packet	Sync Event, H Sync Start
	HSE	Short Packet	Sync Event, H Sync End
	EoTP	Short Packet	End of Transmission Packet (EoTP) Note1
	CMOFF	Short Packet	Color Mode Off Command
	CMON	Short Packet	Color Mode On Command
	SDNP	Short Packet	Shut Down Peripheral Command
	TONP	Short Packet	Turn On Peripheral Command
	GENWN-S	Short Packet	Generic Short WRITE, no parameters
	GENW1-S	Short Packet	Generic Short WRITE, 1 parameters
	GENW2-S	Short Packet	Generic Short WRITE, 2 parameters
	GENRN-S	Short Packet	Generic Short READ, no parameters
	GENR1-S	Short Packet	Generic Short READ, 1 parameters
	GENR2-S	Short Packet	Generic Short READ, 2 parameters
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data, Note2
	BLK-L	Long Packet	Blanking Packet, no data
	GENW-L	Long Packet	Generic Long Write
	DCSW-L	Long Packet	DCS Write Long
	PKPS16	Long Packet	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
	PKPS18	Long Packet	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	LPKPS18	Long Packet	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	PKPS24	Long Packet	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

Table 19: Packet Level Communication for Peripheral-sourced packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
Display Module (ILI9342E)	Aw ER	Short Packet	Acknowledge with Error Report
	EoTP	Short Packet	End of Transmission Packet
	GENRR1-S	Short Packet	Generic Short READ Response, 1 byte returned
	GENRR2-S	Short Packet	Generic Short READ Response, 2 byte returned
	GENRR-L	Long Packet	Generic Long READ Response
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response, 1 byte returned
	DCSRR2-S	Short Packet	DCS Read Short Response, 2 byte returned

4.4.3.3.2. Sequences

4.4.3.3.2.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined in the section "4.4.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences on how this packet is used are described in following tables.

Table 20: DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 21: DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 22: DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	Aw ER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.4.3.3.2.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined in the section "4.4.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences on how this packet is used are described in following tables.

Table 23: DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 24: DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 25: DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.4.3.3.2.3. DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined in the section "4.4.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)" and example sequences on how this packet is used are described in following tables.

Table 26: DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 27: DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 28: DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.4.3.3.2.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined in the section "4.4.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences on how this packet is used are described in following tables.

Table 29: DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

Table 30: DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

4.4.3.3.2.5. Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined in the section "4.4.3.2.1.6 Null Packet, No Data (NP-L)", and an example sequence on how this packet is used is described in the following table.

Table 31: Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.4.3.3.2.6. End of Transmission Packet

A Short Packet (SPa) of "End of Transmission (EoTP)" is defined in the section "4.4.3.2.1.7 End of Transmission Packet (EoTP)", and an example sequence on how this packet is used is described in the following table.

Table 32: End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MCU		Information Direction	Display Module (ILI9342E)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.5. Display Data Format (DSI transmission data format)

4.5.1. 16-bit per Pixel, Long packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, ILI9806P has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifice.

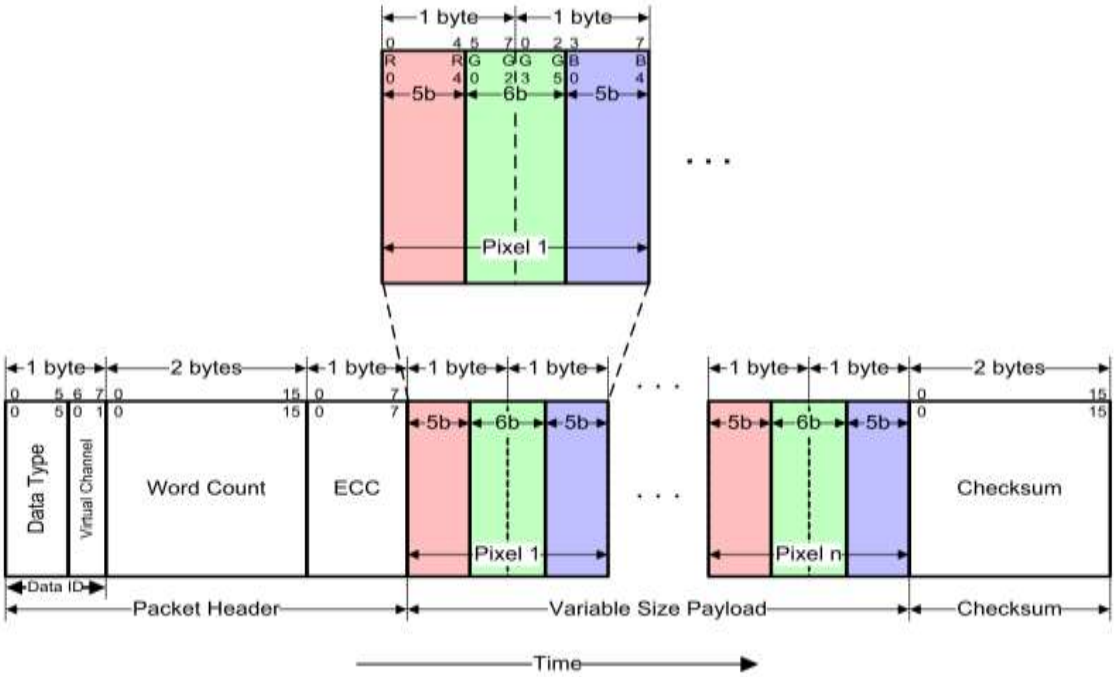


Figure 69 16-bit per Pixel, Data Type 00 1110 (0Eh)

4.5.2. 18-bit per Pixel, Long packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

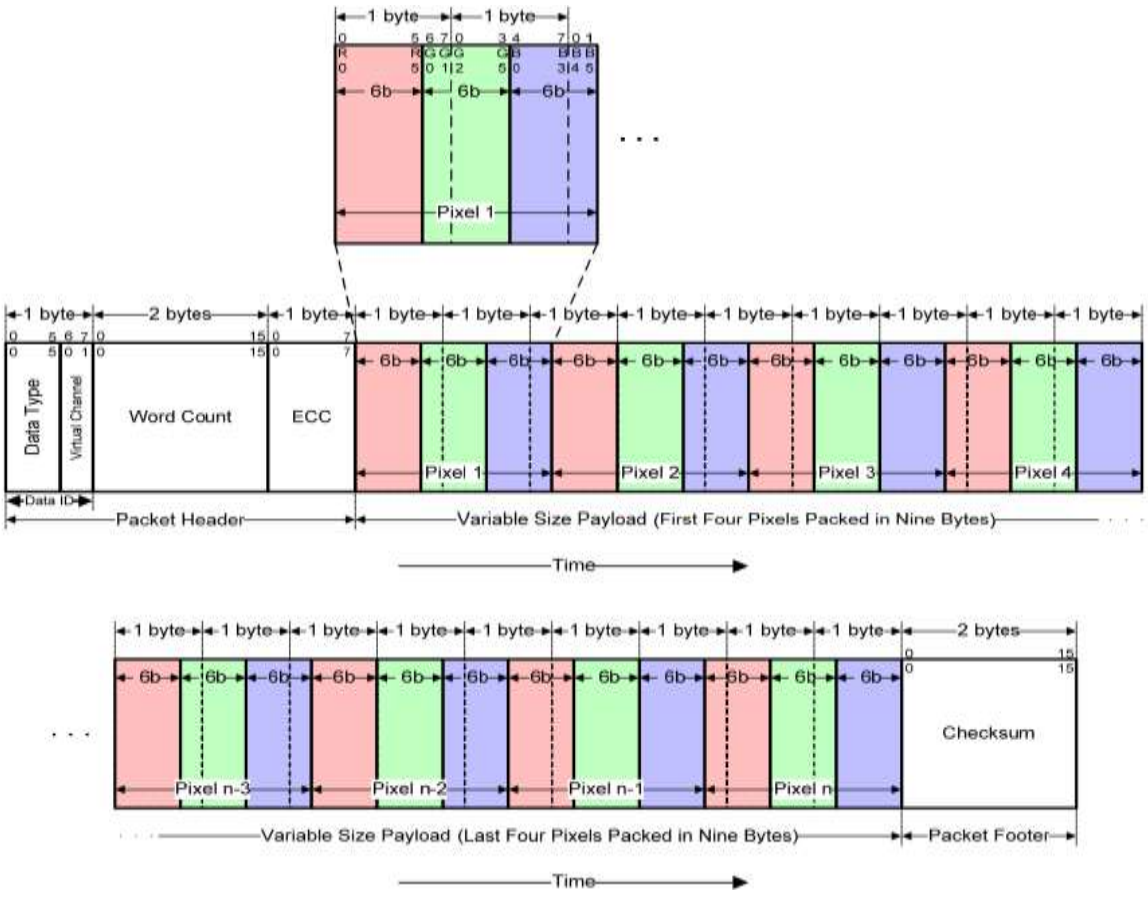


Figure 70 18-bit per Pixel, Data Type = 01 1110 (1Eh)

4.5.3. 18-bit per Pixel, Long packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

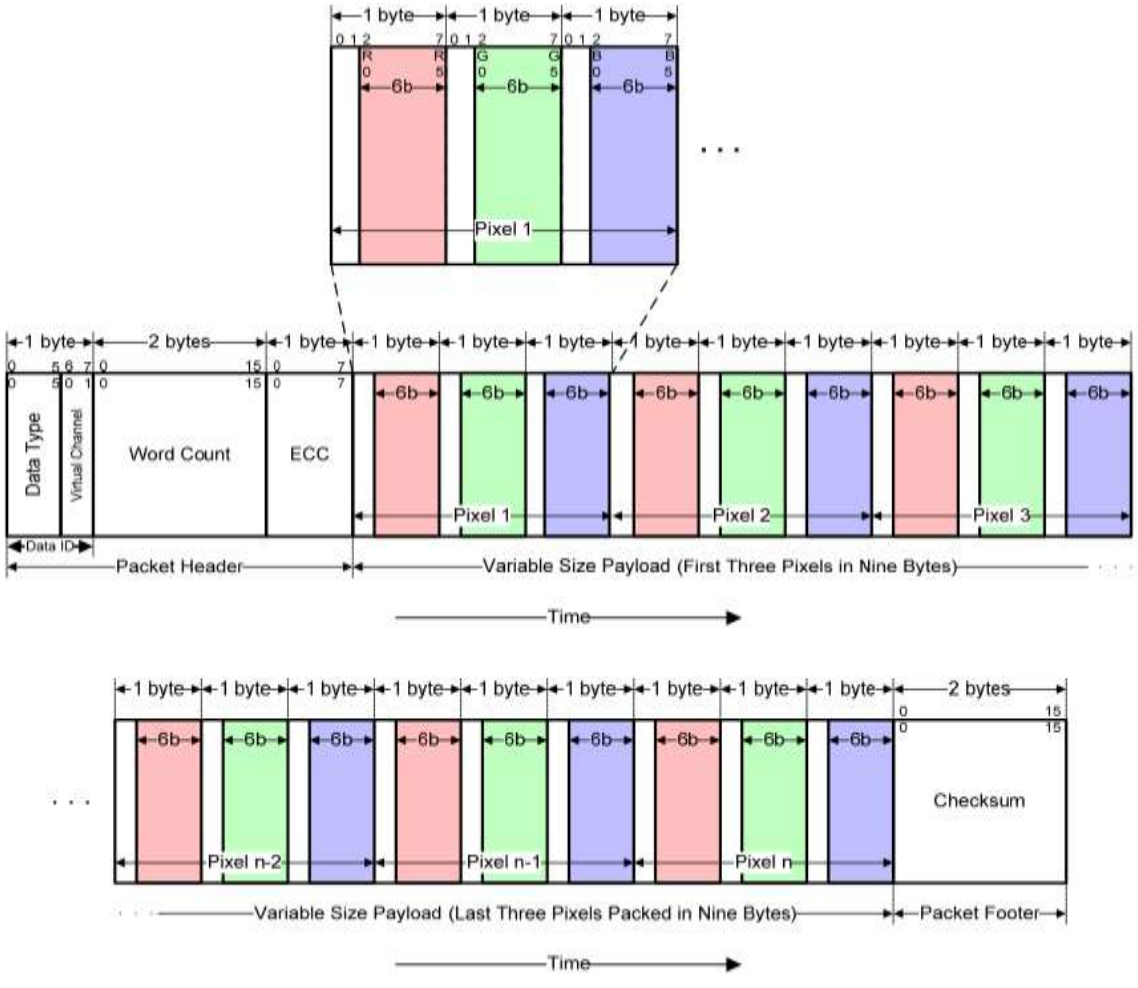


Figure 71 18-bit per Pixel, Data Type = 10 1110 (2Eh)

4.5.4. 24-bit per Pixel, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

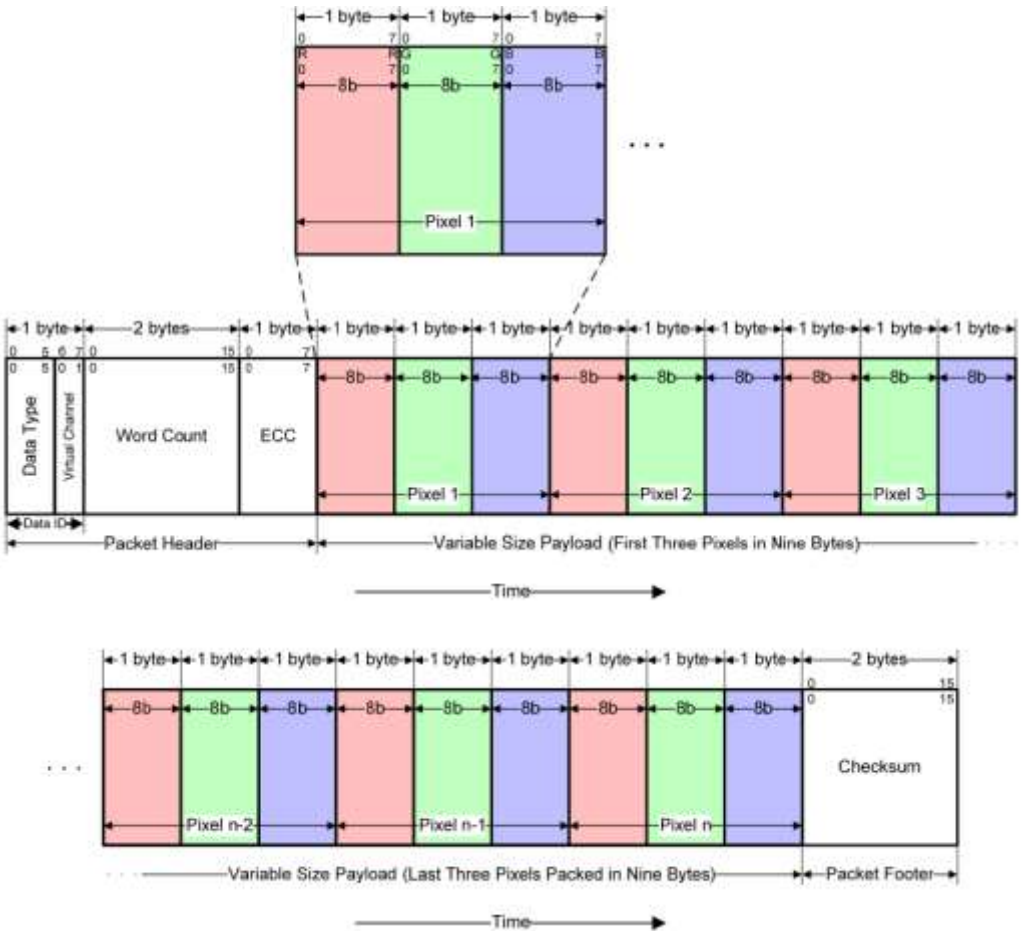
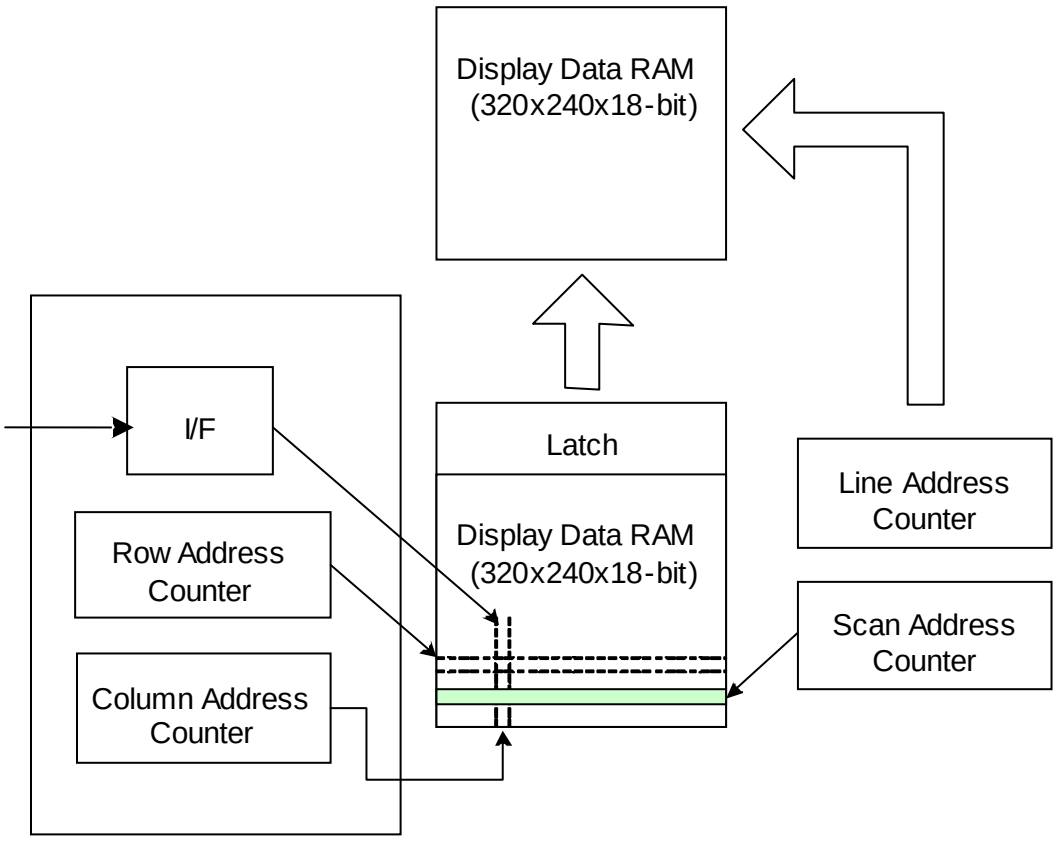


Figure 72 24-bit per Pixel, Data Type = 11 1110 (3Eh)

4.6. Display Data RAM (DDRAM)

ILI9342E has an integrated 320x240x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 320xRGBx240 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

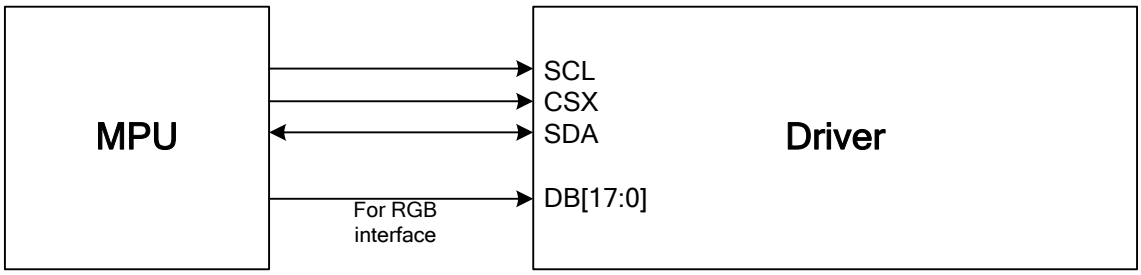


4.7. Display Data Format

ILI9342E supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

4.7.1. 3-line Serial Interface

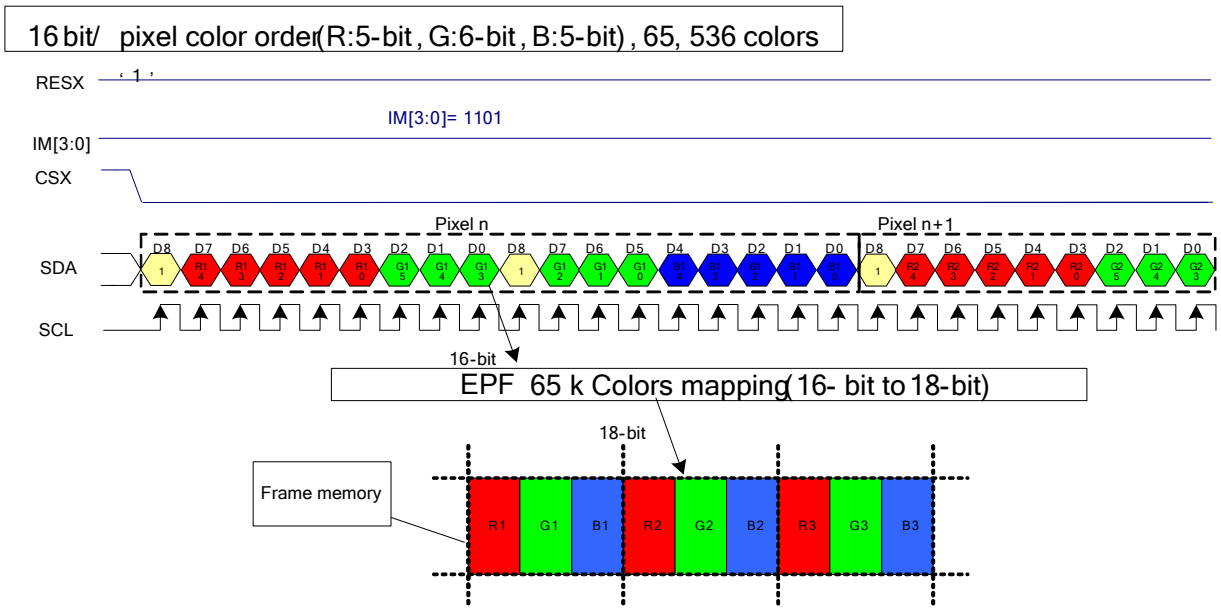
The 3-line/9-bit serial bus interface of ILI9342E can be used by setting external pin as IM [3:0] to "1101" for serial interface. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.



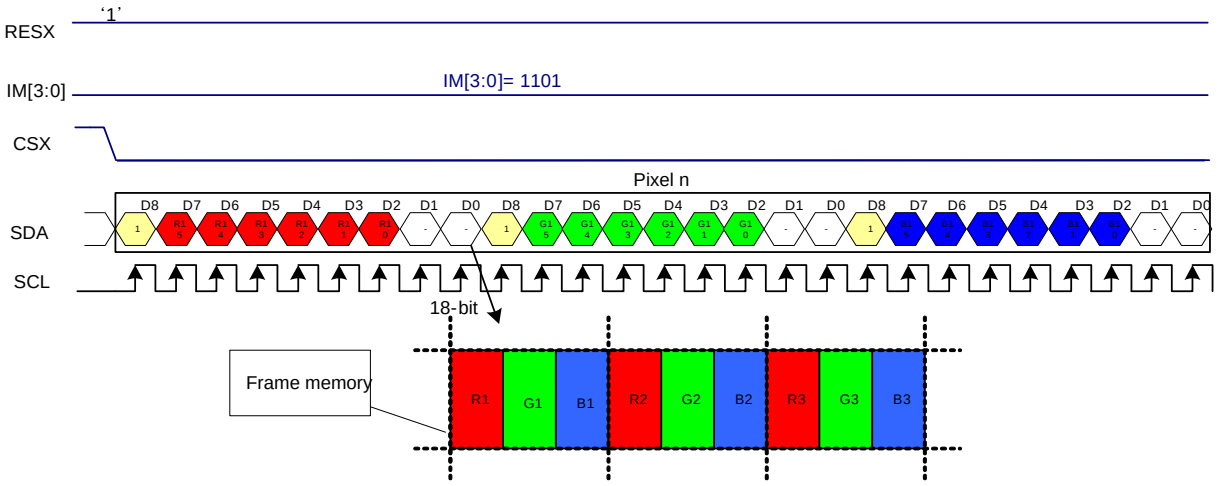
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/ pixel color order (R:6-bit, G:6-bit, B:6-bit), 262, 144 colors



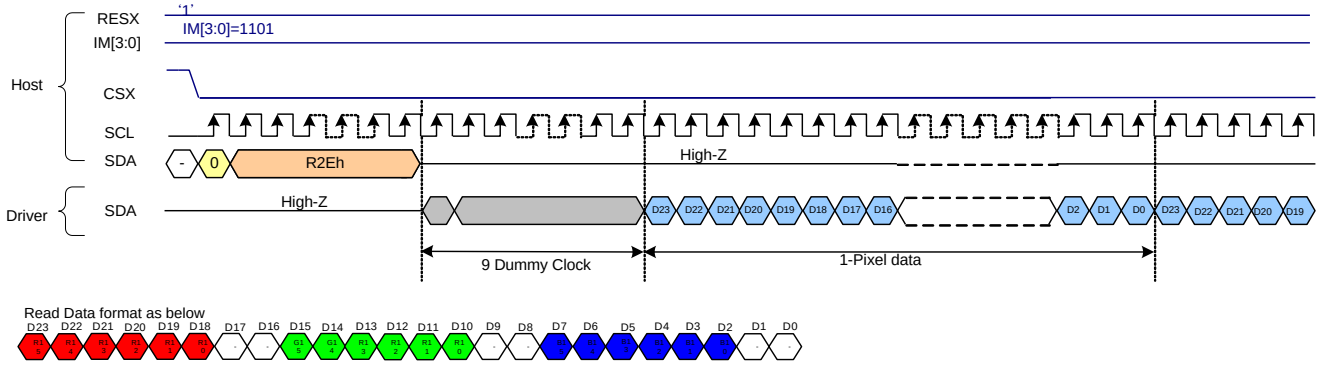
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

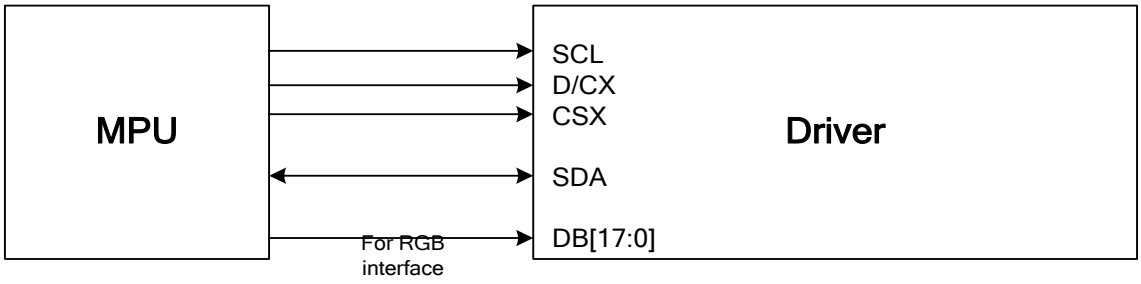
Read data through 3-line SPI mode



Note 1: '-'= Don't care –Can be set "0" or "1".

4.7.2. 4-line Serial Interface

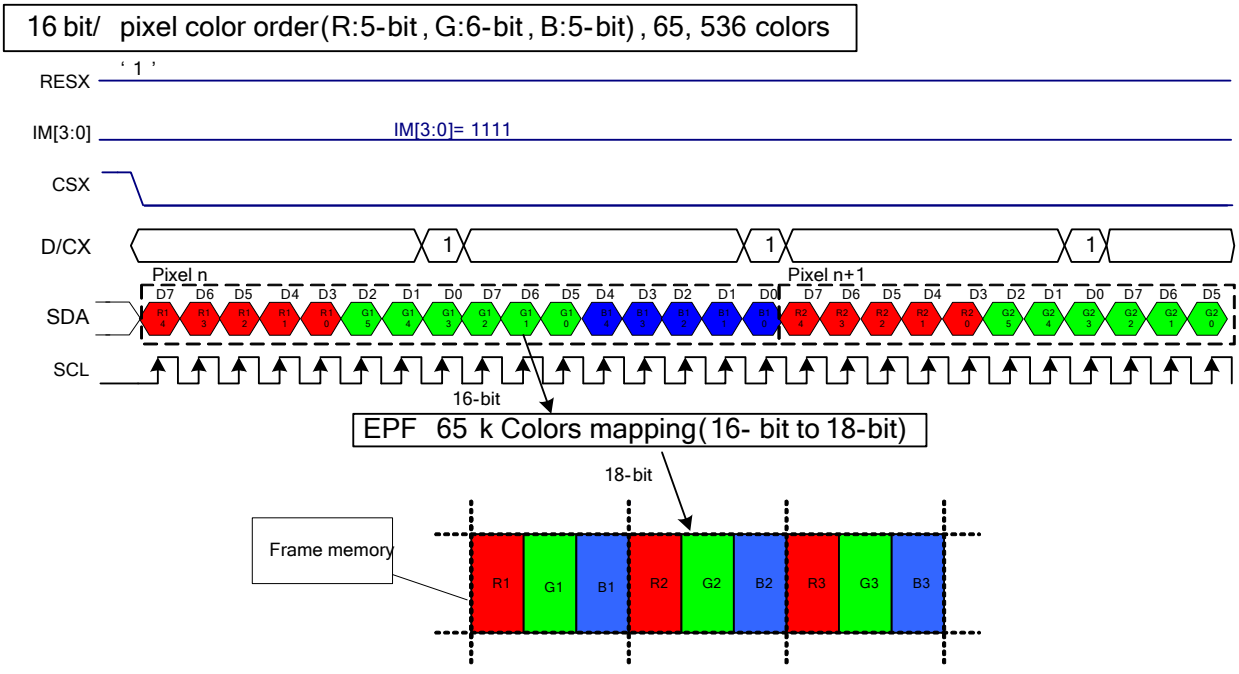
The 4-line/8-bit serial bus interface of ILI9342E can be used by setting external pin as IM [3:0] to "1111" for serial interface. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.



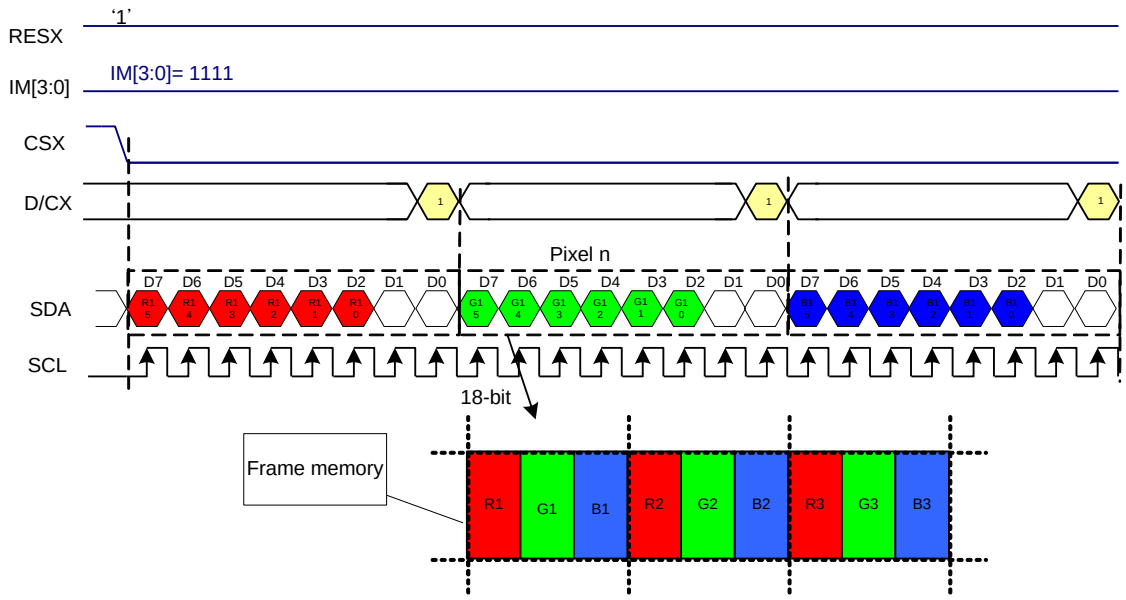
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



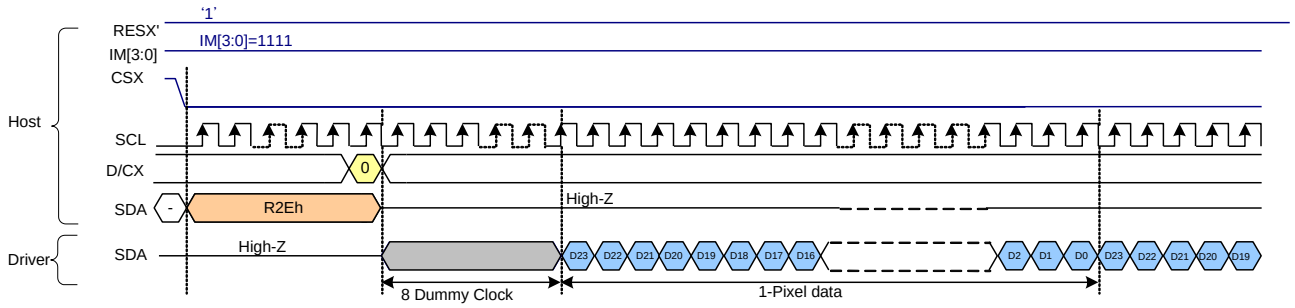
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

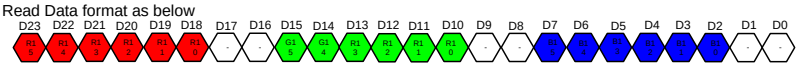
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Read data through 4-line SPI mode



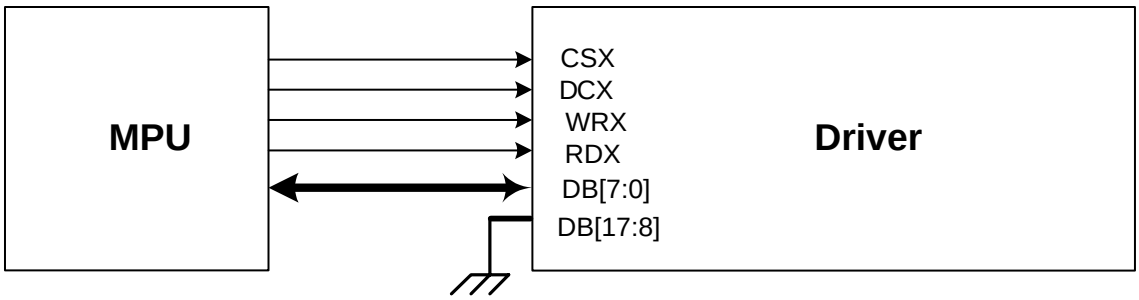
Read Data format as below



Note 1: '-'= Don't care – Can be set "0" or "1".

4.7.3. 8-bit Parallel MCU Interface

The 8080-Ⅰ system 8-bit parallel bus interface of ILI9342E can be used by setting external pin as IM [3:0] to "0100".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

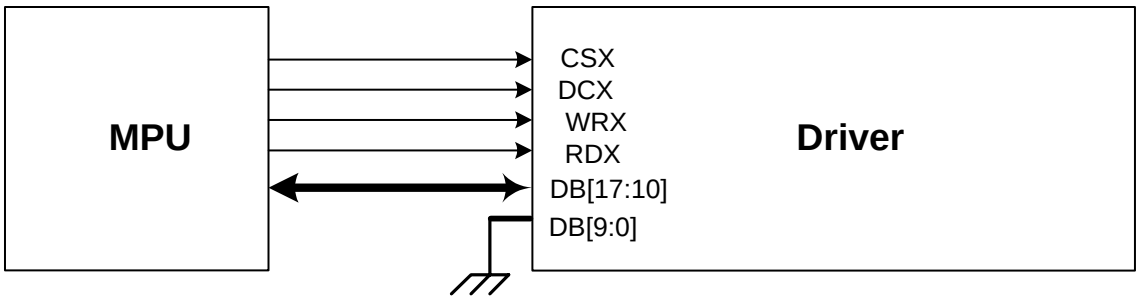
Count	0	1	2	3	4	…	637	638	639	640
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	958	959	960
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-Ⅱ system 8-bit parallel bus interface of ILI9342E can be used by settings as IM [3:0] ="0000". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	637	638	639	640
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

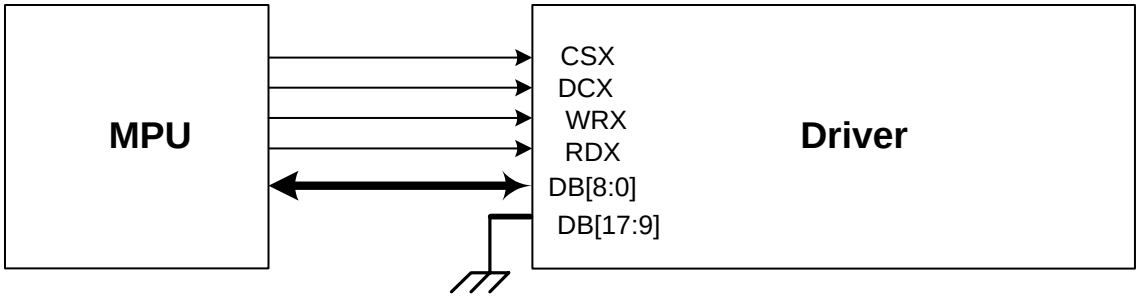
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	958	959	960
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

4.7.4. 9-bit Parallel MCU Interface

The 8080-Ⅰ system 9-bit parallel bus interface of ILI9342E can be selected by setting hardware pin IM [3:0] to "0101". The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	637	638	639	640
D/CX	0	1	1	1	1	…	1	1	1	1
D8										
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

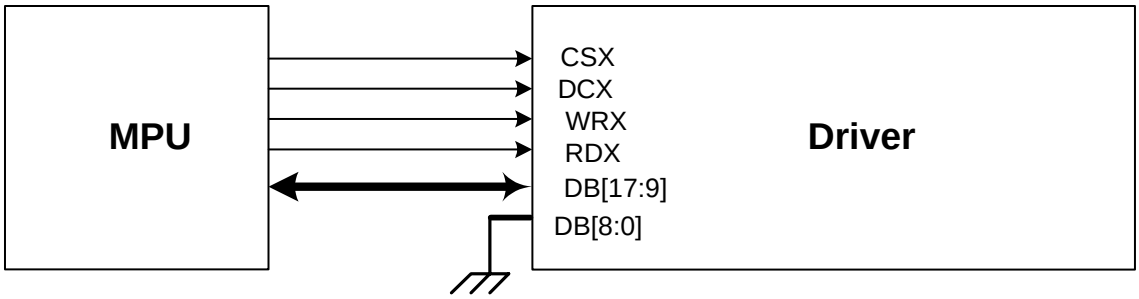
MDT[1:0]="00"

Count	0	1	2	3	4	…	637	638	639	640
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

MDT[1:0]=”01”

Count	0	1	2	3	…	958	959	960
D/CX	0	1	1	1	…	1	1	1
D8								
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-Ⅱ system 9-bit parallel bus interface of ILI9342E can be selected by setting hardware pin IM [3:0] to “0001”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	4	…	637	638	639	640
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7									
D16	C6	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

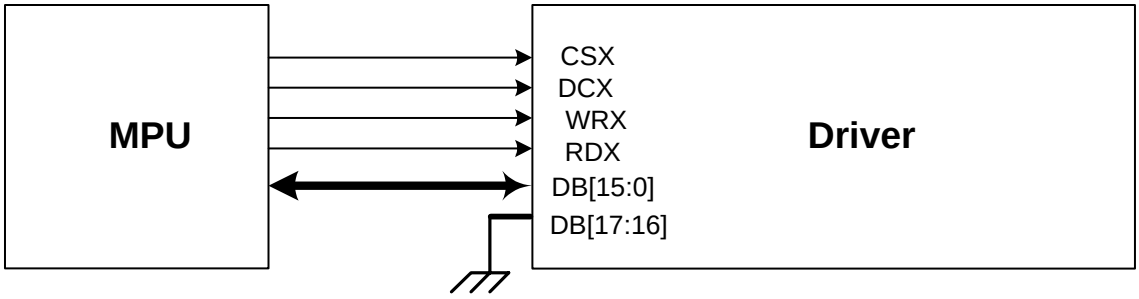
Count	0	1	2	3	4	…	637	638	639	640
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

MDT[1:0]="01"

Count	0	1	2	3	…	958	959	960
D/CX	0	1	1	1	…	1	1	1
D17	C7							
D16	C6	0R5	0G5	0B5	…	239R5	239G5	239B5
D15	C5	0R4	0G4	0B4	…	239R4	239G4	239B4
D14	C4	0R3	0G3	0B3	…	239R3	239G3	239B3
D13	C3	0R2	0G2	0B2	…	239R2	239G2	239B2
D12	C2	0R1	0G1	0B1	…	239R1	239G1	239B1
D11	C1	0R0	0G0	0B0	…	239R0	239G0	239B0
D10	C0				…			
D9					…			

4.7.5. 16-bit Parallel MCU Interface

The 8080-Ⅰ system 16-bit parallel bus interface of ILI9342E can be selected by setting hardware pin IM[3:0] to "0110".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	318	319	320
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

MDT[1:0]=”00”

Count	0	1	2	3	…	478	479	480
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9					…			
D8					…			
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1				…			
D0	C0				…			

MDT[1:0]=”01”

Count	0	1	2	3		…	637	638	639	640
D/CX	0	1	1	1		…		1	1	1
D15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	238G5		239G5	
D6	C6	0G4		1G4		…	238G4		239G4	
D5	C5	0G3		1G3		…	238G3		239G3	
D4	C4	0G2		1G2		…	238G2		239G2	
D3	C3	0G1		1G1		…	238G1		239G1	
D2	C2	0G0		1G0		…	238G0		239G0	
D1	C1					…				
D0	C0					…				

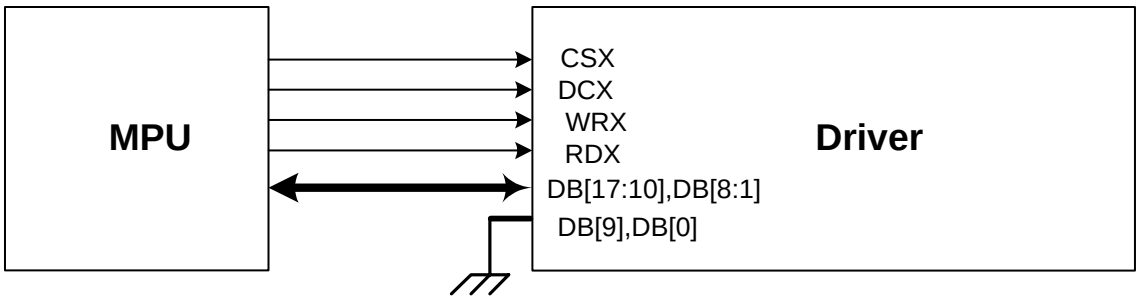
MDT[1:0]=”10”

Count	0	1	2	3		…	637	638	639	640
D/CX	0	1	1	1		…		1	1	1
D15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D13		0R3		1R3		…	238R3		239R3	
D12		0R2		1R2		…	238R2		239R2	
D11		0R1		1R1		…	238R1		239R1	
D10		0R0		1R0		…	238R0		239R0	
D9		0G5		1G5		…	238G5		239G5	
D8		0G4		1G4		…	238G4		239G4	
D7	C7	0G3		1G3		…	238G3		239G3	
D6	C6	0G2		1G2		…	238G2		239G2	
D5	C5	0G1		1G1		…	238G1		239G1	
D4	C4	0G0		1G0		…	238G0		239G0	
D3	C3	0B5		1B5		…	238B5		239B5	
D2	C2	0B4		1B4		…	238B4		239B4	
D1	C1	0B3		1B3		…	238B3		239B3	
D0	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=”11”

Count	0	1	2	3		…	637	638	639	640
D/CX	0	1	1	1		…		1	1	1
D15			0R3		1R3	…		238R3		239R3
D14			0R2		1R2	…		238R2		239R2
D13			0R1		1R1	…		238R1		239R1
D12			0R0		1R0	…		238R0		239R0
D11			0G5		1G5	…		238G5		239G5
D10			0G4		1G4	…		238G4		239G4
D9			0G3		1G3	…		238G3		239G3
D8			0G2		1G2	…		238G2		239G2
D7	C7		0G1		1G1	…		238G1		239G1
D6	C6		0G0		1G0	…		238G0		239G0
D5	C5		0B5		1B5	…		238B5		239B5
D4	C4		0B4		1B4	…		238B4		239B4
D3	C3		0B3		1B3	…		238B3		239B3
D2	C2		0B2		1B2	…		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-Ⅱ system 16-bit parallel bus interface of ILI9342E can be selected by settings IM [3:0] =”0010”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	…	318	319	320
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	237R4	238R4	239R4
D16		0R3	1R3	2R3	…	237R3	238R3	239R3
D15		0R2	1R2	2R2	…	237R2	238R2	239R2
D14		0R1	1R1	2R1	…	237R1	238R1	239R1
D13		0R0	1R0	2R0	…	237R0	238R0	239R0
D12		0G5	1G5	2G5	…	237G5	238G5	239G5
D11		0G4	1G4	2G4	…	237G4	238G4	239G4
D10		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

MDT[1:0]=”00”

Count	0	1	2	3	…	478	479	480
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	238R5	238B5	239G5
D16		0R4	0B4	1G4	…	238R4	238B4	239G4
D15		0R3	0B3	1G3	…	238R3	238B3	239G3
D14		0R2	0B2	1G2	…	238R2	238B2	239G2
D13		0R1	0B1	1G1	…	238R1	238B1	239G1
D12		0R0	0B0	1G0	…	238R0	238B0	239G0
D11					…			
D10					…			
D8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D2	C1				…			
D1	C0				…			

MDT[1:0]=”01”

Count	0	1	2	3		…	637	638	639	640
D/CX	0	1	1	1		…		1	1	1
D17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	238G5		239G5	
D7	C6	0G4		1G4		…	238G4		239G4	
D6	C5	0G3		1G3		…	238G3		239G3	
D5	C4	0G2		1G2		…	238G2		239G2	
D4	C3	0G1		1G1		…	238G1		239G1	
D3	C2	0G0		1G0		…	238G0		239G0	
D2	C1					…				
D1	C0					…				

MDT[1:0]=”10”

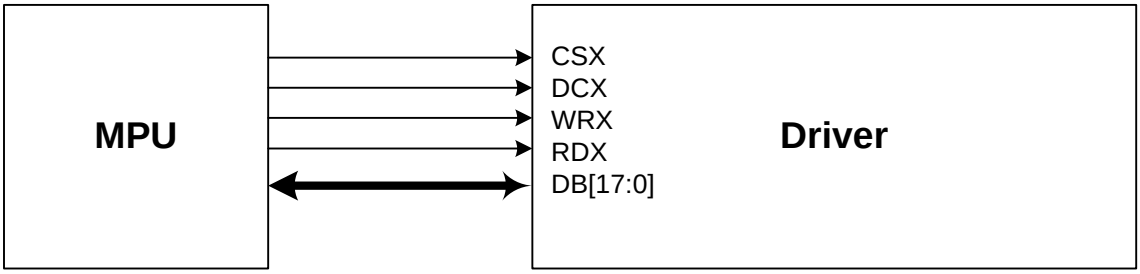
Count	0	1	2	3		…	637	638	639	640
D/CX	0	1	1	1		…		1	1	1
D17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D15		0R3		1R3		…	238R3		239R3	
D14		0R2		1R2		…	238R2		239R2	
D13		0R1		1R1		…	238R1		239R1	
D12		0R0		1R0		…	238R0		239R0	
D11		0G5		1G5		…	238G5		239G5	
D10		0G4		1G4		…	238G4		239G4	
D8	C7	0G3		1G3		…	238G3		239G3	
D7	C6	0G2		1G2		…	238G2		239G2	
D6	C5	0G1		1G1		…	238G1		239G1	
D5	C4	0G0		1G0		…	238G0		239G0	
D4	C3	0B5		1B5		…	238B5		239B5	
D3	C2	0B4		1B4		…	238B4		239B4	
D2	C1	0B3		1B3		…	238B3		239B3	
D1	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=”11”

Count	0	1	2	3		…	637	638	649	640
D/CX	0	1	1	1		…		1	1	1
D17			0R3		1R3	…		238R3		239R3
D16			0R2		1R2	…		238R2		239R2
D15			0R1		1R1	…		238R1		239R1
D14			0R0		1R0	…		238R0		239R0
D13			0G5		1G5	…		238G5		239G5
D12			0G4		1G4	…		238G4		239G4
D11			0G3		1G3	…		238G3		239G3
D10			0G2		1G2	…		238G2		239G2
D8	C7		0G1		1G1	…		238G1		239G1
D7	C6		0G0		1G0	…		238G0		239G0
D6	C5		0B5		1B5	…		238B5		239B5
D5	C4		0B4		1B4	…		238B4		239B4
D4	C3		0B3		1B3	…		238B3		239B3
D3	C2		0B2		1B2	…		238B2		239B2
D2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

4.7.6. 18-bit Parallel MCU Interface

The 8080-Ⅰ system 18-bit parallel bus interface of ILI9342E can be selected by setting hardware pin IM[3:0] to "0111".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

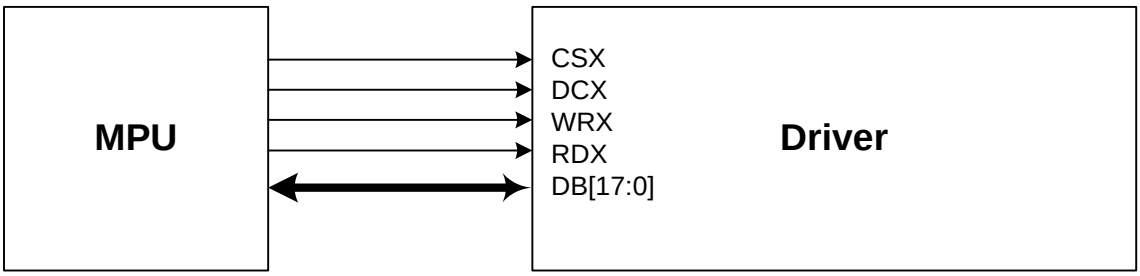
Count	0	1	2	3	…	318	319	320
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	318	319	320
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-Ⅱ system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="0011". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	318	319	320
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

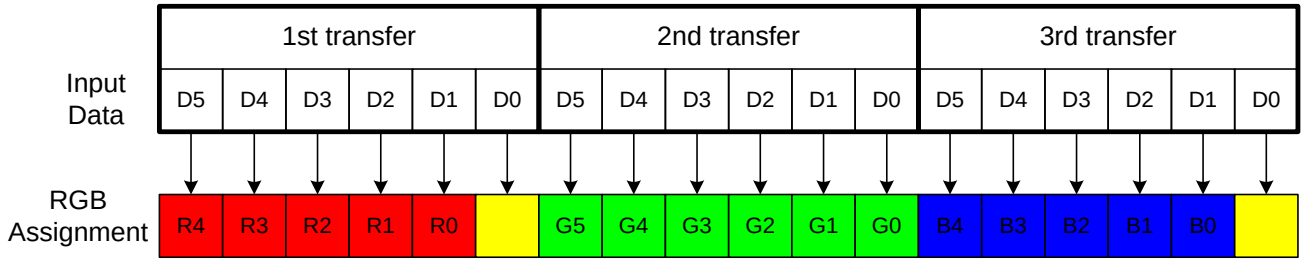
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	318	319	320
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

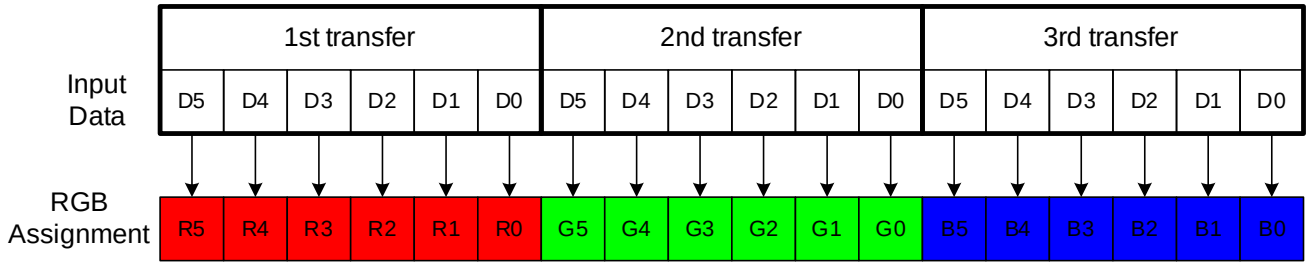
4.7.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



262K color: 18-bit/pixel (RGB 6-6-6 bits input)



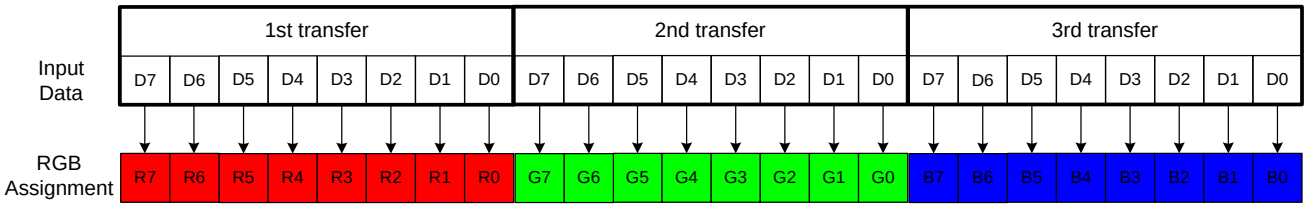
ILI9342E has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

4.7.8. 8-bit Parallel RGB Interface

The 8-bit RGB interface is selected by setting the DPI [2:0] bit to "111". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 8-bit RGB data bus (D [7:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [7:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

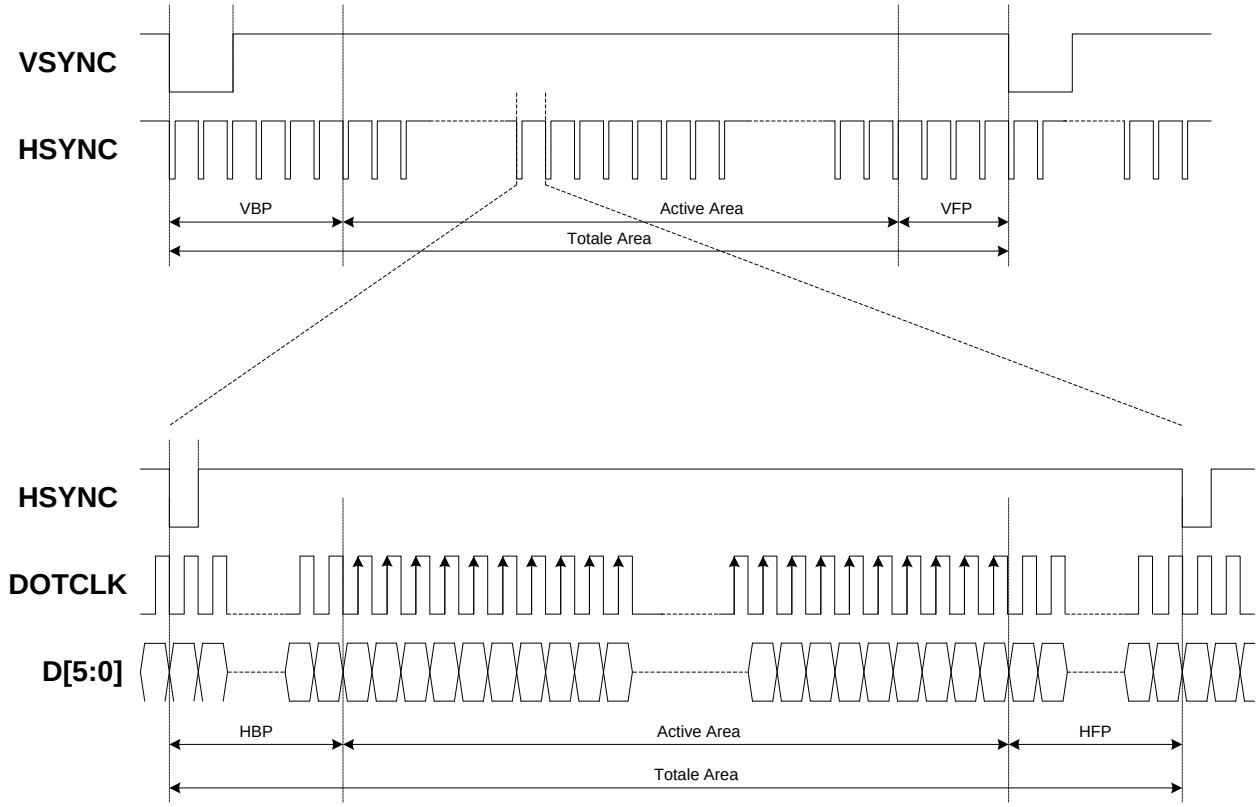
16.77M color: 24-bit/pixel (RGB 8-8-8 bits input)



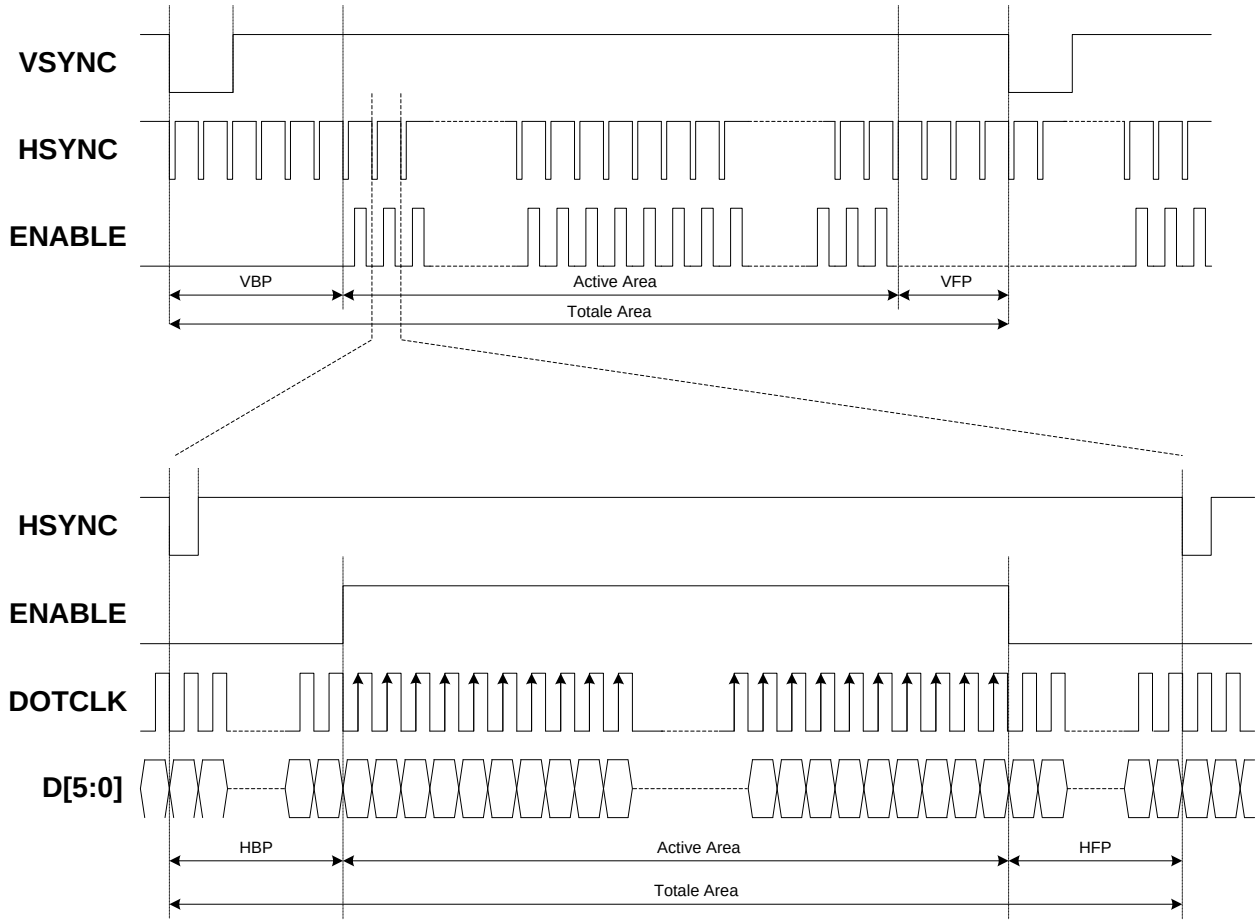
ILI9342E has data transfer counters to count the first, second, third data transfer in 8-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode, RCM[1:0]="11"

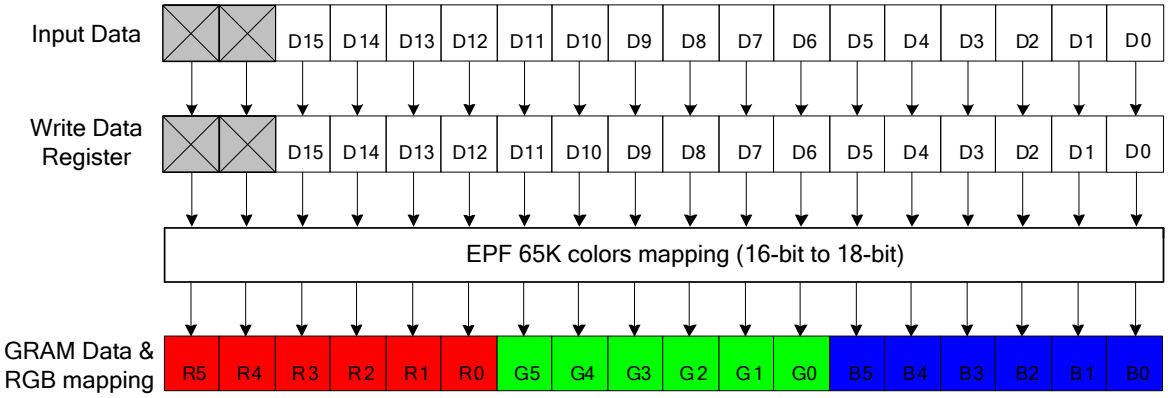


DE Mode, RCM[1:0]="10"



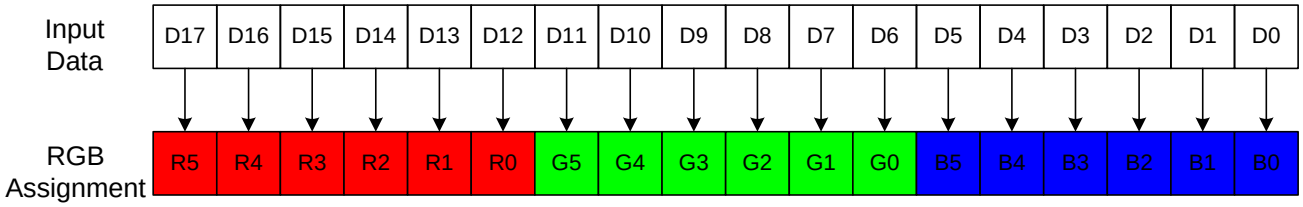
4.7.9. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [15:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via (D [15:0]) according to the VFP/VBP and HFP/HBP settings. The unused D17 and D16 pins must be connected to DGND for ensure normally operation. Registers can be set by the SPI system interface.



4.7.10. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



5. Command

5.1. Command List

Level 1 Command		W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)
Address	Parameter											
00h	-	W	No Operation	No Argument								-
01h	-	W	Software Reset	No Argument								-
04h	1st	R	Read Display Identification Information	X	X	X	X	X	X	X	X	XX
	2nd	R		ID1 [7:0]								E3h
	3rd	R		ID2 [7:0]								00h
	4th	R		ID3 [7:0]								00h
05h	1st	R	Read Number of the Errors on DSI	X	X	X	X	X	X	X	X	XX
	2nd	R		mipi_err_cnt[7:0]								00h
09h	1st	R	Read Display Status	X	X	X	X	X	X	X	X	XX
	2nd	R		D31	D30	D29	D28	D27	D26	D25	0	00h
	3rd	R		0	D22	D21	D20	D19	D18	D16	D16	61h
	4th	R		D15	D14	D13	D12	D11	D10	D9	D8	00h
	5th	R		D7	D6	D5	0	0	0	0	0	00h
0Ah	1st	R	Read Display Power Mode	X	X	X	X	X	X	X	X	XX
	2nd	R		D7	D6	D5	D4	D3	D2	0	0	08h
0Bh	1st	R	Read Display MADCTL	X	X	X	X	X	X	X	X	XX
	2nd	R		D7	D6	D5	D4	D3	D2	0	0	00h
0Ch	1st	R	Read Display Pixel Format	X	X	X	X	X	X	X	X	XX
	2nd	R		0	DPI[2:0]			0	DBI[2:0]			06h
0Dh	1st	R	Read Display Image Mode	X	X	X	X	X	X	X	X	XX
	2nd	R		D7	0	D5	0	0	D2	D1	D0	00h
0Eh	1st	R	Read Display Signal Mode	X	X	X	X	X	X	X	X	XX
	2nd	R		D7	D6	0	0	0	0	0	D0	00h
0Fh	1st	R	Read Display Self-Diagnostic Result	X	X	X	X	X	X	X	X	XX
	2nd	R		D7	D6	0	0	0	0	0	0	00h
10h	-	W	Sleep In	No Argument								-
11h	-	W	Sleep Out	No Argument								-
12h	-	W	Partial Mode On	No Argument								-
13h	-	W	Normal Display Mode On	No Argument								-
20h	-	W	Display Inversion Off	No Argument								-
21h	-	W	Display Inversion On	No Argument								-
28h	-	W	Display Off	No Argument								-
29h	-	W	Display ON	No Argument								-
2Ah	1st	W	Column Address Set	0	0	0	0	0	0	0	SC[8]	00h
	2nd	W		SC[7:0]								00h
	3rd	W		0	0	0	0	0	0	0	EC[8]	01h
	4th	W		EC[7:0]								3Fh
2Bh	1st	W	Page Address Set	0	0	0	0	0	0	0	SP[8]	00h
	2nd	W		SP[7:0]								00h
	3rd	W		0	0	0	0	0	0	0	EP[8]	00h
	4th	W		EP[7:0]								EFh
2Ch	1st	W	Memory Write	D1 [17:0]								-
	:	W		:								-
	Nth	W		Dn [17:0]								-
2Eh	1st	R	Memory Read	X	X	X	X	X	X	X	X	XX

	2nd	R		D1 [17:0]									-
	:	R		:									-
	(N+1)th	R		Dn [17:0]									-
30h	1st	W	Partial Area	0	0	0	0	0	0	0	SR[8]		00h
	2nd	W		SR [7:0]									00h
	3rd	W		0	0	0	0	0	0	0	ER[8]		00h
	4th	W		ER [7:0]									EFh
33h	1st	W	Vertical Scrolling Definition	0	0	0	0	0	0	0	TFA[8]		00h
	2nd	W		TFA [7:0]									00h
	3rd	W		0	0	0	0	0	0	0	VSA[8]		00h
	4th	W		VSA [7:0]									F0h
	5th	W		0	0	0	0	0	0	0	BFA[8]		00h
	6th	W		BFA [7:0]									00h
34h	-	W	Tearing Effect Line OFF	No Argument									-
35h	1st	W	Tearing Effect Line ON	0	0	0	0	0	0	0	M		00h
36h	1st	W	Memory Access Control	MY	MX	MV	ML	BGR	MH	0	0		00h
37h	1st	W	Vertical Scrolling Start Address	0	0	0	0	0	0	0	VSP[8]		00h
	2nd	W		VSP [7:0]									00h
38h	-	W	Idle Mode Off	No Argument									-
39h	-	W	Idle Mode On	No Argument									-
3Ah	1st	W	Pixel Format Set	0	DPI [2:0]			0	DBI [2:0]				66h
3Ch	1st	W	Memory Write Continue	D1 [17:0]									-
	:	W		:									-
	Nth	W		Dn [17:0]									-
3Eh	1st	R	Memory Read Continue	X	X	X	X	X	X	X	X		XX
	2nd	R		D1 [17:0]									-
	:	R		:									-
	(N+1)th	R		Dn [17:0]									-
44h	1st	W	Set tear scan line	0	0	0	0	0	0	0	STS[8]		00h
	2nd	W		STS[7:0]									00h
45h	1st	R	Get tear scan line	X	X	X	X	X	X	X	X		XX
	2nd	R		0	0	0	0	0	0	0	GTS[8]		00h
	3rd	R		GTS[7:0]									00h
51h	1st	W	Write Display Brightness	DBV [7:0]									00h
52h	1st	R	Read Display Brightness	X	X	X	X	X	X	X	X		XX
	2nd	R		DBV[7:0]									00h
53h	1st	W	Write CTRL Display	0	0	BCTRL	0	DD	BL	0	0		00h
54h	1st	R	Read CTRL Display	X	X	X	X	X	X	X	X		XX
	2nd	R		0	0	BCTRL	0	DD	BL	0	0		00h
55h	1st	W	Write CAB Control	0	0	0	0	0	0	C[1]	C[0]		00h
56h	1st	R	Read CAB Control	X	X	X	X	X	X	X	X		XX
	2nd	R		0	0	0	0	0	0	C[1]	C[0]		00h
5Eh	1st	W	Write CABC Minimum Brightness	CMB[7:0]									00h
5Fh	1st	R	Read CABC Minimum Brightness	X	X	X	X	X	X	X	X		XX
	2nd	R		CMB[7:0]									00h
68h	1st	R	Read Automatic Brightness Control Self-Diagnostic Result	X	X	X	X	X	X	X	X		XX
	2nd	R		D7	D6	0	0	0	0	0	0		00h
DAh	1st	R	Read ID1	X	X	X	X	X	X	X	X		XX
	2nd	R		ID1[7:0]									E3h
DBh	1st	R	Read ID2	X	X	X	X	X	X	X	X		XX

	2nd	R		ID2[6:0]									00h
DCh	1st	R	Read ID3	X	X	X	X	X	X	X	X		XX
	2nd	R		ID3[7:0]									00h

Level 2 Command		W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)
Address	Parameter											
B0h	1st	W/R	Frame Rate control	RTNA [8]	0	0	0	0	0	0	0	80h
	2nd	W/R		RTNA[7:0]								04h
	3rd	W/R		RTNB [8]	0	0	0	0	0	0	0	80h
	4th	W/R		RTNB[7:0]								04h
	5th	W/R		RTNC [8]	0	0	0	0	0	0	0	80h
	6th	W/R		RTNC[7:0]								04h
	7th	W/R		TE_1M[7:0]								10h
B1h	1st	W/R	Display Inversion Control	0	0	DINVA[1:0]		0	0	DINVB[1:0]		00h
B7h	1st	W/R	Source Chopper Control	0	1	0	1	1	0	1	0	5Ah
	2nd	W/R		0	1	0	0	0	0	0	1	41h
	3rd	W/R		0	0	0	1	0	0	0	1	11h
	4th	W/R		0	0	0	line_ chop_ shift_ en	frame_ chopper_ opt[1:0]		line_ chopper_ opt[1:0]		1Ah
	5th	W/R		0	0	0	0	chopp er_opt	0	0	0	00h
B8h	1st	W/R	Gate Control	0	0	0	1	0	0	0	1	11h
	2nd	W/R		0	0	1	1	1	0	gsw _mode[1:0]		3Bh
BAh	1st	W/R	Pump Frequency Selection	1	0	vgl_clk_ fast_a[1:0]		1	0	vgh_clk_ fast_a[1:0]		99h
	2nd	W/R		0	1	vsnac_clk_ fast_a[1:0]		0	1	vspac_clk_ fast_a[1:0]		55h
	3rd	W/R		0	1	vsndc_clk_ fast_a[1:0]		0	1	vspdc_clk_ fast_a[1:0]		55h
	4th	-		1	0	0	0	1	1	0	0	8Ch
	5th	W/R		1	0	vgl_clk_ fast_b[1:0]		1	0	vgl_clk_ fast_b[1:0]		99h
	6th	W/R		0	1	vsnac_clk_ fast_b[1:0]		0	1	vsnac_clk_ fast_b[1:0]		55h
	7th	W/R		0	1	vsndc_clk_ fast_b[1:0]		0	1	vsndc_clk_ fast_b[1:0]		55h
	8th	-		0	0	0	0	1	1	0	0	0Ch
	9th	W/R		1	0	vgl_clk_ fast_c[1:0]		1	0	vgl_clk_ fast_c[1:0]		99h
	10th	W/R		0	1	vsnac_clk_ fast_c[1:0]		0	1	vsnac_clk_ fast_c[1:0]		55h
	11th	W/R		0	1	vsndc_clk_ fast_c[1:0]		0	1	vsndc_clk_ fast_c[1:0]		55h
C2h	1st	-	Pow er Control 1	0	0	0	0	0	0	0	0	00h
	2nd	-		0	1	1	0	0	1	0	0	64h
	3rd	-		0	0	0	0	0	0	0	0	00h
	4th	W/R		VGL_SEL[3:0]				VGH_SEL[3:0]				89h
	5th	-		0	0	1	1	1	1	0	0	3Ch
	6th	W/R		0	0	0	0	0	VSP_DC_SEL[2:0]			03h
	7th	W/R		0	0	0	0	0	VSP_AC_SEL[2:0]			03h
	8th	W/R		0	0	0	0	0	VSN_DC_SEL[2:0]			03h
	9th	W/R		0	0	0	0	0	VSN_AC_SEL[2:0]			03h

	10th	W/R		0	0	0	0	0	VDDN_SEL[2:0]				02h
C3h	1st	-	Power Control 2	0	0	0	0	1	1	1	1		0Fh
	2nd	-		0	0	0	1	0	1	1	0		16h
	3rd	-		0	0	0	0	0	1	1	1		07h
	4th	-		0	1	1	0	0	1	0	1		65h
	5th	-		1	1	1	0	1	1	0	0		ECh
	6th	-		1	1	0	0	1	1	1	1		CFh
	7th	W/R		0	0	0	0	0	1	LVD_VCI_EN	LVD_IOVCC_EN		07h
C8h	1st	W/R	Power Control 3	0	VCOM[6:0]								5Ah
C9h	1st	W/R	Power Control 4	0	0	VRH_DOT[5:0]							13h
CAh	1st	W/R	Power Control 5	0	0	VRH_COL[5:0]							13h
CBh	1st	W/R	Power Control 6	0	0	VDV[5:0]							20h
D0h	1st	W/R	RGB Interface Signal Control	Bypass_Mode	0	RCM[1:0]		VSPL	HSPL	DPL	EPL		20h
D1h	1st	W/R	Blanking Porch Control	VFP[7:0]									02h
	2nd	W/R		VBP[7:0]									02h
	3rd	W/R		0	0	0	0	1	0	1	0		0Ah
	4th	W/R		HBP[7:0]									14h
D2h	1st	W/R	Display Function Control	0	0	0	0	PTG[1:0]		PT[1:0]			0Ah
	2nd	W/R		REV	GS	SS	SM	ISC[3:0]					82h
	3rd	W/R		0	NL[6:0]								77h
D5h	1st	W/R	MADCTL_EOR Control	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	0	0		00h
D8h	1st	W/R	Interface Control	0	0	EPF[1:0]		0	0	MDT[1:0]			00h
	2nd	W/R		0	0	ENDIAN	0	DM[1:0]		RM	RIM		00h
D9h	1st	W/R	Get External Register for SPI	0	0	0	ext_spi_read_en	ext_spi_cnt[3:0]					00h
DDh	1st	W/R	Set EXTC	0	0	0	0	0	0	0	EXTC_EN		00h
DEh	1st	W/R	NV Memory Program Setting	0	0	0	0	0	0	0	0		00h
	2nd	W/R		0	0	0	0	0	0	0	0		00h
	3rd	W/R		0	0	0	0	0	0	0	0		00h
	4th	W/R		0	0	0	0	0	0	0	0		00h
	5th	W/R		otp_te_sel[3:0]				0	0	0	0		00h
DFh	1st	W/R	Smart Resolution Setting	0	0	0	reso_gm	sreso_en	0	0	sreso_col_num[8]		01h
	2nd	W/R		sreso_col_num[7:0]									40h
E1h	1st	W/R	Memory Control	0	0	0	0	0	0	0	0		00h
	2nd	W/R		0	0	1	0	0	0	0	wemode		20h
E4h	1st	W/R	Positive Gamma Correction	0	0	0	0	VP0[3:0]					00h
	2nd	W/R		0	0	VP1[5:0]							05h
	3rd	W/R		0	0	VP2[5:0]							12h
	4th	W/R		0	0	0	0	VP4[3:0]					09h
	5th	W/R		0	0	0	VP6[4:0]						17h
	6th	W/R		0	0	0	0	VP13[3:0]					08h
	7th	W/R		0	VP20[6:0]								40h
	8th	W/R		VP36[3:0]				VP27[3:0]					55h
	9th	W/R		0	VP43[6:0]								50h
	10th	W/R		0	0	0	0	VP50[3:0]					04h
	11th	W/R		0	0	0	VP57[4:0]						0Ah
	12th	W/R		0	0	0	0	VP59[3:0]					07h
	13th	W/R		0	0	VP61[5:0]							21h

	14th	W/R		0	0	VP62[5:0]							24h
	15th	W/R		0	0	0	0	VP63[3:0]					0Dh
E5h	1st	W/R	Negative Gamma Correction	0	0	0	0	VN0[3:0]					00h
	2nd	W/R		0	0	VN1[5:0]							05h
	3rd	W/R		0	0	VN2[5:0]							11h
	4th	W/R		0	0	0	0	VN4[3:0]					09h
	5th	W/R		0	0	0	VN6[4:0]						17h
	6th	W/R		0	0	0	0	VN13[3:0]					09h
	7th	W/R		0	VN20[6:0]								40h
	8th	W/R		VN36[3:0]				VN27[3:0]					46h
	9th	W/R		0	VN43[6:0]								4Eh
	10th	W/R		0	0	0	0	VN50[3:0]					08h
	11th	W/R		0	0	0	VN57[4:0]						0Fh
	12th	W/R		0	0	0	0	VN59[3:0]					0Ch
	13th	W/R		0	0	VN61[5:0]							21h
	14th	W/R		0	0	VN62[5:0]							25h
	15th	W/R		0	0	0	0	VN63[3:0]					0Dh
E8h	1st	W/R	Backlight Control 1	1	1	1	1	1	1	1	1		FFh
	2nd	W/R		0	0	0	0	0	ledon	ledon_pol	pwm_pol		00h
E9h	1st	W/R	Backlight Control 2	THRES_MOV[3:0]				THRES_STILL[3:0]					BBh
	2nd	W/R		0	0	0	0	THRES_UI[3:0]					0Bh
EAh	1st	W/R	Backlight Control 3	DTH_MOV[3:0]				DTH_STILL[3:0]					A8h
	2nd	W/R		0	0	0	0	DTH_UI[3:0]					03h
EBh	1st	W/R	Backlight Control 4	0	cabc_dim_mov[2:0]			0	cabc_dim_still[2:0]				43h
	2nd	W/R		cabc_dim_min[3:0]				0	cabc_dim_ui[2:0]				02h
ECh	1st	W/R	Backlight Control 5	PWM_DIV[7:0]									D0h
EFh	1st	W	ID code setting	REG_ID1[7:0]									E3h
	2nd	W		REG_ID2[7:0]									00h
	3rd	W		REG_ID3[7:0]									00h
F8h	1st	-	NV Memory Control and Status Read	0	0	0	0	0	0	0	0		00h
	2nd	-		0	0	0	1	0	0	0	0		10h
	3rd	-		0	0	0	1	0	0	1	0		12h
	4th	-		0	0	0	0	0	0	0	0		00h
	5th	-		0	0	0	0	0	0	0	0		00h
	6th	-		0	0	0	0	0	0	0	0		00h
	7th	-		0	0	0	0	0	0	0	0		00h
	8th	R		prog_finish	prog_finish_fail	0	0	0	0	0	0		00h
	9th	W/R		0	0	0	0	0	0	otp_finish_flag_sel[1:0]			00h
F9h	1st	W/R	NV Memory Control	0	0	0	0	0	0	0	mtp_pump_set_en		00h
FDH	1st	W	NV Memory Write	pgm_adr[7:0]									-
	2nd	W		pgm_adr[15:8]									-
	3rd	W		pgm_data[7:0]									-
FEh	1st	W	NV Memory Protection Key	KEY[23:16]									55h
	2nd	W		KEY[15:8]									AAh
	3rd	W		KEY[7:0]									66h
FFh	1st	R	NV Memory Status Read	X	X	X	X	X	X	X	X		XX
	2nd	R		0	0	0	0	0	0	0	0		00h
	3rd	R		madctl_mark[1:0]		id3_mark[1:0]		id2_mark[1:0]		id1_mark[1:0]			00h
	4th	R		0	0	0	gamma_mark	0	vcm_mark[2:0]				00h

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP (00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9342E is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.

5.2. Description of Level 1 Command

5.2.1. NOP (00h)

00h	NOP (No Operation)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	0	0	0	00h
Parameter	No Parameter.											
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.											
Restriction	None											
Register Availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart: None

5.2.2. Software Reset (01h)

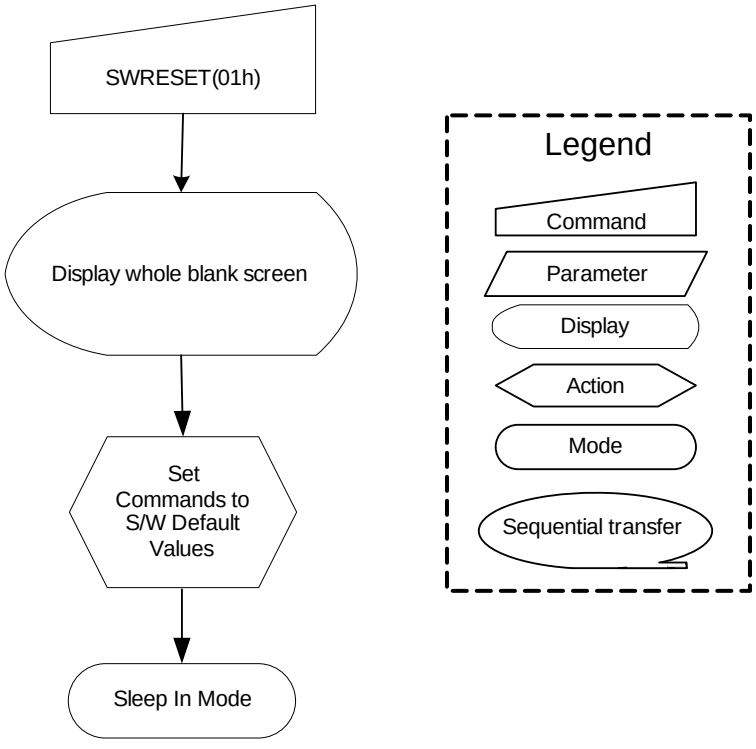
01h	SWRESET											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	0	0	1	01h
Parameter	No Parameter.											
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = Don't care.											
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.											
Register Availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



5.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	ID1 [7:0]								E3
3rd Parameter	1	↑	1	ID2 [7:0]								00
4th Parameter	1	↑	1	ID3 [7:0]								00

Description

This read byte returns 24 bits display identification information.

The 1st parameter is dummy data.

The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID.

The 3rd parameter (ID2 [7:0]): LCD module/driver version ID.

The 4th parameter (ID3 [7:0]): LCD module/driver ID.

Restriction

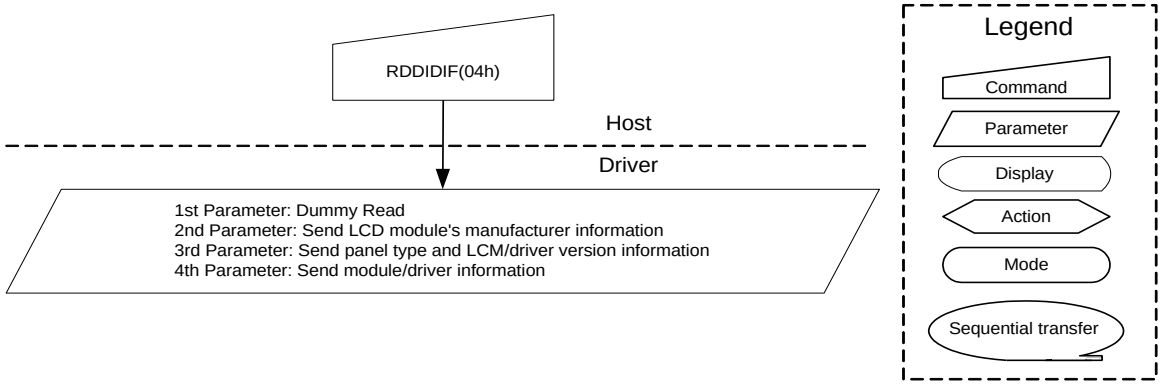
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OTP Value
SW Reset	OTP Value
HW Reset	OTP Value

Flow Chart

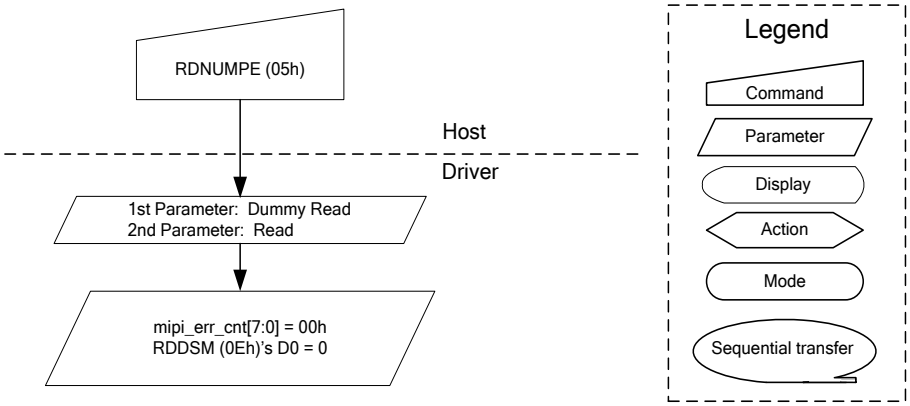


5.2.4. Read Number of the Errors on DSI (05h)

05h	Read Number of the Errors on DSI											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	1	0	1	05h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	mipi_error_cnt[7:0]								00
Description	The parameter tells the number of errors on DSI. The more details of the bits are described as below. mipi_error_cnt[6..0] bits tells the number of the error. mipi_error_cnt[7] is set to '1' if there is overflow with mipi_error_cnt [6..0] bits. mipi_error_cnt[7...0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after the parameter information is sent (= The read function is completed).This function always returns mipi_error_cnt [7...0] = 00h if the parallel MPU interface is selected.											
Restriction												
Register Availability												
Default												
Flow Chart												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h



5.2.5. Read Display Status (09h)

09h	RDDST (Read Display Status)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D31	D30	D29	D28	D27	D26	D25	D24	00
3rd Parameter	1	↑	1	D23	D22	D21	D20	D19	D18	D17	D16	61
4th Parameter	1	↑	1	D15	D14	D13	D12	D11	D10	D9	D8	00
5th Parameter	1	↑	1	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below :

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster Off
		1	Booster On
D30	Row address order	0	Top to Bottom (When MADCTL D7='0')
		1	Bottom to Top (When MADCTL D7='1')
D29	Column address order	0	Left to Right (When MADCTL D6='0').
		1	Right to Left (When MADCTL D6='1').
D28	Row /column exchange	0	Normal Mode (When MADCTL D5='0').
		1	Reverse Mode (When MADCTL D5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL D4='0')
		1	LCD Refresh Bottom to Top (When MADCTL D4='1').
D26	RGB/BGR order	0	RGB (When MADCTL D3='0')
		1	BGR (When MADCTL D3='1')
D25	Not used	0	---
D24	Not used	0	---
D23	Not used	0	---
D22	Interface color pixel format definition (DBI [2:0])	101	16-bit/pixel
D21		110	18-bit/pixel
D20		other	Not defined
D19	Idle mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D18	Partial mode On/Off	0	Partial Mode Off
		1	Partial Mode On.
D17	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode.
D16	Display normal mode On/Off	0	Display Normal Mode Off.
		1	Display Normal Mode On.
D15	Vertical scrolling status	0	Vertical Scrolling is Off
		1	Vertical Scrolling is On
D14	Not used	0	---
D13	Inversion On/Off	0	Inversion is Off
		1	Inversion is On
D12	Not used	0	---
D11	Not used	0	---
D10	Display On/Off	0	Display is Off
		1	Display is On
D9	Tearing effect line On/Off	0	Tearing Effect Line Off
		1	Tearing Effect On
D[8:6]	Gamma curve selection	000	GC0(Gamma 2.2)
		other	Not defined
D5	Tearing effect line mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking.
D4	Horizontal Sync.	0	Horizontal Sync. line is Off (Low)

		(HSYNC, DPI I/F) (Note)	1	Horizontal Sync. line is On (High)
	D3	Vertical Sync. (VSYNC, DPI I/F) (Note)	0	Vertical Sync. line is Off (Low)
			1	Vertical Sync. line is On (High)
	D2	DOT Clock (DCK, DPI I/F) (Note)	0	DCK line is Off (Low)
			1	DCK line is On (High)
	D1	Data Enable (ENABLE, DPI I/F) (Note)	0	DE line is Off (Low)
			1	DE line is On (High)
	D0	Error on DSI	0	No Error on DSI
			1	Error on DSI

Restriction

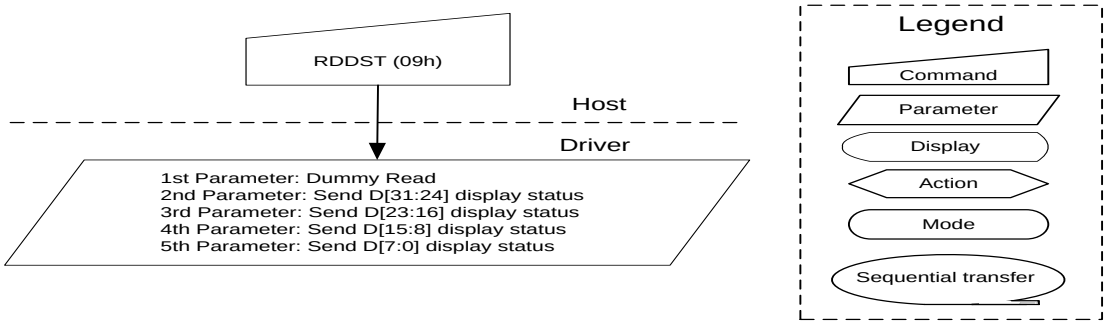
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32'h00610000h
SW Reset	32'h00610000h
HW Reset	32'h00610000h

Flow Chart



5.2.6. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D7	D6	D5	D4	D3	D2	0	0	08

Description

This command indicates the current status of the display as described in the table below :

Bit	Value	Description	Comment
D7	0	Booster Off or has a fault.	---
	1	Booster On and working OK	---
D6	0	Idle Mode Off.	---
	1	Idle Mode On.	---
D5	0	Partial Mode Off.	---
	1	Partial Mode On.	---
D4	0	Sleep In Mode	---
	1	Sleep Out Mode	---
D3	0	Display Normal Mode Off.	---
	1	Display Normal Mode On	---
D2	0	Display is Off.	---
	1	Display is On	---
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

Restriction

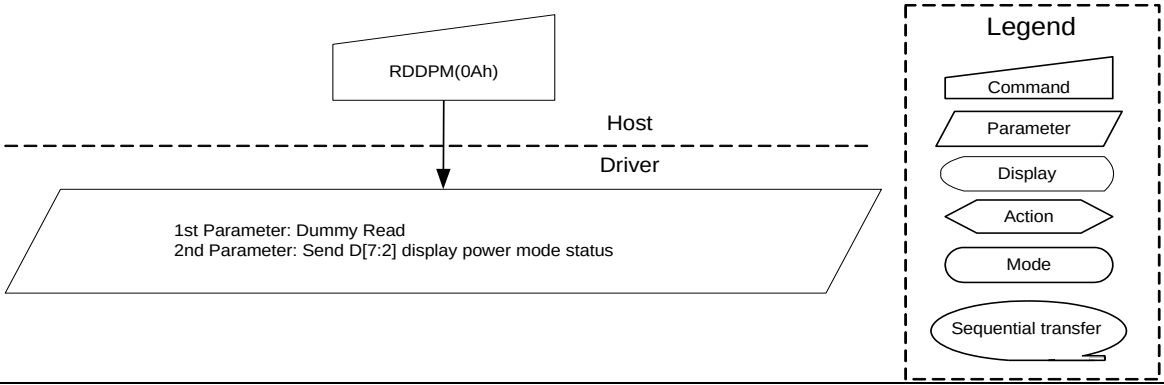
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h08h
SW Reset	8'h08h
HW Reset	8'h08h

Flow Chart



5.2.7. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D7	D6	D5	D4	D3	0	0	0	00

Description

This command indicates the current status of the display as described in the table below :

Bit	Value	Description	Comment
D7	0	Top to Bottom (When MADCTL D7='0').	---
	1	Bottom to Top (When MADCTL D7='1').	---
D6	0	Left to Right (When MADCTL D6='0')	---
	1	Right to Left (When MADCTL D6='1')	---
D5	0	Normal Mode (When MADCTL D5='0').	---
	1	Reverse Mode (When MADCTL D5='1')	---
D4	0	LCD Refresh Top to Bottom (When MADCTL D4='0')	---
	1	LCD Refresh Bottom to Top (When MADCTL D4='1').	---
D3	0	RGB (When MADCTL D3='0')	---
	1	BGR (When MADCTL D3='1').	---
D2	--	Not Defined	Set to '0'
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

Restriction

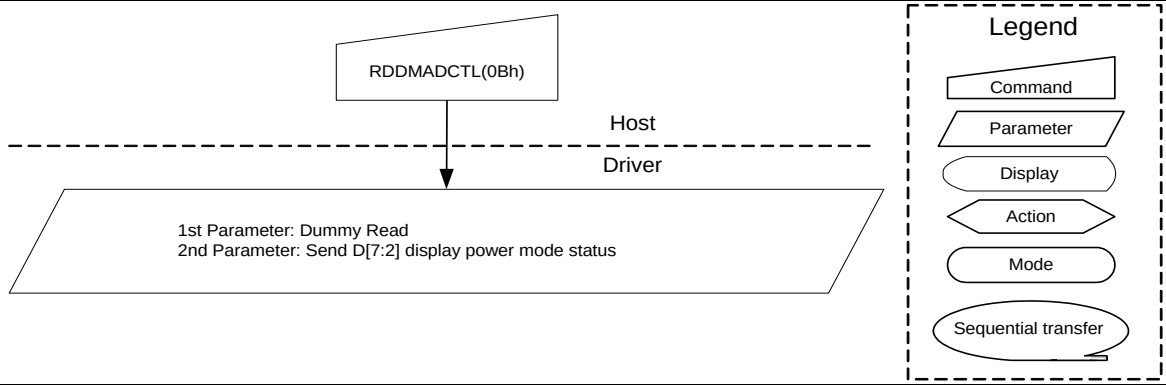
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

Flow Chart



5.2.8. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display Pixel Format)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	0	DPI [2:0]			0	DBI [2:0]			06

Description

This command indicates the current status of the display as described in the table below :

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	24 bits / pixel

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

Restriction

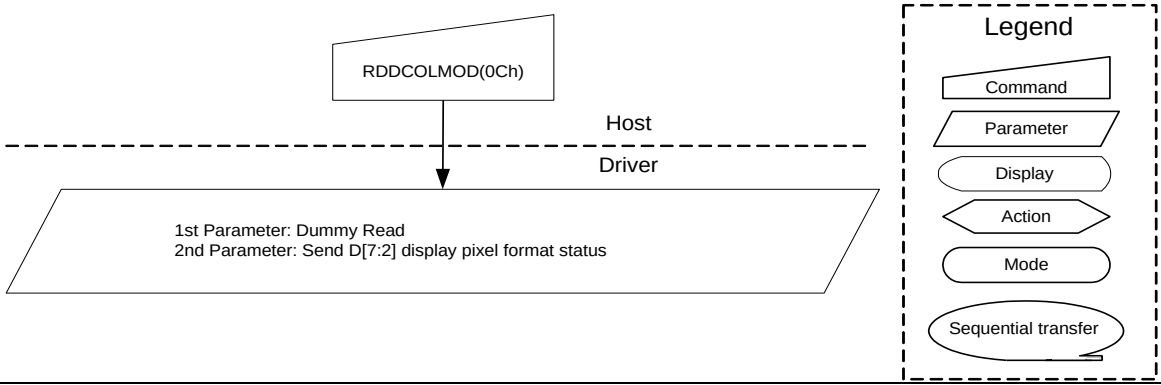
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b000	3'b110
SW Reset	No Change	No Change
HW Reset	3'b000	3'b110

Flow Chart



5.2.9. Read Display Image Mode (0Dh)

0Dh	RDDIM (Read Display Image Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D7	0	D5	0	0	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below :

Bit	Description	Value	Status
D7	Vertical Scrolling Status	0	Vertical Scrolling is Off
		1	Vertical Scrolling is On
D5	Inversion On/Off	0	Inversion is Off
		1	Inversion is On
D[2:0]	Gamma Curve Selection	000	GC0(Gamma 2.2)
		other	Not defined

Restriction

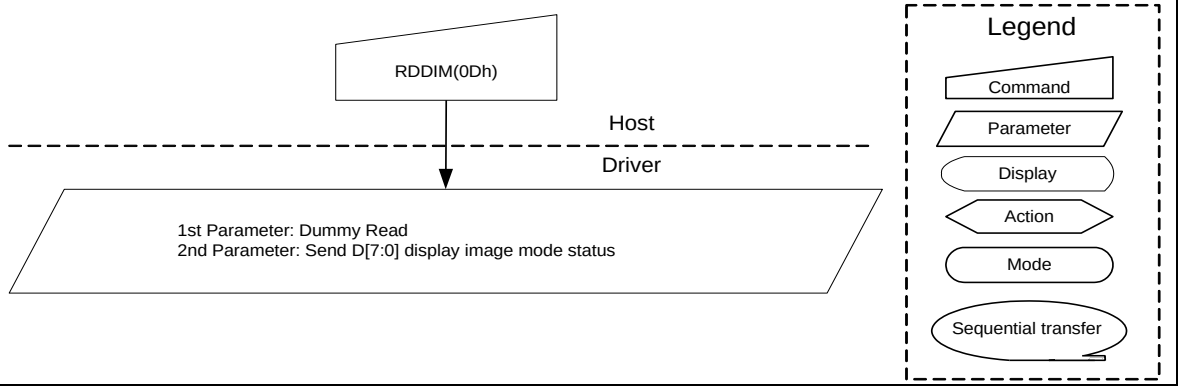
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



5.2.10. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D7	D6	0	0	0	0	0	D0	00

Description

This command indicates the current status of the display as described in the table below :

Bit	Description	Value	Status
D7	Tearing Effect Line On/Off	0	Tearing Effect Line Off.
		1	Tearing Effect Line On.
D6	Tearing Effect Line Output Mode	0	Tearing Effect Line Mode 1
		1	Tearing Effect Line Mode 2
D5	Reserved	0	Reserved, so it is set to '0'
D4	Reserved	0	Reserved, so it is set to '0'
D3	Reserved	0	Reserved, so it is set to '0'
D2	Reserved	0	Reserved, so it is set to '0'
D1	Reserved	0	Reserved, so it is set to '0'
D0	Error on DSI,	0	No Error on DSI
		1	Error on DSI

Restriction

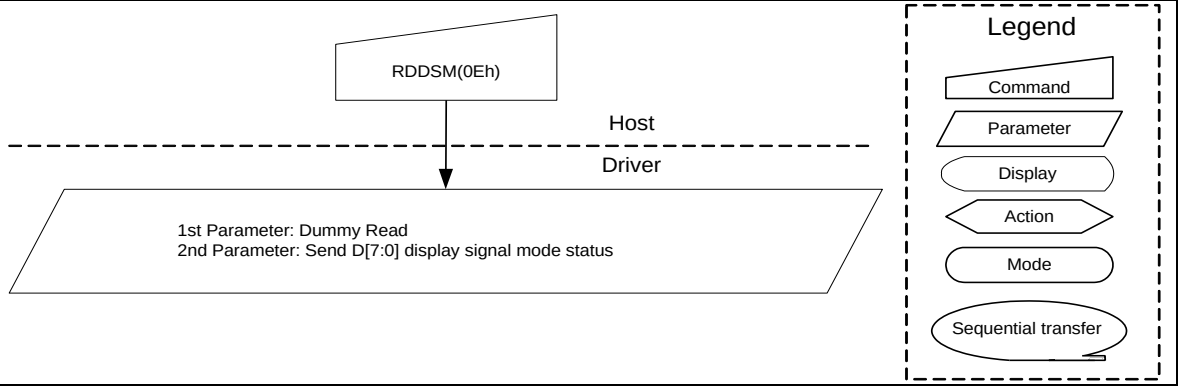
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



5.2.11. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)											
	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading w ork properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

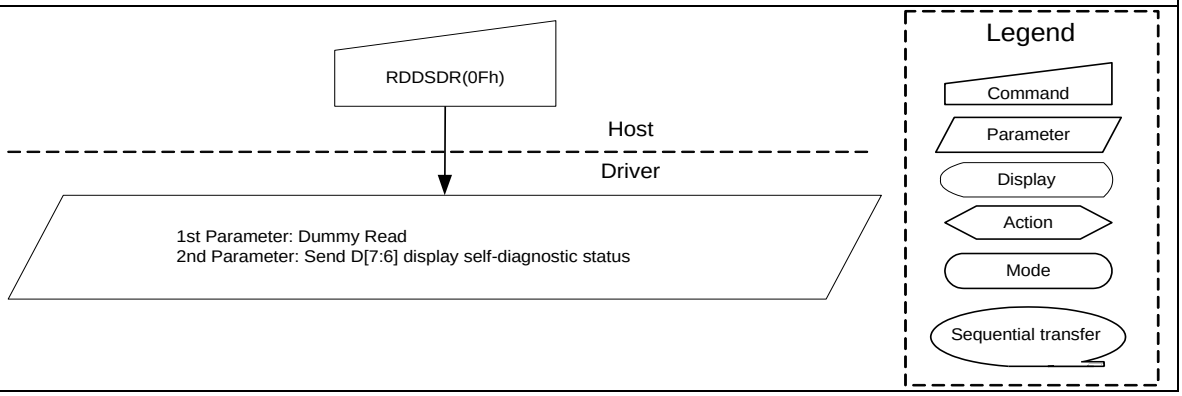
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Pow er On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



5.2.12. Enter Sleep Mode (10h)

10h	SPLIN (Enter Sleep Mode)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter											
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Out → Blank → STOP MCU interface and memory are still working and the memory keeps its contents.											
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.											
Register Availability												

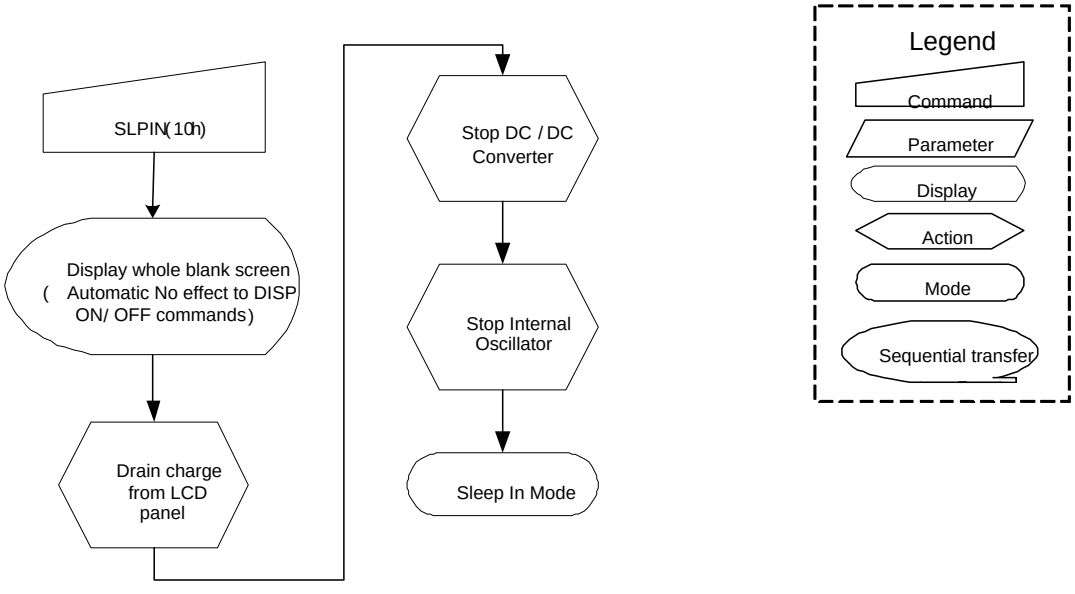
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



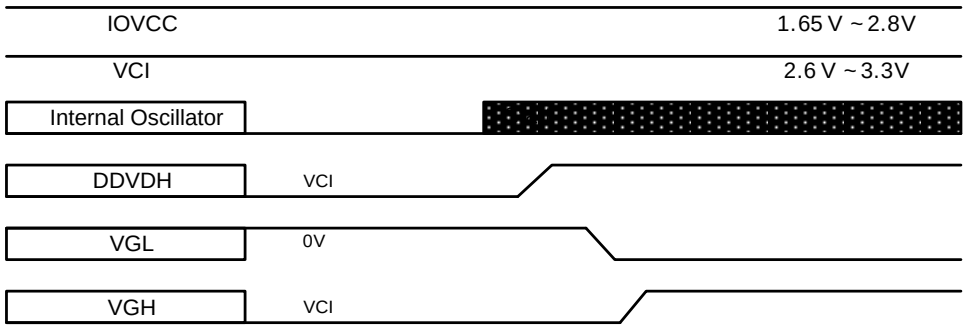
5.2.13. Sleep Out (11h)

11h	SLPOUT (Sleep Out)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	1	0	0	0	1	11h
Parameter	No Parameter											

Description

This command turns off sleep mode.

In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.



Restriction

This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this 120msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

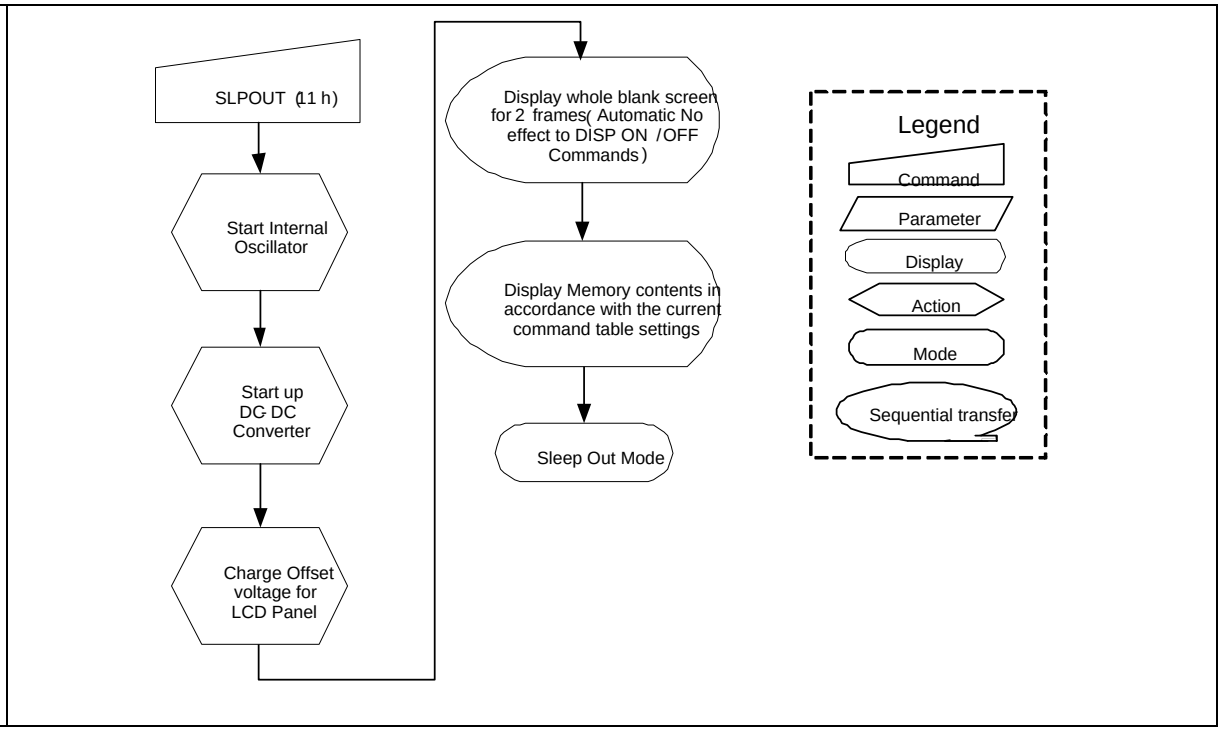
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



5.2.14. Partial Mode ON (12h)

<table>
<tr><th>12h</th><th colspan="12">PTLON (Partial Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

5.2.15. Normal Display Mode ON (13h)

<table>
<tr><th>13h</th><th colspan="12">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

5.2.16. Display Inversion OFF (20h)

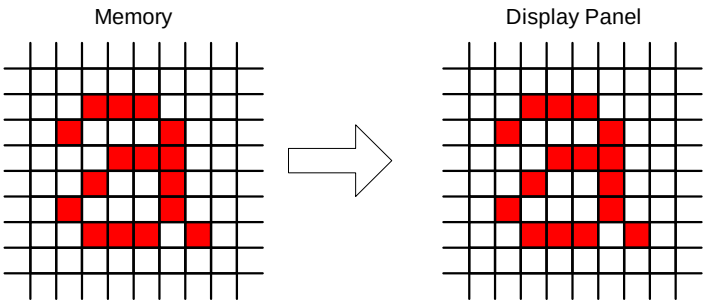
20h	DINVOFF (Display Inversion OFF)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter											

Description

This command is used to recover from display inversion mode.

This command makes no change of the content of frame memory.

This command doesn't change any other status.



Restriction

This command has no effect when module already is inversion OFF mode.

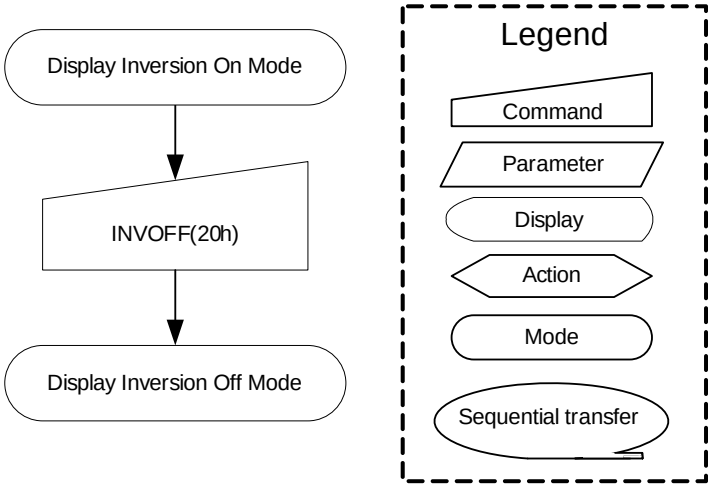
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

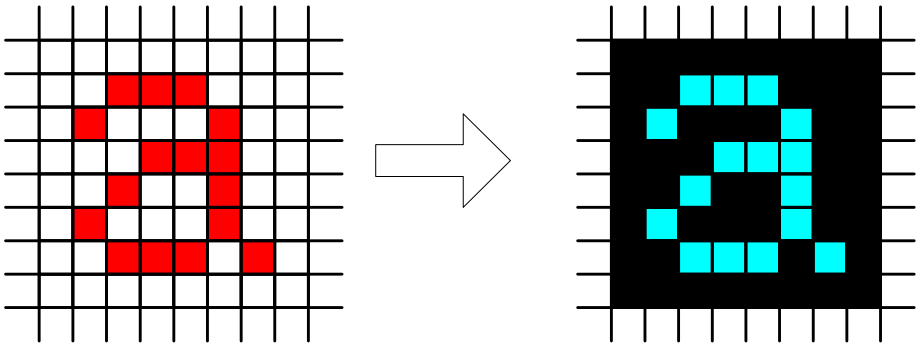
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



5.2.17. Display Inversion ON (21h)

21h	DINVON (Display Inversion ON)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter											
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written. 											
Restriction	This command has no effect when module already is inversion ON mode.											

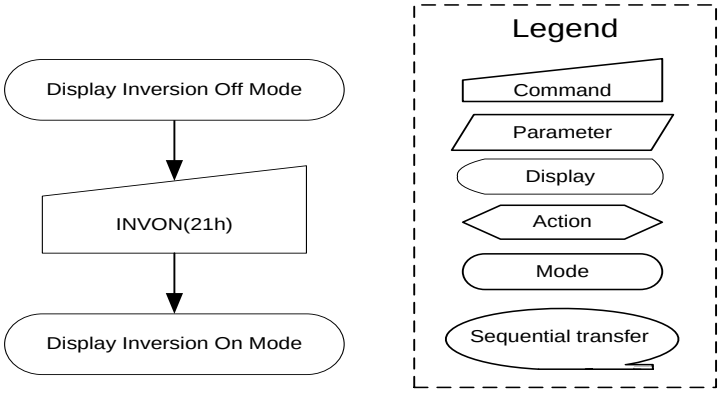
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



5.2.18. Display OFF (28h)

28h	DISPOFF (Display OFF)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter											

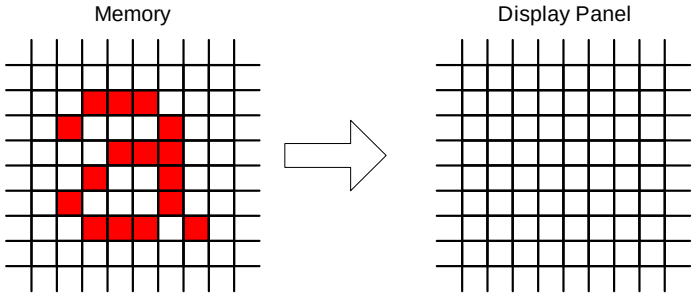
Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.

This command makes no change of contents of frame memory.

This command does not change any other status.

There will be no abnormal visible effect on the display.



Restriction

This command has no effect when module is already in display off mode.

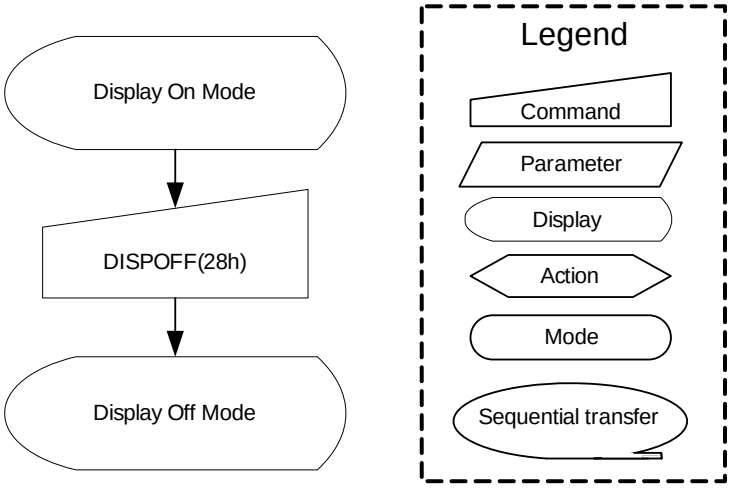
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

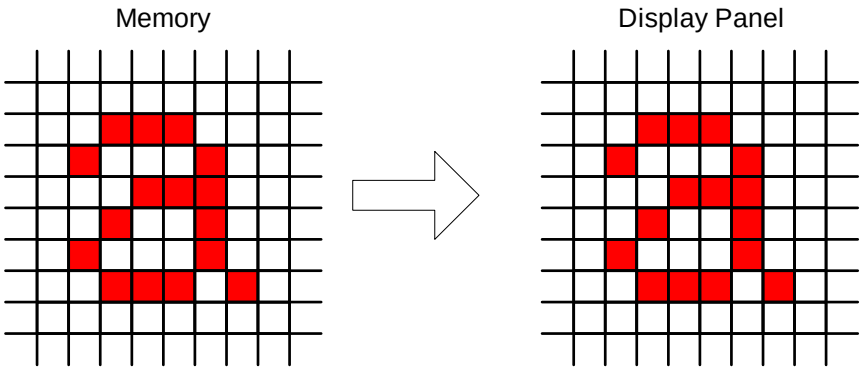
Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



5.2.19. Display ON (29h)

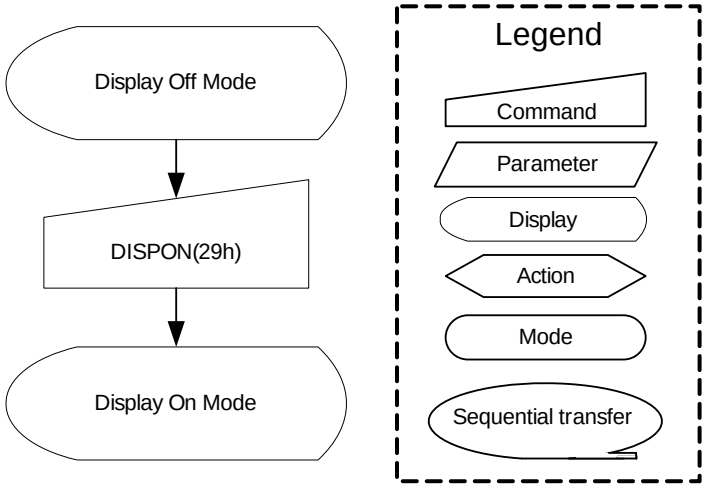
29h	DISPON (Display ON)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter											
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status 											
Restriction	This command has no effect when module is already in display on mode.											
Register Availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

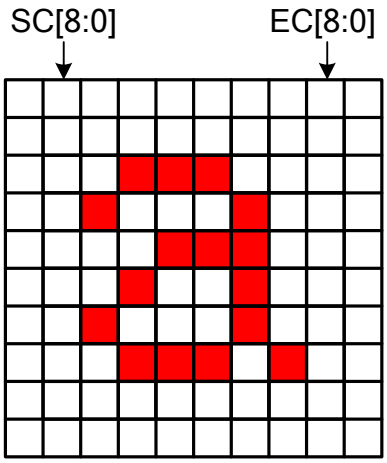


5.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑								SC[8]	Note1
2nd Parameter	1	1	↑	SC[7:0]								
3rd Parameter	1	1	↑								EC[8]	Note1
4th Parameter	1	1	↑	EC[7:0]								

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [8:0] and EC [8:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

SC [8:0] always must be equal to or less than EC [8:0].

Note 1: When SC [8:0] or EC [8:0] is greater than 0EFh (When MADCTL's D5 = 0) or 13Fh (When MADCTL's D5 = 1), data of out of range will be ignored

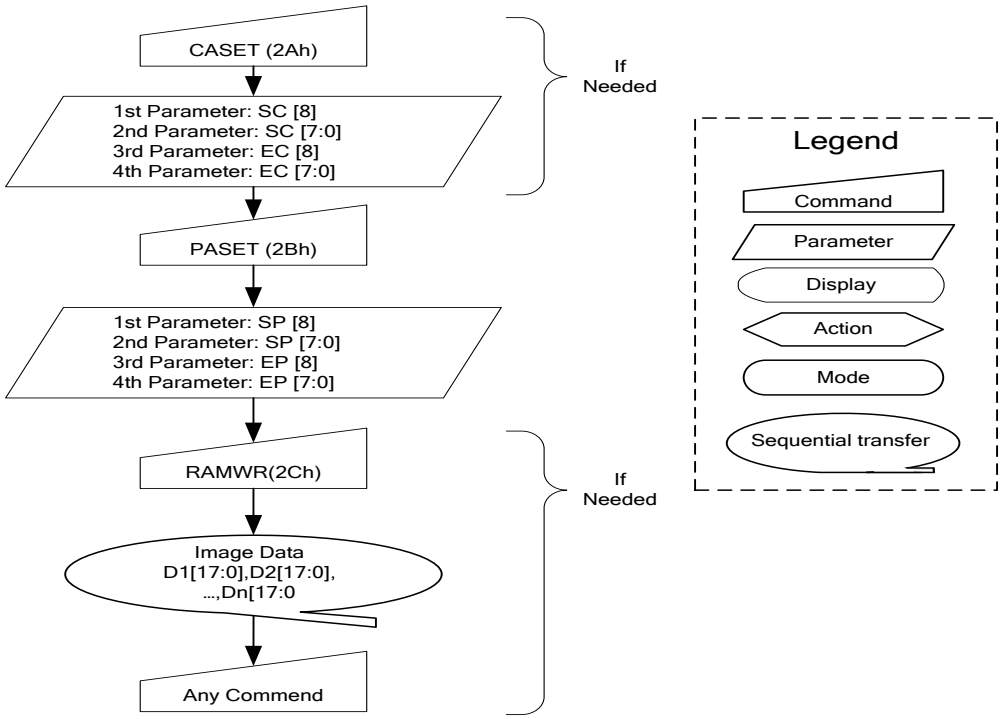
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [8:0]=000h	EC [8:0]=13Fh
SW Reset	SC [8:0]=000h	If MADCTL's D5 = 0: EC [8:0]=13Fh If MADCTL's D5 = 1: EC [8:0]=0EFh
HW Reset	SC [8:0]=000h	EC [8:0]=13Fh

Flow Chart

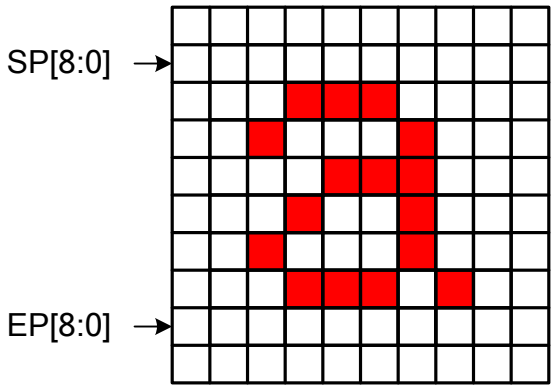


5.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	0	0	0	0	0	0	0	SP[8]	Note1
2nd Parameter	1	1	↑	SP[7:0]								
3rd Parameter	1	1	↑	0	0	0	0	0	0	0	EP[8]	Note1
4th Parameter	1	1	↑	EP[7:0]								

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [8:0] and EP [8:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



Restriction

SP [8:0] always must be equal to or less than EP [8:0]

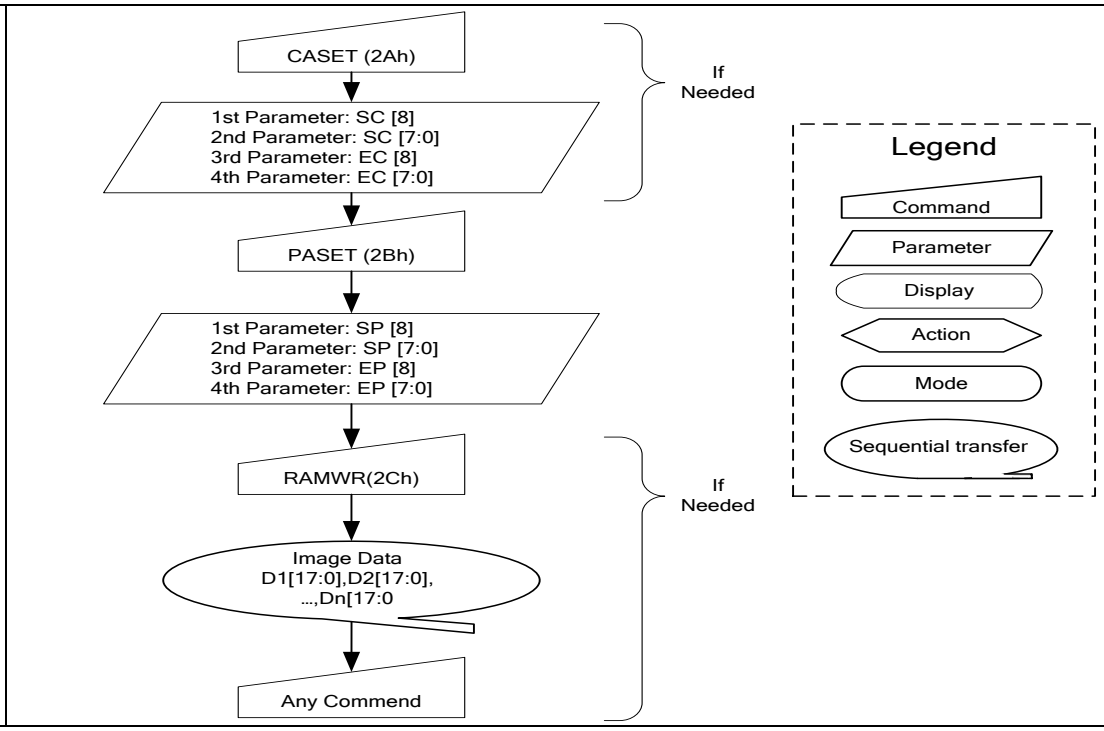
Note 1: When SP [8:0] or EP [8:0] is greater than 13Fh (When MADCTL's D5 = 0) or 00EFh (When MADCTL's D5 = 1), data of out of range will be ignored.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [8:0]=000h	EP [8:0]=0EFh
SW Reset	SP [8:0]=000h	If MADCTL's D5 = 0: EP [8:0]=0EFh If MADCTL's D5 = 1: EP [8:0]=13Fh
HW Reset	SP [8:0]=000h	EP [8:0]=0EFh

Flow Chart	

5.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X X	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write.												
Restriction	In all color modes, there is no restriction on length of parameters.												

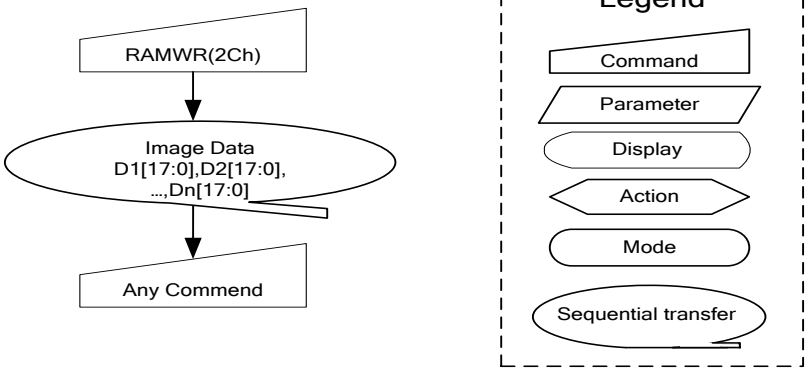
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



5.2.23. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X X	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	↑	1	X X	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D1 [17:0]									XX
:	1	↑	1	Dx [17:0]									XX
(N+1)th Parameter	1	↑	1	Dn [17:0]									XX

Description

This command transfers image data from ILI9342E's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control D5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control D5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

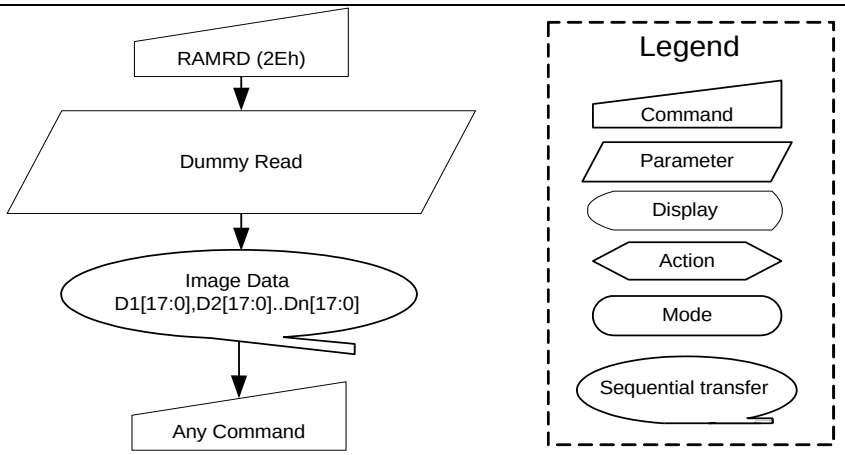
There is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

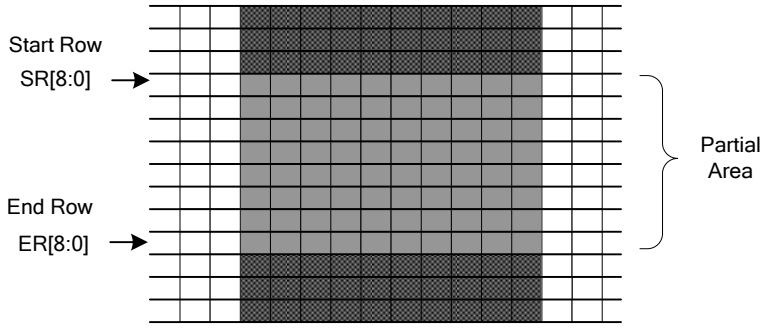
5.2.24. Partial Area (30h)

30h	PLTAR (Partial Area)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	0	0	0	0	0	0	0	SR[8]	00
2nd Parameter	1	1	↑	SR[7:0]								00
3rd Parameter	1	1	↑	0	0	0	0	0	0	0	ER[8]	00
4th Parameter	1	1	↑	ER[7:0]								EF

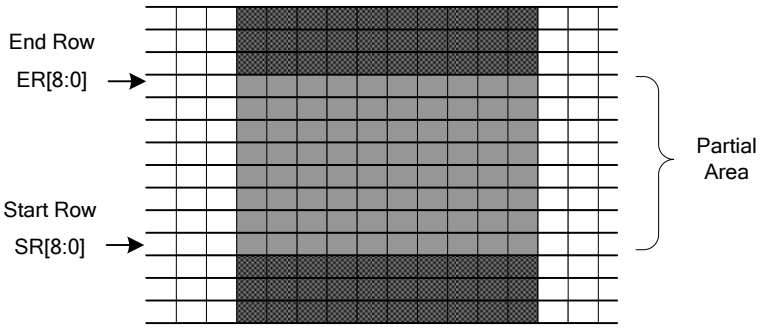
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

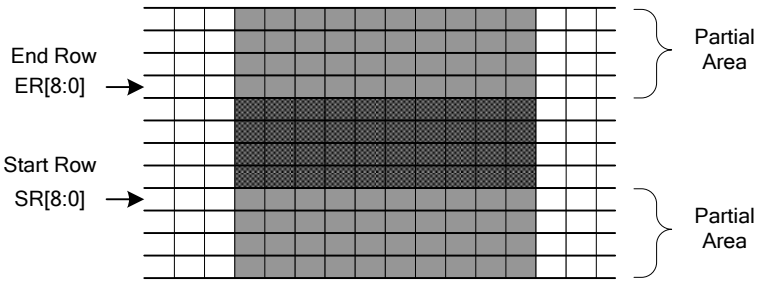
If End Row >Start Row when MADCTL D4=0:-



If End Row >Start Row when MADCTL D4=1:-



If End Row <Start Row when MADCTL D4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

Restriction	SR [8…0] and ER [8…0] cannot be 000h nor exceed 0EFh.

Register Availability

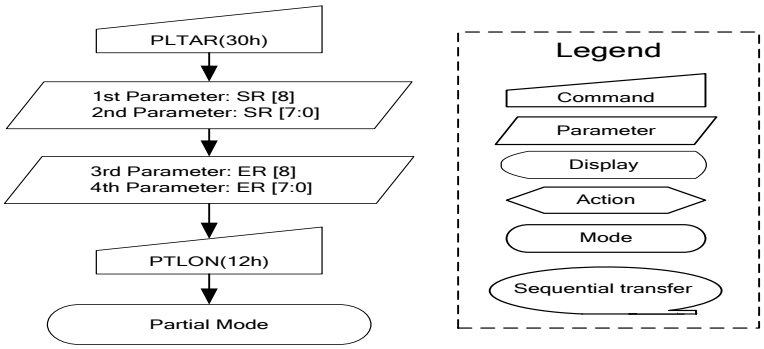
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

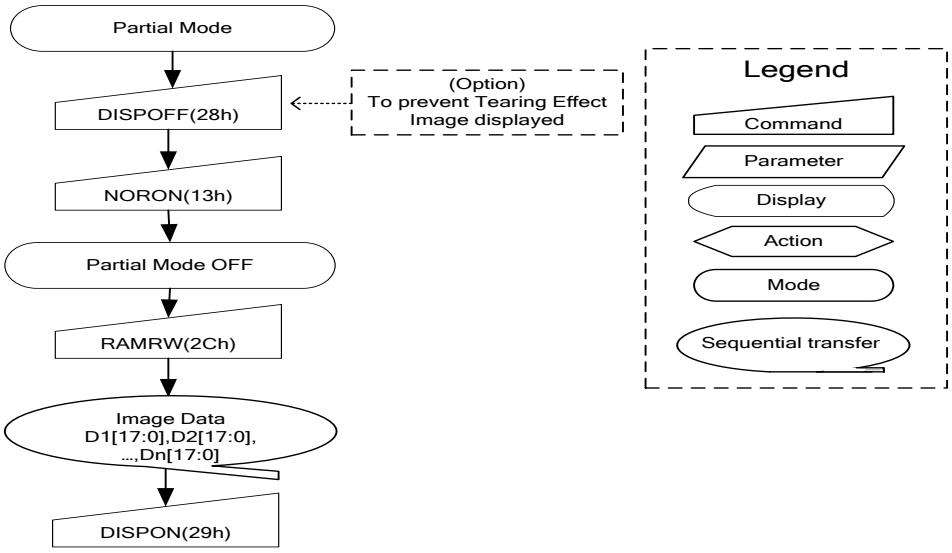
Status	Default Value	
	SR [8:0]	ER [8:0]
Power On Sequence	9'h 000h	9'h0EFh
SW Reset	9'h 000h	9'h0EFh
HW Reset	9'h 000h	9'h0EFh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



5.2.25. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	0	0	0	0	0	0	0	TFA [8]	00
2nd Parameter	1	1	↑	TFA [7:0]								00
3rd Parameter	1	1	↑	0	0	0	0	0	0	0	VSA [8]	00
4th Parameter	1	1	↑	VSA [7:0]								F0
5th Parameter	1	1	↑	0	0	0	0	0	0	0	BFA [8]	00
6th Parameter	1	1	↑	BFA [7:0]								00

Description

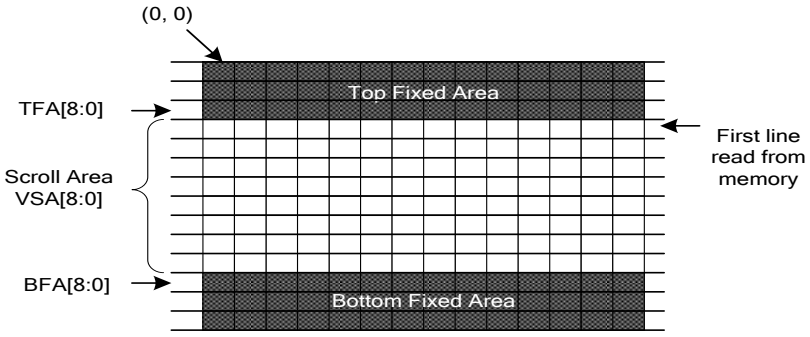
This command defines the Vertical Scrolling Area of the display.

When MADCTL D4=0

The 1st & 2nd parameter TFA [8...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [8...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [8...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.

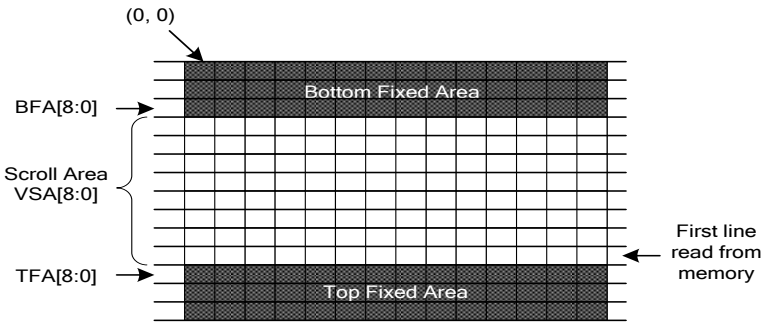


When MADCTL D4=1

The 1st & 2nd parameter TFA [8...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [8...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [8...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



Restriction

Register Availability

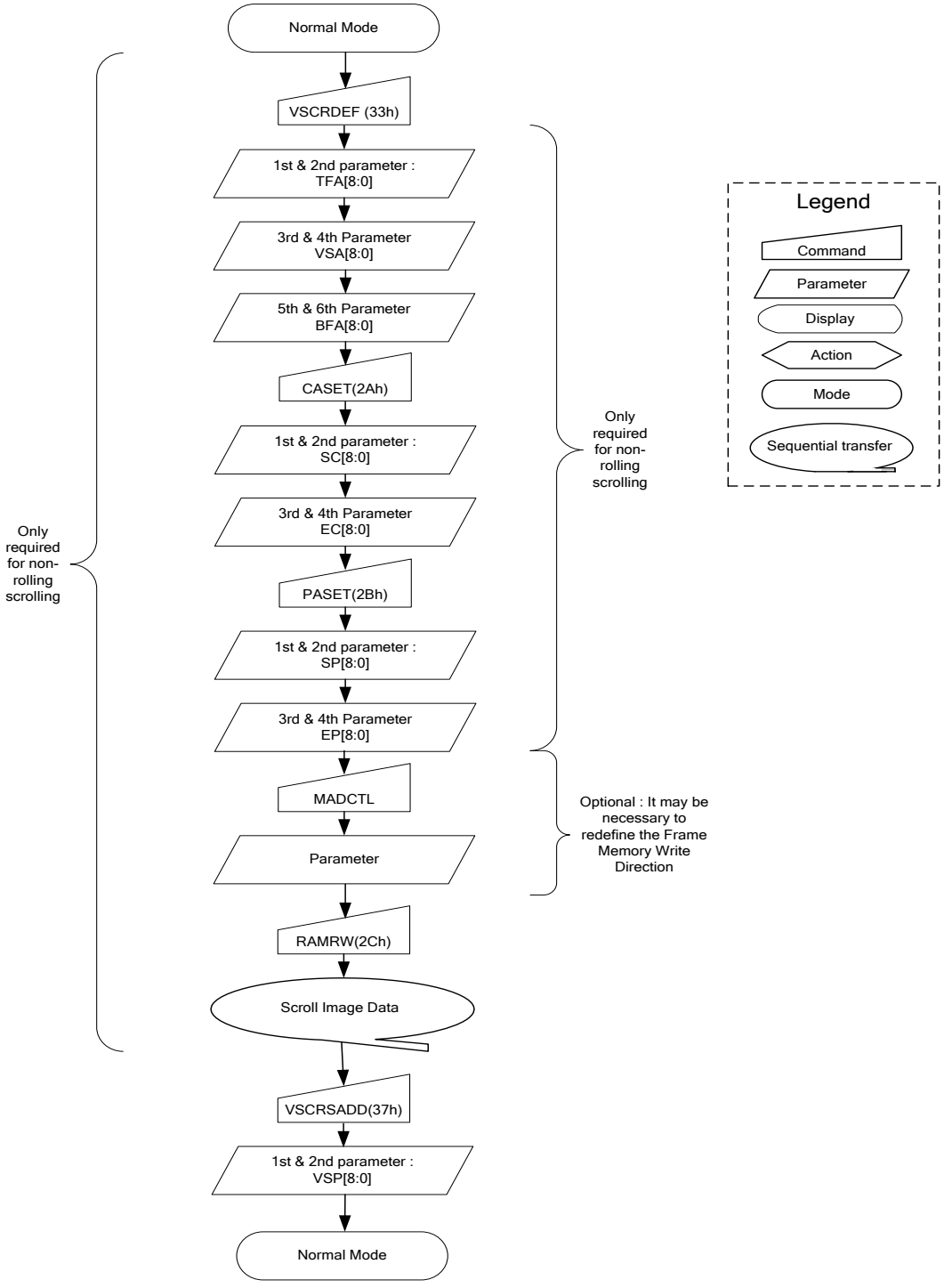
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TFA [8:0]	VSA [8:0]	BFA [8:0]
Power On Sequence	9'h000h	9'h0F0h	9'h000h
SW Reset	9'h000h	9'h0F0h	9'h000h
HW Reset	9'h000h	9'h0F0h	9'h000h

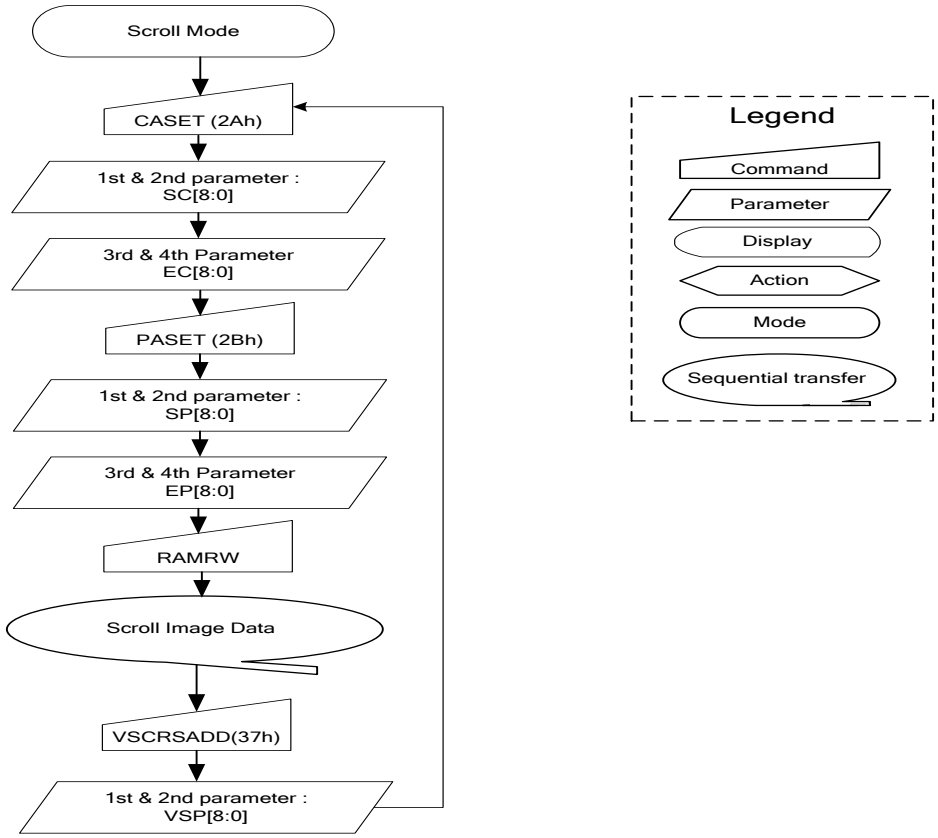
Flow Chart

1. To enter Vertical Scroll Mode :

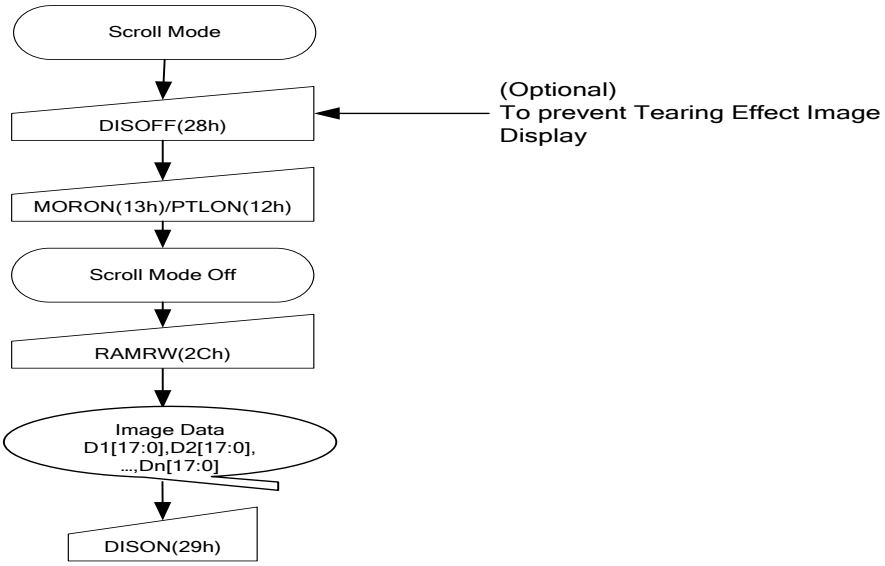


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:



3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

5.2.26. Tearing Effect Line OFF (34h)

34h	TEOFF (Tearing Effect Line OFF)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	0	34h
Parameter	No Parameter											
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.											
Restriction	This command has no effect when Tearing Effect output is already OFF.											

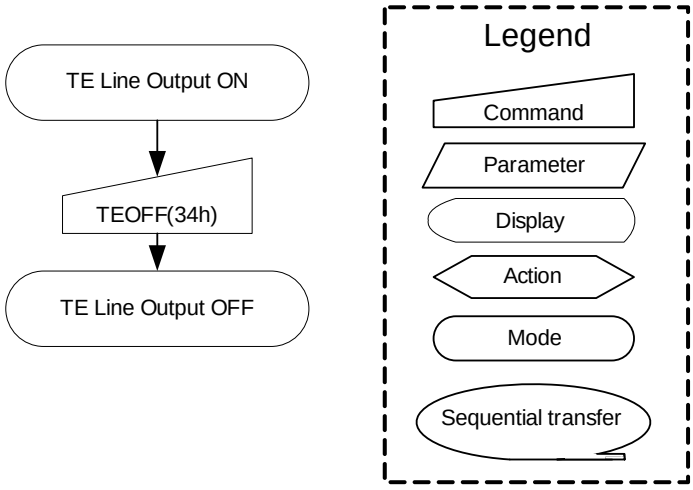
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



5.2.27. Tearing Effect Line ON (35h)

35h	TEON (Tearing Effect Line ON)											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	X	X	X	X	X	X	X	M	00

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit D4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:

When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

Restriction

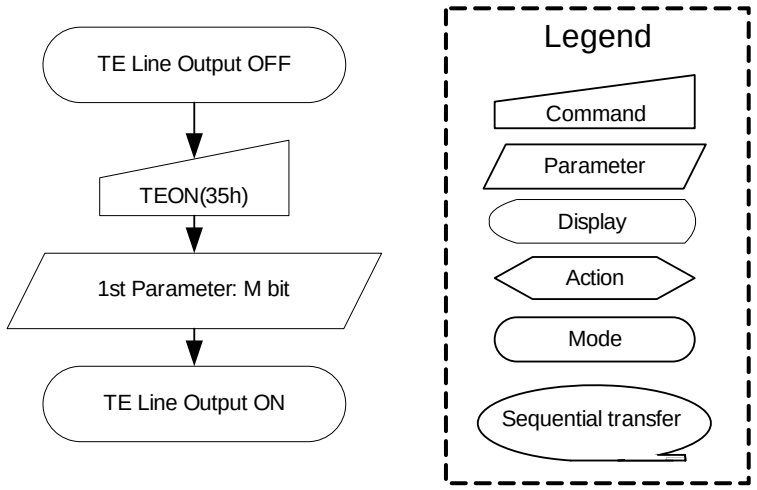
This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

5.2.28. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	MY	MX	MV	ML	BGR	0	0	0	00

Description

This command defines read/write scanning direction of frame memory.

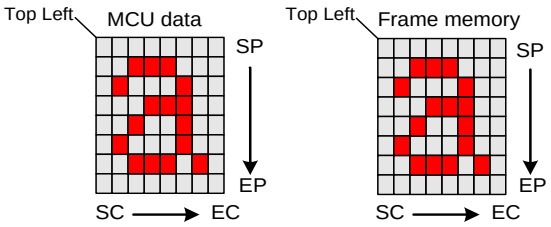
This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)

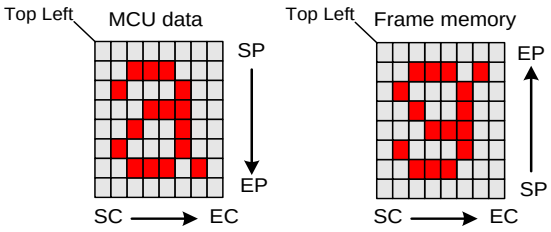
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.

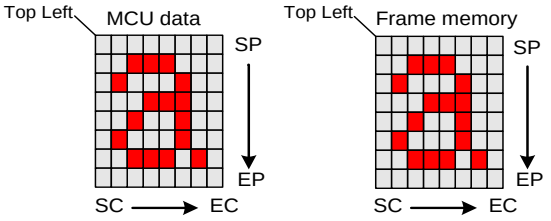
MY (Page Address Order)="0"



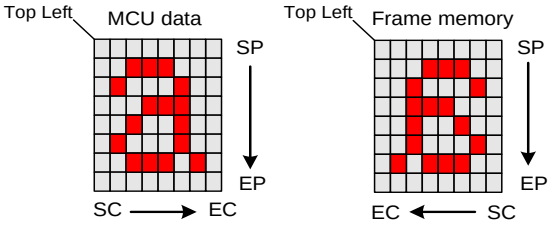
MY (Page Address Order)="1"



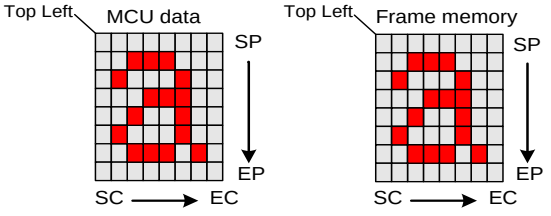
MX (Column Address Order)="0"



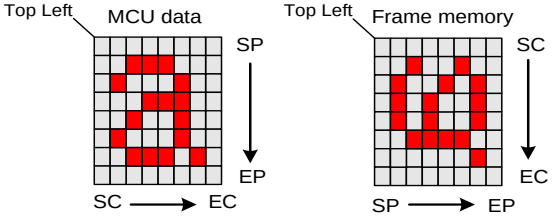
MX (Column Address Order)="1"



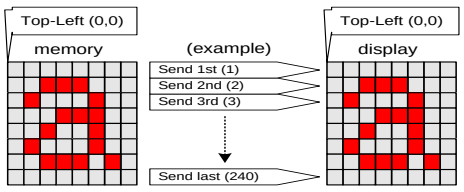
MV (Vertical Refresh Order bit)="0"



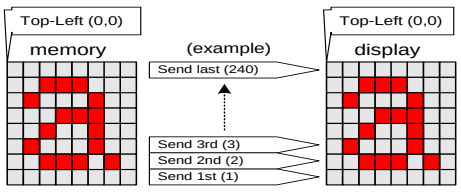
MV (Vertical Refresh Order bit)="1"

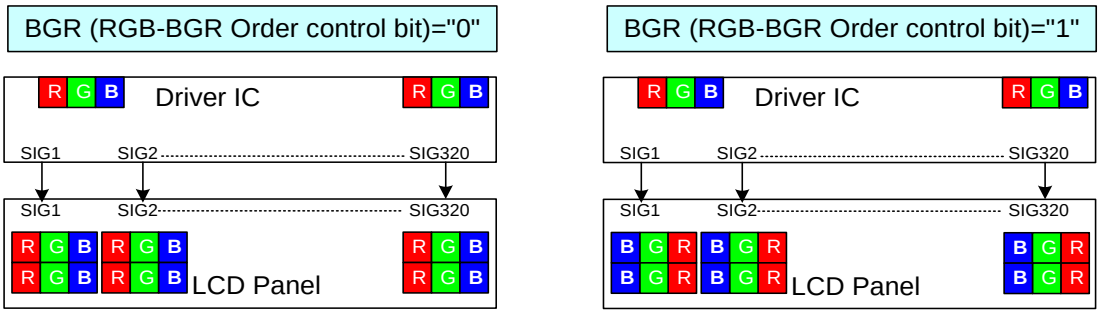


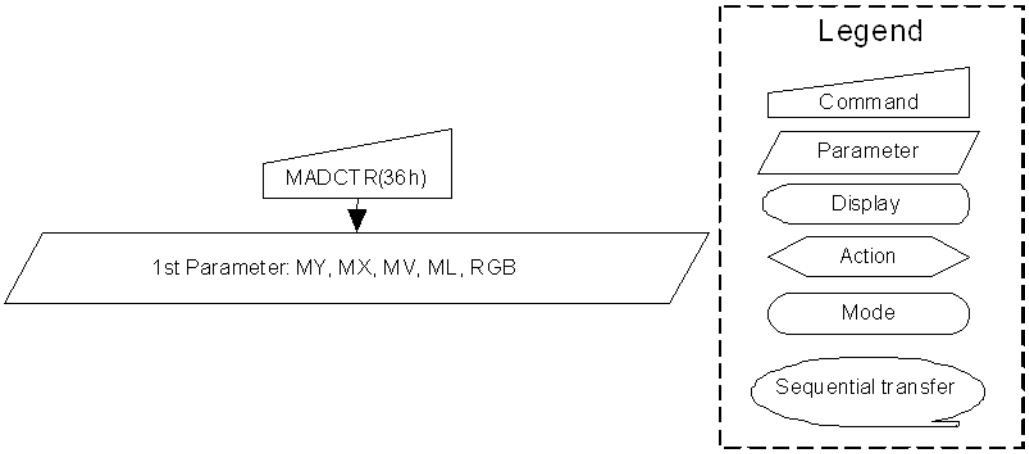
ML (Vertical refresh order bit)="0"



ML (Vertical refresh order bit)="1"



<table>
<tr><td></td><td>


Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8'h00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>8'h00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

5.2.29. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	0	0	0	0	0	0	0	VSP[8]	00
2nd Parameter	1	1	↑	VSP [7:0]								00

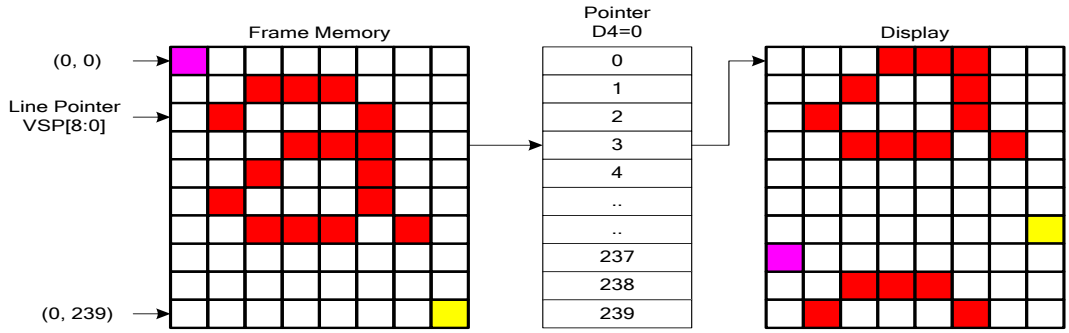
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below :-

When MADCTL D4=0

Example:

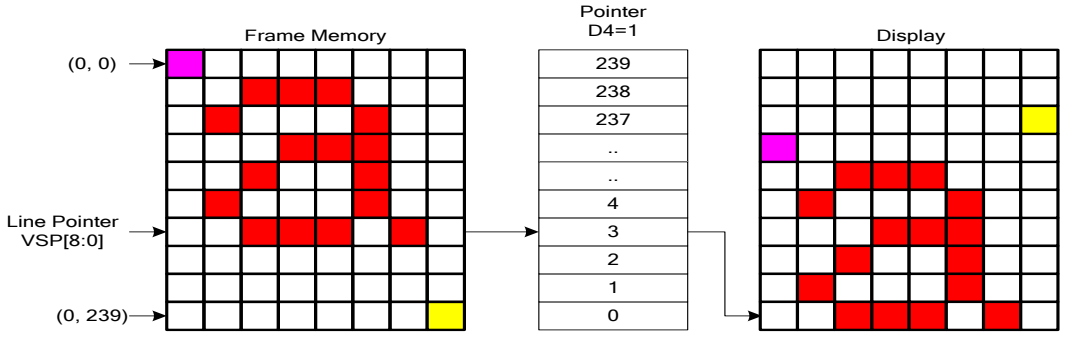
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP='3'.



When MADCTL D4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9342E enters Partial mode.

Restriction

<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [8:0]</th></tr>
<tr><td>Power On Sequence</td><td>9'h000h</td></tr>
<tr><td>SW Reset</td><td>9'h000h</td></tr>
<tr><td>HW Reset</td><td>9'h000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

5.2.30. Idle Mode OFF (38h)

38h	IDMOFF (Idle Mode OFF)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	0	38h
Parameter	No Parameter											
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors.											
Restriction	This command has no effect when module is already in idle off mode.											

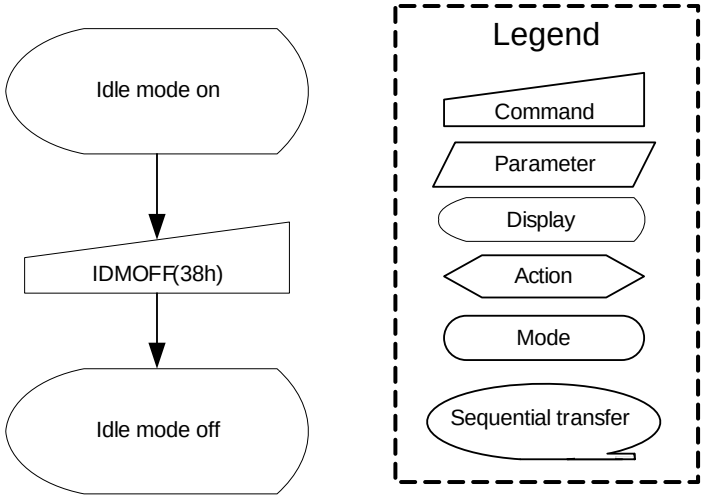
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



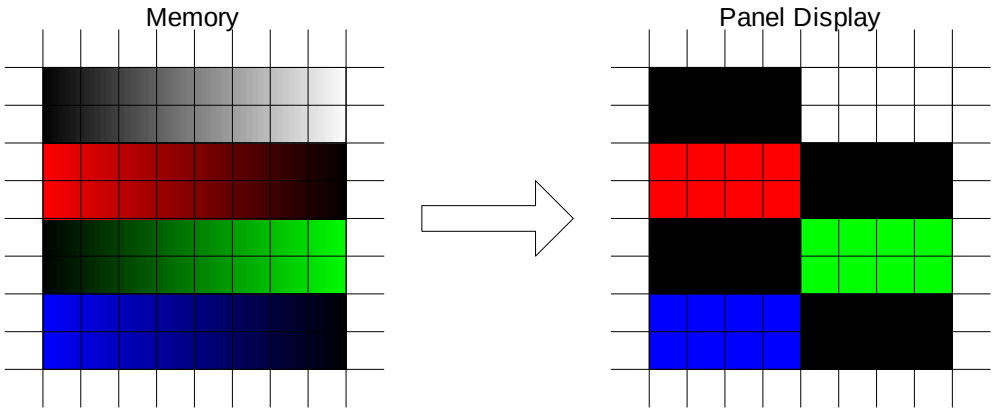
5.2.31. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter											

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Color			
	R_5 R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_5 B_4 B_3 B_2 B_1 B_0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

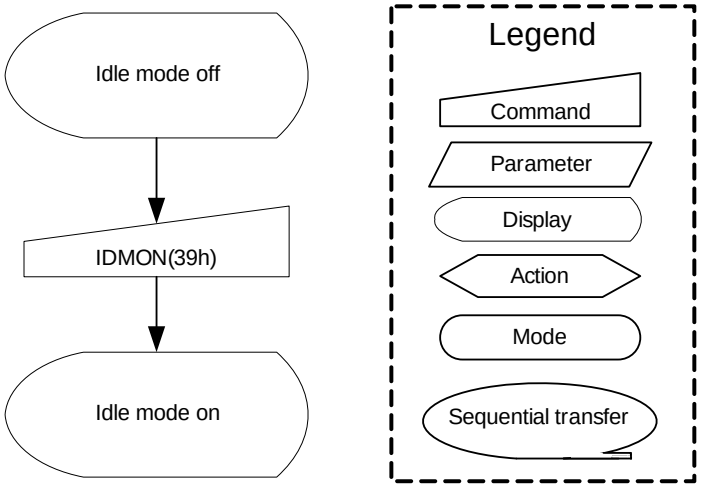
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart	

5.2.32. COLMOD: Pixel Format Set (3Ah)

3Ah	PIXSET (Pixel Format Set)											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	1	0	3Ah
Parameter	1	1	↑	0	DPI [2:0]			0	DBI [2:0]			66

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	24 bits / pixel

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

If using RGB Interface must selection serial interface.

Restriction

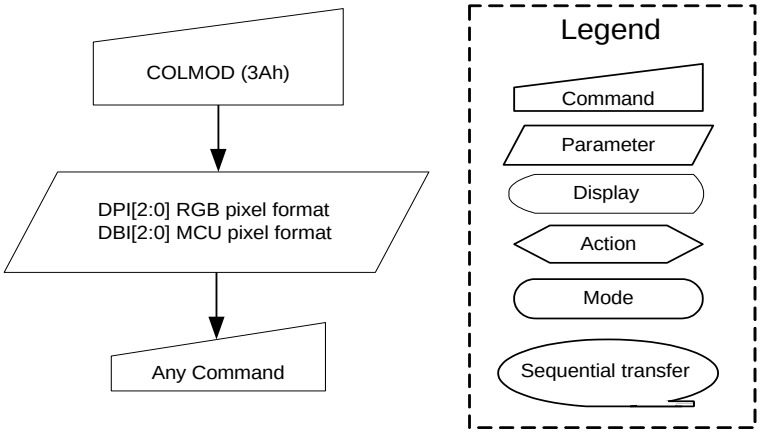
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b110	3'b110
SW Reset	No Change	No Change
HW Reset	3'b110	3'b110

Flow Chart



5.2.33. Memory Write Continue (3Ch)

3Ch	RAMWRC (Memory Write Continue)												
W	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	D1[17:0]									XX
:	1	1	↑	Dx[17:0]									XX
Nth Parameter	1	1	↑	Dn[17:0]									XX

Description

This command is used to transfer data from the MPU to the frame memory if the frame memory wants to continue memory write after the "Memory Write (2Ch)" command. This command makes no change to the other status of the driver.

When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions after it is done on the "Memory Write (2Ch)" command.

Then D [17:0] is stored in the frame memory and the column register and the page register are incremented, as the table below : Column and Page Counter Control.

Condition	Column counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is large than "End Column"	Return to "Start Column"	Increment by 1
The Page counter value is large than "End Page"	Return to "Start Column"	Return to "Start Page"

Sending any other command can stop the Memory Write Continue command.

X = void

Restriction

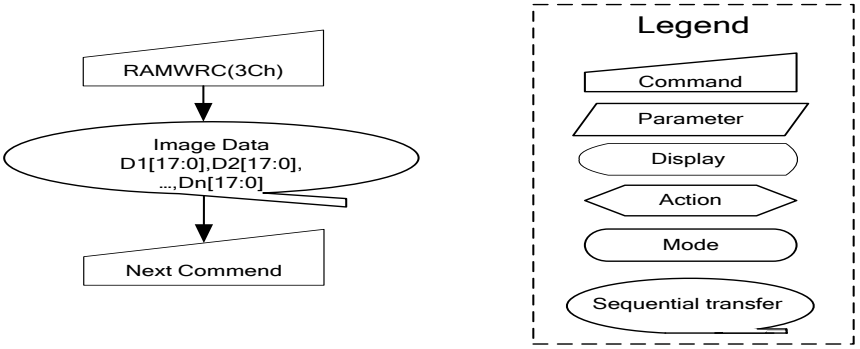
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart



5.2.34. Memory Read Continue (3Eh)

3Eh	RAMWRC (Memory Read Continue)												
R	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	D1[17:0]									XX
:	1	↑	1	Dx[17:0]									XX
(N+1)th Parameter	1	↑	1	Dn[17:0]									XX

Description

This command is used to transfer data from the Frame Memory to the MPU, if the MPU wants to continue memory read after "Memory Read (2Eh)" command. This command makes no change to the other status of the driver.

When this command is accepted, the column register and the page register will not reset to the Start Column/Start Page positions since it is done on the "Memory Read (2Eh)" command.

Then D [17:0] is read back from the frame memory, and the column register and the page register are incremented, as the table below : Column and Page Counter Control.

Condition	Column counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is large than "End Column"	Return to "Start Column"	Increment by 1
The Page counter value is large than "End Page"	Return to "Start Column"	Return to "Start Page"

Sending any other command can stop the Memory Read Continue command.

X = void.

Restriction

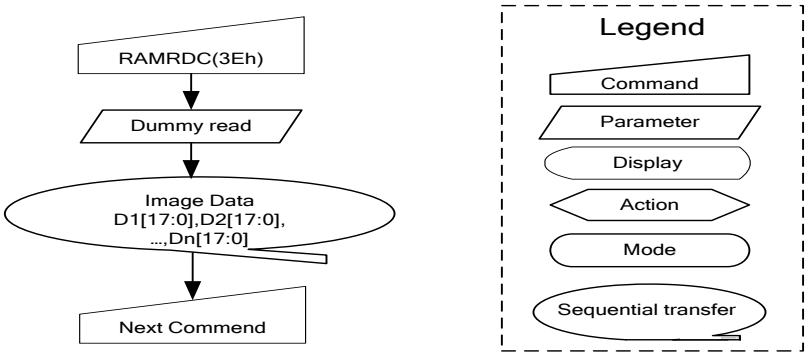
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart

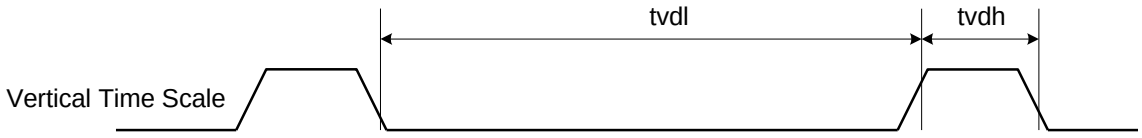


5.2.35. Set_Tear_Scanline (44h)

44h	Set_Tear_Scanline											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	0	0	0	0	0	0	0	STS[8]	00
2nd Parameter	1	1	↑	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



Note that set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

-

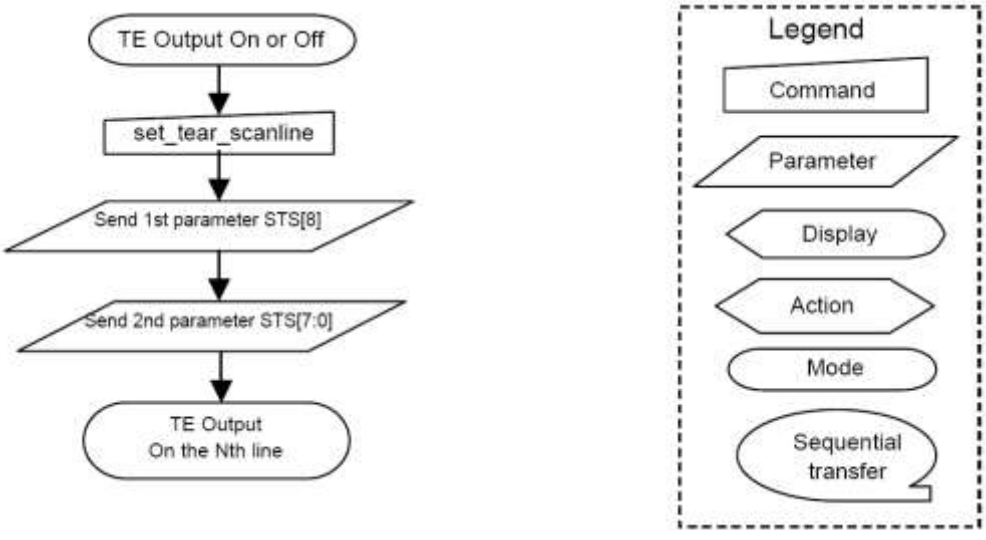
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS [8:0]=000h
SW Reset	STS [8:0]=000h
HW Reset	STS [8:0]=000h

Flow Chart



5.2.36. Get_Scanline (45h)

45h	Get_Scanline											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	0	0	0	0	0	0	0	GTS[8]	00
3rd Parameter	1	↑	1	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	00

Description

The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.

When in Sleep Mode, the value returned by get_scanline is undefined.

Restriction

-

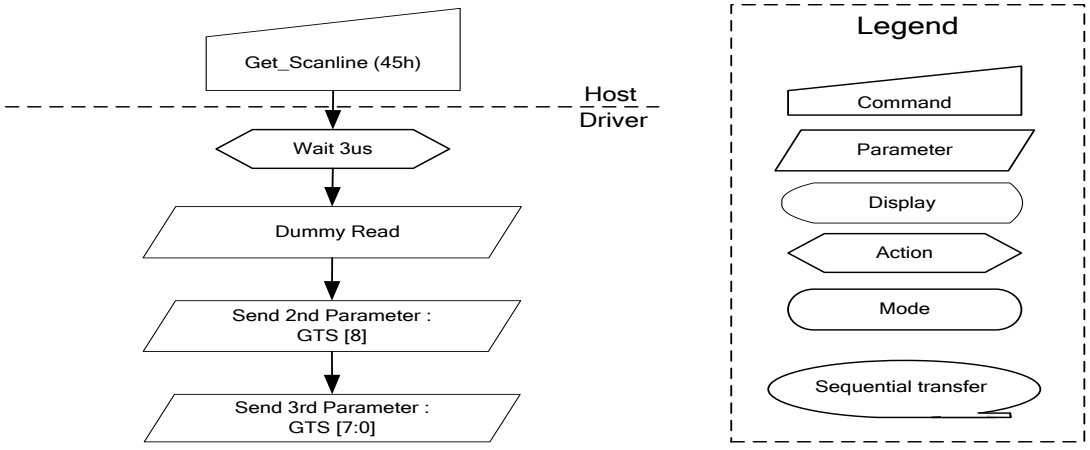
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GTS [8:0]
Pow er On Sequence	GTS [8:0]=000h
SW Reset	GTS [8:0]=000h
HW Reset	GTS [8:0]=000h

Flow Chart



5.2.37. Write Display Brightness (51h)

51h	WRDISBV (Write Display Brightness)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	0	1	51h
Parameter	1	1	↑	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.											
Restriction	None											

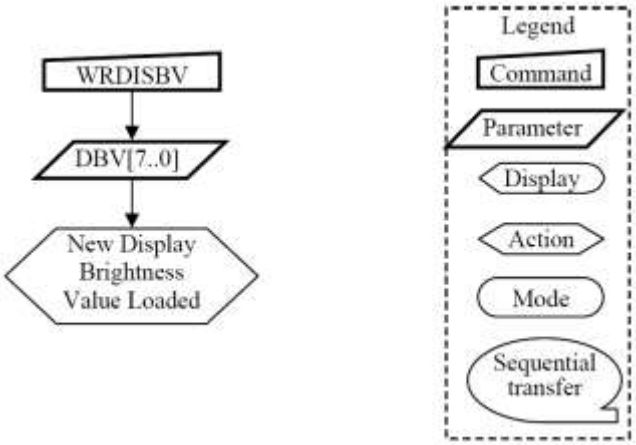
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DBV [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



5.2.38. Read Display Brightness (52h)

52h	RDDISBV (Read Display Brightness Value)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	0	52h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

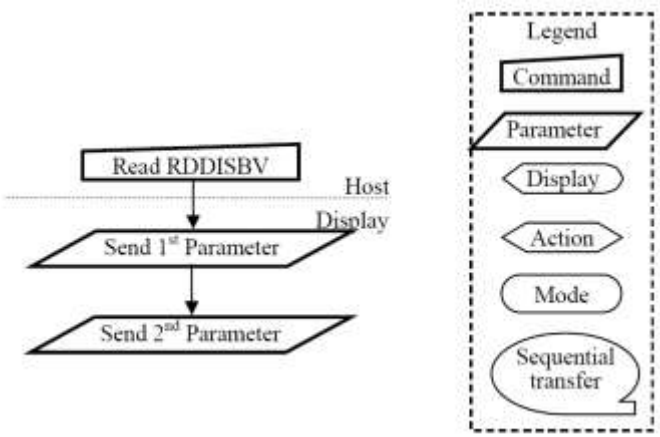
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DBV [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



5.2.39. Write CTRL Display (53h)

53h	WRCTRLD (Write Control Display)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	0	1	1	53h
Parameter	1	1	↑	0	0	BCTRL	0	DD	BL	0	0	00

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off (Brightness registers are 00h, DBV[7..0])

1 = On (Brightness registers are active, according to the other parameters.)

DD: Display Dimming, only for manual brightness setting

DD = 0: Display Dimming is off

DD = 1: Display Dimming is on

BL: Backlight Control On/Off

0 = Off (Completely turn off backlight circuit. Control lines must be low.)

1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1→ 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

Restriction

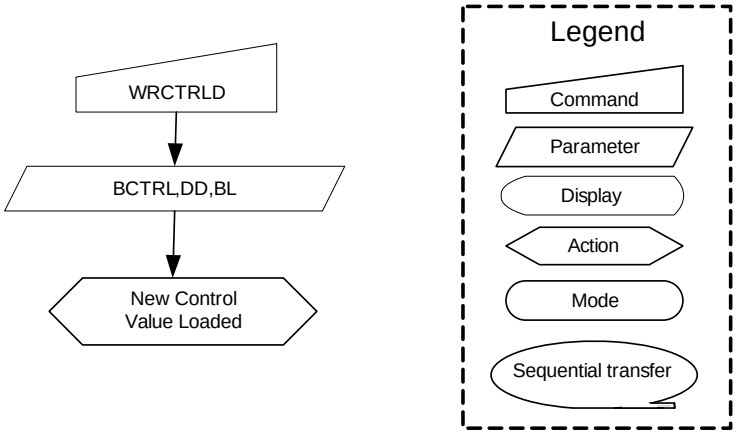
None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	

5.2.40. Read CTRL Display (54h)

54h	RDCTRLD (Read Control Display)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	0	54h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	0	0	BCTRL	0	DD	BL	0	0	00

Description

This command is used to return brightness setting.

BCTRL: Brightness Control Block On/Off,

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)

DD: Display Dimming

'0' = Display Dimming is off

'1' = Display Dimming is on

BL: Backlight On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low.)

'1' = On

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

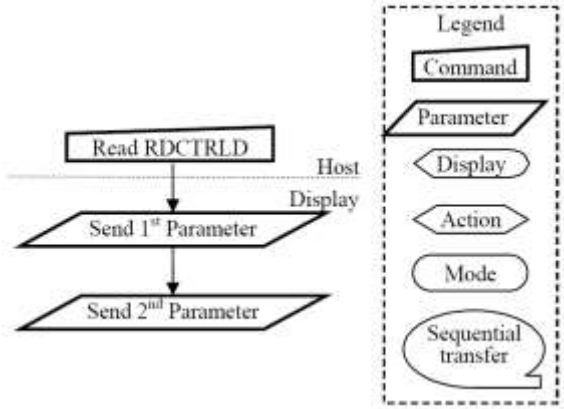
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	

5.2.41. Write Content Adaptive Brightness Control (55h)

55h	WRCABC (Write Content Adaptive Brightness Control)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	0	1	55h
Parameter	1	1	↑	0	0	0	0	0	0	C [1]	C [0]	00

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, w hich are defined on a table below .

C [1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

None

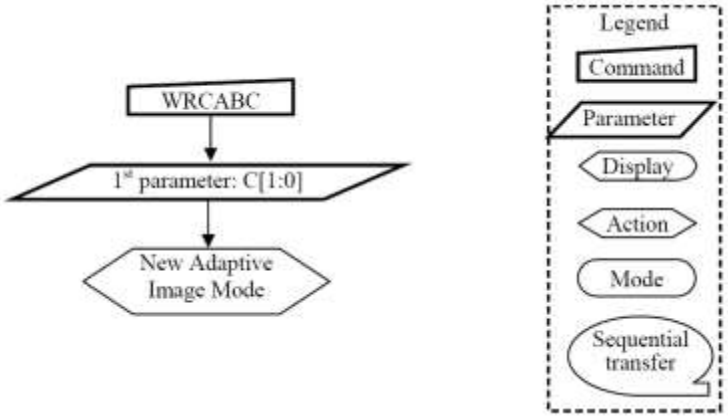
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Pow er On Sequence	C [1:0]=00h
SW Reset	C [1:0]=00h
HW Reset	C [1:0]=00h

Flow Chart



5.2.42. Read Content Adaptive Brightness Control (56h)

56h	RDCABC (Read Content Adaptive Brightness Control)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	0	1	1	0	56h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	0	0	0	0	0	0	C[1]	C[0]	00

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C [1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

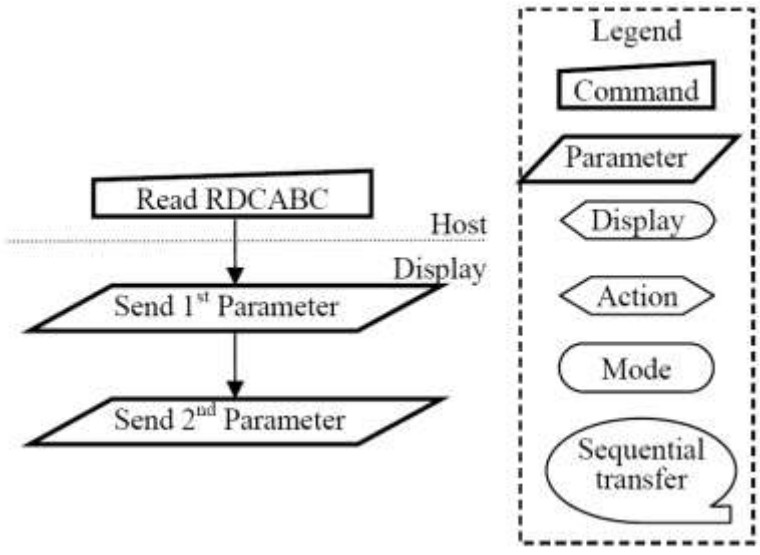
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C [1:0]=00h
SW Reset	C [1:0]=00h
HW Reset	C [1:0]=00h

Flow Chart



5.2.43. Write CABC Minimum Brightness (5Eh)

<table>
<tr><th>5Eh</th><th colspan="12">Write CABC Minimum Brightness</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>5Eh</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>CMB[7]</td><td>CMB[6]</td><td>CMB[5]</td><td>CMB[4]</td><td>CMB[3]</td><td>CMB[2]</td><td>CMB[1]</td><td>CMB[0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set the minimum brightness value of the display for CABC function.
CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.
When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed.
This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.
When display brightness is turned off (BCTRL=0 of “Write CTRL Display (53h)”), CABC minimum brightness setting is ignored.
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>CMB [7:0]</th></tr><tr><td>Power On Sequence</td><td>8’h00h</td></tr><tr><td>SW Reset</td><td>8’h00h</td></tr><tr><td>HW Reset</td><td>8’h00h</td></tr></table></td></tr>
</table>

5.2.44. Read CABC Minimum Brightness (5Fh)

5Fh	Read CABC Minimum Brightness											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	0	1	1	1	1	1	5Fh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00

Description

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CMB [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

5.2.45. Read Automatic Brightness Control Self-Diagnostic Result (68h)

68h	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	1	1	0	1	0	0	0	68h
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading w ork properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

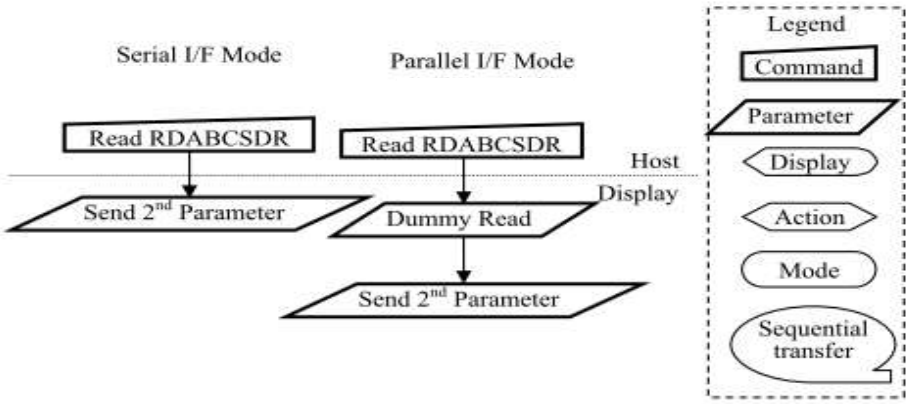
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Pow er On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



5.2.46. Read ID1 (DAh)

DAh	RDID1 (Read ID1)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	ID1 [7:0]								E3

Description

This read byte identifies the LCD module's manufacturer ID and it is specified by User

The 1st parameter is dummy data.

The 2nd parameter is LCD module's manufacturer ID.

Restriction

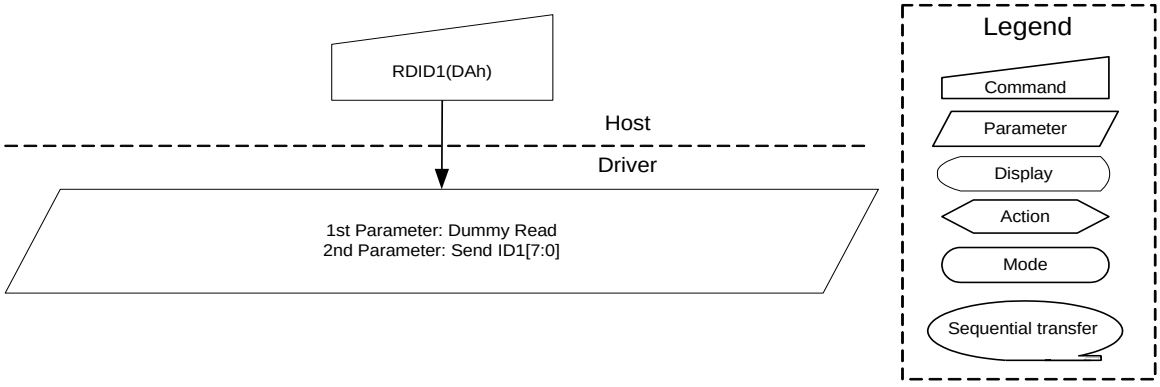
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



5.2.47. Read ID2 (DBh)

DBh	RDID2 (Read ID2)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	ID2 [7:0]								00

Description

This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.

The 1st parameter is dummy data.

The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.

The ID2 can be programmed by MTP function.

Restriction

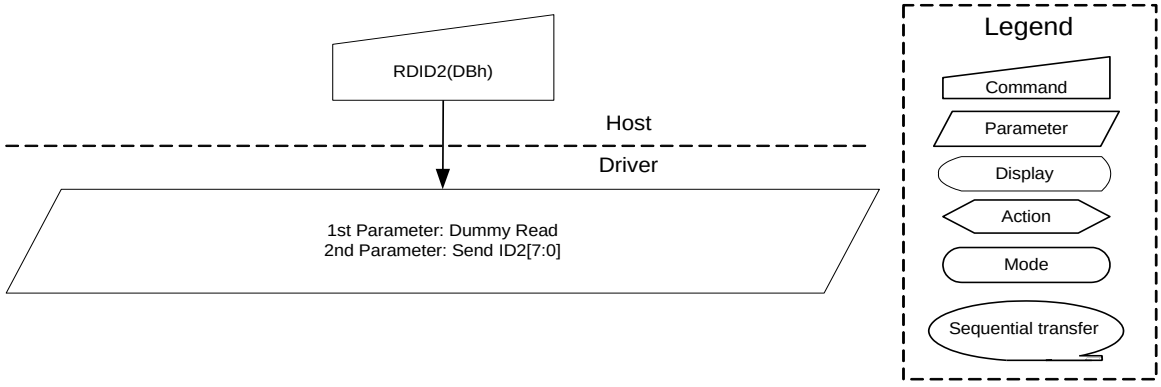
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h80h	MTP value
SW Reset	8'h80h	MTP value
HW Reset	8'h80h	MTP value

Flow Chart



5.2.48. Read ID3 (DCh)

DCh	RDID3 (Read ID3)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	ID3 [7:0]								00

Description

This read byte identifies the LCD module/driver and It is specified by User.

The 1st parameter is dummy data.

The 2nd parameter is LCD module/driver ID.

The ID3 can be programmed by MTP function.

Restriction

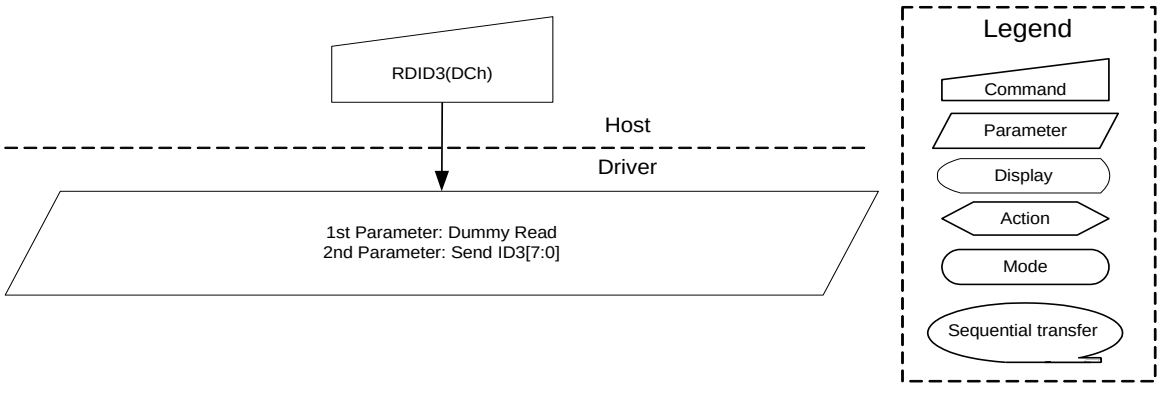
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



5.3. Description of Level 2 Command

5.3.1. Frame Rate Control (B0h)

B0h	Frame Rate Control											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	0	0	B0h
1st Parameter	1	1	↑	RTNA [8]	0	0	0	0	0	0	0	80
2nd Parameter	1	1	↑	RTNA[7:0]								04
3rd Parameter	1	1	↑	RTNB [8]	0	0	0	0	0	0	0	80
4th Parameter	1	1	↑	RTNB[7:0]								04
5th Parameter	1	1	↑	RTNC [8]	0	0	0	0	0	0	0	80
6th Parameter	1	1	↑	RTNC[7:0]								04
7th Parameter	1	1	↑	TE_1M[7:0]								10

Description

RTNA[8:0]：

Set the 1H(line) period in normal mode at MCU interface (RTNA Max=260, min=174 , Unit：op_clk).

RTNB[8:0]：

Set the 1H(line) period in idle mode at MCU interface (RTNB Max=260, min=174 , Unit：op_clk).

RTNC[8:0]：

Set the 1H(line) period in Partial mode at MCU interface (RTNC Max=260, min=174 , Unit：op_clk).

TE_1M[7:0]：It is used to limit the time(line number) in the vertical porch because the TE signal shall be greater than 1ms in the Nokia specification.

The formula to calculate the frame rate is as below

$$\text{Frame Rate} = \frac{4\text{MHz}}{\text{RTN} \times \text{Division Ratio} \times (\text{Line Number} + \text{Max}\{\text{VBP}+\text{VFP}, \text{TE\_1M}\})}$$

Note：1. VBP+VFP must be greater than 1ms. (VBP+VFP ≥ 1ms timing). 2. Division Ratio = 1

whose 1/op_clk is the internal operation frequency

For example, if

1/op_clk = fosc/4 = 16MHz/4 = 4MHz

RTN = 260 (set RTN[8]=1h , RTN[7:0]=04h)

Division Ratio = 1 (set DIV[1:0]=01h)

VBP = VFP = 2

TE_1M = 16 (set TE_1M[7:0]=10h)

Line Number = 240

	Then $\text{Frame Rate} = \frac{4\text{MHz}}{260 \times 1 \times (240 + \text{Max}\{2+2, 16\})} = 60.10\text{Hz}$
Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.2. Display Inversion Control (B1h)

B1h	Display Inversion Control											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	0	0	DINVA[1:0]		0	0	DINVB[1:0]		00

Description

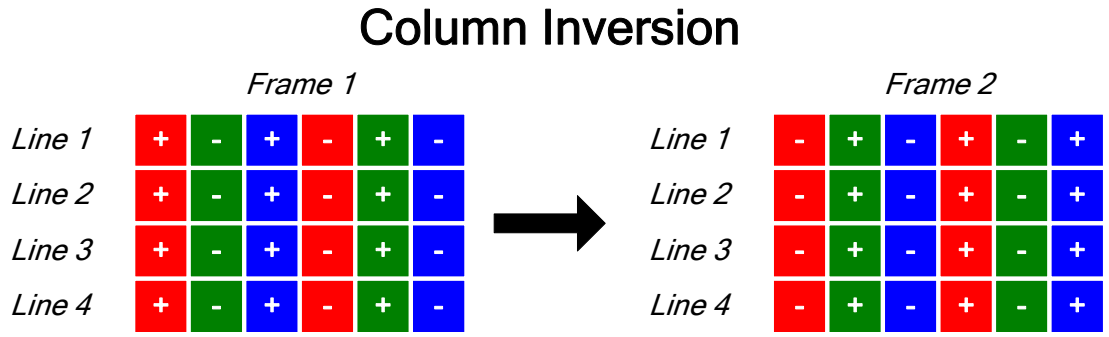
DINVA[1:0]:

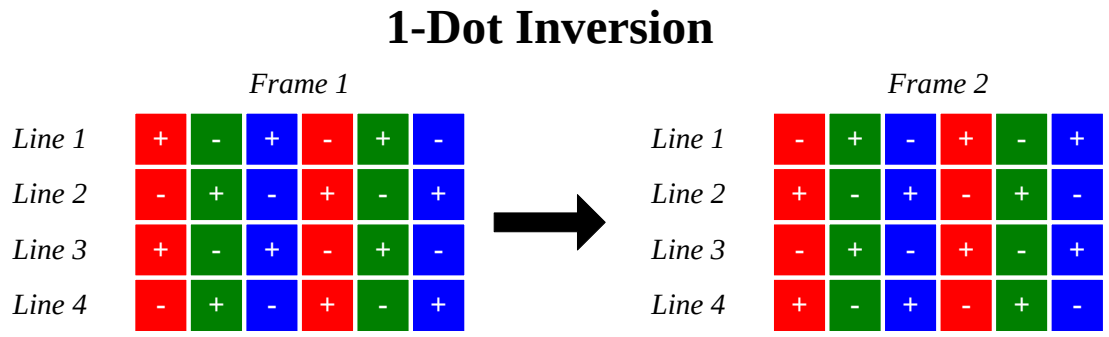
Panel inversion mode setting in the normal mode or in the partial mode.

DINVB[1:0]:

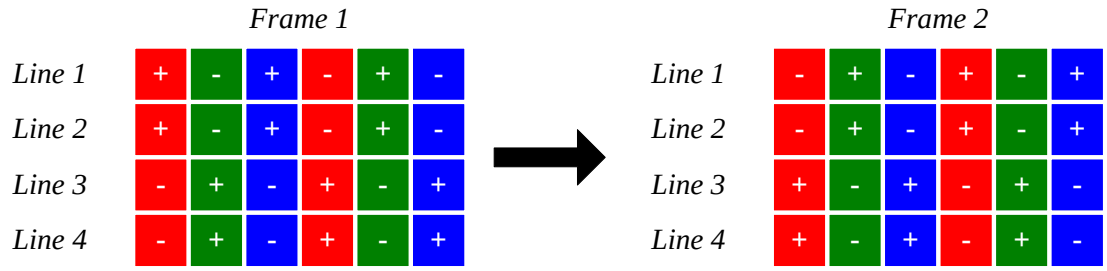
Panel inversion mode setting in the idle mode.

DINVA[1:0]/DINVB[1:0]	Inversion mode
2'b00	Column inversion
2'b01	1-dot inversion
2'b10	2-dot inversion
2'b11	4-dot inversion

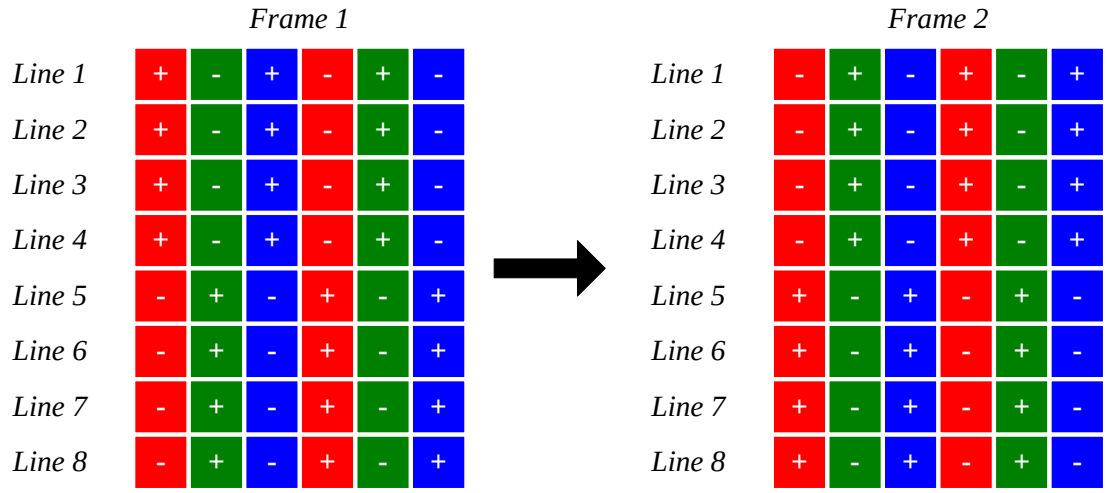




2-Dot Inversion



4-Dot Inversion



Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.3. Source Chopper Control (B7h)

RB7h	Source Chopper Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
1st Parameter	1	1	↑	XX	0	1	0	1	1	0	1	0	5A
2nd Parameter	1	1	↑	XX	0	1	0	0	0	0	0	1	41
3rd Parameter	1	1	↑	XX	0	0	0	1	0	0	0	1	11
4th Parameter	1	1	↑	XX	0	0	0	LINE_CHOP_SHIFT_EN	FRAME_CHOPPER_OPT[1:0]		LINE_CHOPPER_OPT[1:0]		1A
5th Parameter	1	1	↑	XX	0	0	0	0	CHOPPER_OPT	0	0	0	00

Description

LINE_CHOP_SHIFT_EN：

Shift the chopper by 1 line, and it will be (1+N) line chopper eventually.

FRAME_CHOPPER_OPT[1:0]：

Set the chopper change cycle of the source OP by frames.

FRAME_CHOPPER_OPT[1:0]	Function
2'b00	Disable frame chopper (whose stop level depends on CHOPPER_OPT)
2'b01	1 frame
2'b10	2 frame
2'b11	4 frame

LINE_CHOPPER_OPT[1:0]：

Set the chopper change cycle of the source OP by lines.

{LINE_CHOP_SHIFT_EN, LINE_CHOPPER_OPT[1:0]}	Function
3'b000	Disable line chopper
3'b001	1 line
3'b010	2 line
3'b011	4 line
3'b100	Disable line chopper
3'b101	(1+1) line
3'b110	(1+2) line
3'b111	(1+4) line

CHOPPER_OPT：

Set the chopper stop level of source chopper.

CHOPPER_OPT	Function
1'b0	Keep LOW
1'b1	Keep HIGH

Restriction: Access when Command 2 enable = 1

5.3.4. Gate Control (B8h)

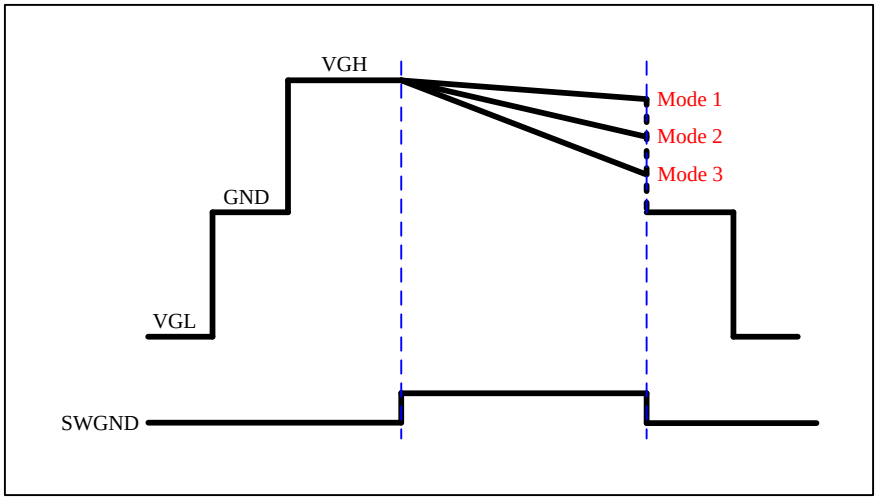
RB8h	Gate Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
1st Parameter	1	1	↑	XX	0	0	0	1	0	0	0	1	11
2nd Parameter	1	1	↑	XX	0	0	1	1	1	0	gsw_mode[1:0]		3B

Description

gsw_mode[1:0] :

Slew to GND select.

gsw_mode[1:0]	Description
2'b00	SWGND Mode 1
2'b01	SWGND Mode 2
2'b10	SWGND Mode 3
2'b11	Disable



Restriction	Access when Command 2 enable = 1

5.3.5. Pump Frequency Selection (BAh)

BAh	Pump Frequency Selection												
W/R	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
1st Parameter	1	1	↑	XX	1	0	vgl_clk_ fast_a[1:0]		1	0	vgh_clk_ fast_a[1:0]		99
2nd Parameter	1	1	↑	XX	0	1	vsnac_clk_ fast_a[1:0]		0	1	vspac_clk_ fast_a[1:0]		55
3rd Parameter	1	1	↑	XX	0	1	vsndc_clk_ fast_a[1:0]		0	1	vspdc_clk_ fast_a[1:0]		55
4th Parameter	1	1	↑	XX	1	0	0	0	1	1	0	0	8C
5th Parameter	1	1	↑	XX	1	0	vgl_clk_ fast_b[1:0]		1	0	vgh_clk_ fast_b[1:0]		99
6th Parameter	1	1	↑	XX	0	1	vsnac_clk_ fast_b[1:0]		0	1	vspac_clk_ fast_b[1:0]		55
7th Parameter	1	1	↑	XX	0	1	vsndc_clk_ fast_b[1:0]		0	1	vspdc_clk_ fast_b[1:0]		55
8th Parameter	1	1	↑	XX	0	0	0	0	1	1	0	0	0C
9th Parameter	1	1	↑	XX	1	0	vgl_clk_ fast_c[1:0]		1	0	vgh_clk_ fast_c[1:0]		99
10th Parameter	1	1	↑	XX	0	1	vsnac_clk_ fast_c[1:0]		0	1	vspac_clk_ fast_c[1:0]		55
11th Parameter	1	1	↑	XX	0	1	vsndc_clk_ fast_c[1:0]		0	1	vspdc_clk_ fast_c[1:0]		55

Description

vgl_clk_fast_a[1:0] / vgl_clk_fast_b[1:0] / vgl_clk_fast_c[1:0] :

VGL pumping clock period in Normal / Idle / Partial displaymode.

(a : Normal , b : Idle , c : Partial)

vgl_clk_fast_a[1:0] vgl_clk_fast_b[1:0] vgl_clk_fast_c[1:0]	Description
2'b00	2.00M Hz
2'b01	2.66M Hz
2'b10	4.00M Hz
2'b11	5.33M Hz

vgh_clk_fast_a[1:0] / vgh_clk_fast_b[1:0] / vgh_clk_fast_c[1:0] :

VGH pumping clock period in Normal / Idle / Partial displaymode.

(a : Normal , b : Idle , c : Partial)

vgh_clk_fast_a[1:0] vgh_clk_fast_b[1:0] vgh_clk_fast_c[1:0]	Description
2'b00	2.00M Hz
2'b01	2.66M Hz
2'b10	4.00M Hz
2'b11	5.33M Hz

vsnac_clk_fast_a[1:0] / vsnac_clk_fast_b[1:0] / vsnac_clk_fast_c[1:0] :

VSNAC pumping clock period in Normal / Idle / Partial displaymode.

(a : Normal , b : Idle , c : Partial)

vsnac_clk_fast_a[1:0] vsnac_clk_fast_b[1:0] vsnac_clk_fast_c[1:0]	Description
2'b00	1.33M Hz
2'b01	2.00M Hz
2'b10	2.66M Hz
2'b11	4.00M Hz

vspac_clk_fast_a[1:0] / vspac_clk_fast_b[1:0] / vspac_clk_fast_c[1:0] :

VSPAC pumping clock period in Normal / Idle / Partial display mode.

(a : Normal , b : Idle , c : Partial)

vspac_clk_fast_a[1:0] vspac_clk_fast_b[1:0] vspac_clk_fast_c[1:0]	Description
2'b00	1.33M Hz
2'b01	2.00M Hz
2'b10	2.66M Hz
2'b11	4.00M Hz

vsndc_clk_fast_a[1:0] / vsndc_clk_fast_b[1:0] / vsndc_clk_fast_c[1:0] :

VSNDC pumping clock period in Normal / Idle / Partial display mode.

(a : Normal , b : Idle , c : Partial)

vsndc_clk_fast_a[1:0] vsndc_clk_fast_b[1:0] vsndc_clk_fast_c[1:0]	Description
2'b00	1.33M Hz
2'b01	2.00M Hz
2'b10	2.66M Hz
2'b11	4.00M Hz

vspdc_clk_fast_a[1:0] / vspdc_clk_fast_b[1:0] / vspdc_clk_fast_c[1:0] :

VSPDC pumping clock period in Normal / Idle / Partial display mode.

(a : Normal , b : Idle , c : Partial)

vspdc_clk_fast_a[1:0] vspdc_clk_fast_b[1:0] vspdc_clk_fast_c[1:0]	Description
2'b00	1.33M Hz
2'b01	2.00M Hz
2'b10	2.66M Hz
2'b11	4.00M Hz

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.6. Power Control 1(C2h)

C2h	Power Control 1											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	0	C2
1st Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
2nd Parameter	1	1	↑	0	1	1	0	0	1	0	0	64
3rd Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
4th Parameter	1	1	↑	VGL_SEL[3:0]				VGH_SEL[3:0]				89
5th Parameter	1	1	↑	0	0	1	1	1	1	0	0	3C
6th Parameter	1	1	↑	0	0	0	0	0	VSP_DC_SEL[2:0]			03
7th Parameter	1	1	↑	0	0	0	0	0	VSP_AC_SEL[2:0]			03
8th Parameter	1	1	↑	0	0	0	0	0	VSN_DC_SEL[2:0]			03
9th Parameter	1	1	↑	0	0	0	0	0	VSN_AC_SEL[2:0]			03
10th Parameter	1	1	↑	0	0	0	0	0	VDDN_SEL[2:0]			02

Description

VGH_SEL[3:0]：

Setting VGH voltage.

VGH_SEL[3:0]	VGH Voltage(V)
0000	10.5
0001	11.0
0010	11.5
0011	12.0
0100	12.5
0101	13.0
0110	13.5
0111	14.0
1000	14.5
1001	15.0(default)
1010	15.5
1011	16.0
1100	16.5
1101	17.0
1110	17.5
1111	18.0

VGL_SEL[3:0]：

Setting VGL voltage.

VGL_SEL[3:0]	VGL Voltage(V)
0000	-6.0
0001	-6.5
0010	-7.0
0011	-7.5
0100	-8.0
0101	-8.5
0110	-9.0
0111	-9.5

1000	-10.0(default)
1001	-10.5
other	reserve

VSP_DC_SEL[2:0] :

Setting VSP_DC voltage.

VSP_DC_SEL[2:0]	VSP_DC Voltage(V)
001	6.2
010	6.3
011	6.4(default)
100	6.5
101	6.6
110	6.7
other	reserve

VSP_AC_SEL[2:0] :

Setting VSP_AC voltage.

VSP_AC_SEL[2:0]	VSP_AC Voltage(V)
001	6.2
010	6.3
011	6.4(default)
100	6.5
101	6.6
110	6.7
other	reserve

VSN_DC_SEL[2:0] :

Setting VSN_DC voltage.

VSN_DC_SEL[2:0]	VSN_DC Voltage(V)
001	-4.4
010	-4.5
011	-4.6(default)
100	-4.7
101	-4.8
110	-4.9
other	reserve

VSN_AC_SEL[2:0] :

Setting VSN_AC voltage.

VSN_AC_SEL[2:0]	VSN_AC Voltage(V)
001	-4.4
010	-4.5
011	-4.6(default)
100	-4.7
101	-4.8
110	-4.9
other	reserve

VDDN_SEL[2:0]：

Setting VDDN voltage.

VDDN_SEL[2:0]	VDDN Voltage(V)
000	1.6
001	1.7
010	1.8
011	1.9
100	2.0
101	2.0(default)
110	2.0
111	2.0

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.7. Power Control 2 (C3h)

C3h	Power Control 2											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	0	0	1	1	C3
1st Parameter	1	1	↑	0	0	0	0	1	1	1	1	0F
2nd Parameter	1	1	↑	0	0	0	1	0	1	1	0	16
3rd Parameter	1	1	↑	0	0	0	0	0	1	1	1	07
4th Parameter	1	1	↑	0	1	1	0	0	1	0	1	65
5th Parameter	1	1	↑	1	1	1	0	1	1	0	0	EC
6th Parameter	1	1	↑	1	1	0	0	1	1	1	1	CF
7th Parameter	1	1	↑	0	0	0	0	0	1	LVD_ VCI_EN	LVD_ IOVCC_ EN	07

Description

LVD_VCI_EN：

VCI Low voltage detection(LVD) control.

LVD_VCI_EN	Description
0	VCI LVD disable
1	VCI LVD enable (default)

LVD_IOVCC_EN：

IOVCC Low voltage detection(LVD) control.

LVD_IOVCC_EN	Description
0	IOVCC LVD disable
1	IOVCC LVD enable (default)

Restriction: Access when EXTC_EN=1 (Set RDDh=01)

5.3.8. Power Control 3 (C8h)

C8h	Power Control 3											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	0	0	C8
1st Parameter	1	1	↑	0	VCOM[6:0]							5A

Description

VCOM[6:0] :

Setting VCOM reference voltage.

VCOM[6:0]	VCOM(V)	VCOM[6:0]	VCOM(V)	VCOM[6:0]	VCOM(V)	VCOM[6:0]	VCOM(V)
00h	0.3	20h	0.7	40h	1.1	60h	1.5
01h	0.3125	21h	0.7125	41h	1.1125	61h	1.5125
02h	0.325	22h	0.725	42h	1.125	62h	1.525
03h	0.3375	23h	0.7375	43h	1.1375	63h	1.5375
04h	0.35	24h	0.75	44h	1.15	64h	1.55
05h	0.3625	25h	0.7625	45h	1.1625	65h	1.5625
06h	0.375	26h	0.775	46h	1.175	66h	1.575
07h	0.3875	27h	0.7875	47h	1.1875	67h	1.5875
08h	0.4	28h	0.8	48h	1.2	68h	1.6
09h	0.4125	29h	0.8125	49h	1.2125	69h	1.6125
0Ah	0.425	2Ah	0.825	4Ah	1.225	6Ah	1.625
0Bh	0.4375	2Bh	0.8375	4Bh	1.2375	6Bh	1.6375
0Ch	0.45	2Ch	0.85	4Ch	1.25	6Ch	1.65
0Dh	0.4625	2Dh	0.8625	4Dh	1.2625	6Dh	1.6625
0Eh	0.475	2Eh	0.875	4Eh	1.275	6Eh	1.675
0Fh	0.4875	2Fh	0.8875	4Fh	1.2875	6Fh	1.6875
10h	0.5	30h	0.9	50h	1.3	70h	1.7
11h	0.5125	31h	0.9125	51h	1.3125	71h	1.7125
12h	0.525	32h	0.925	52h	1.325	72h	1.725
13h	0.5375	33h	0.9375	53h	1.3375	73h	1.7375
14h	0.55	34h	0.95	54h	1.35	74h	1.75
15h	0.5625	35h	0.9625	55h	1.3625	75h	1.7625
16h	0.575	36h	0.975	56h	1.375	76h	1.775
17h	0.5875	37h	0.9875	57h	1.3875	77h	1.7875
18h	0.6	38h	1	58h	1.4	78h	1.8
19h	0.6125	39h	1.0125	59h	1.4125	79h	1.8125
1Ah	0.625	3Ah	1.025	5Ah	1.425	7Ah	1.825
1Bh	0.6375	3Bh	1.0375	5Bh	1.4375	7Bh	1.8375
1Ch	0.65	3Ch	1.05	5Ch	1.45	7Ch	1.85
1Dh	0.6625	3Dh	1.0625	5Dh	1.4625	7Dh	1.8625
1Eh	0.675	3Eh	1.075	5Eh	1.475	7Eh	1.875
1Fh	0.6875	3Fh	1.0875	5Fh	1.4875	7Fh	1.8875

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.9. Power Control 4 (C9h)

C9h	Power Control 4											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	0	1	C9
1st Parameter	1	1	↑	0	0	VRH_DOT[5:0]						13

Description

VRH_DOT[5:0] :

Setting reference voltage for VREG1OUT in Dot inversion (RB1h setting).

VRH_DOT[5:0]	VREG1OUT(V)	VRH_DOT[5:0]	VREG1OUT (V)
00h	3.55+(VCOM+0.5VDV)	15h	4.6+(VCOM+0.5VDV)
01h	3.6+(VCOM+0.5VDV)	16h	4.65+(VCOM+0.5VDV)
02h	3.65+(VCOM+0.5VDV)	17h	4.7+(VCOM+0.5VDV)
03h	3.7+(VCOM+0.5VDV)	18h	4.75+(VCOM+0.5VDV)
04h	3.75+(VCOM+0.5VDV)	19h	4.8+(VCOM+0.5VDV)
05h	3.8+(VCOM+0.5VDV)	1Ah	4.85+(VCOM+0.5VDV)
06h	3.85+(VCOM+0.5VDV)	1Bh	4.9+(VCOM+0.5VDV)
07h	3.9+(VCOM+0.5VDV)	1Ch	4.95+(VCOM+0.5VDV)
08h	3.95+(VCOM+0.5VDV)	1Dh	5+(VCOM+0.5VDV)
09h	4+(VCOM+0.5VDV)	1Eh	5.05+(VCOM+0.5VDV)
0Ah	4.05+(VCOM+0.5VDV)	1Fh	5.1+(VCOM+0.5VDV)
0Bh	4.1+(VCOM+0.5VDV)	20h	5.15+(VCOM+0.5VDV)
0Ch	4.15+(VCOM+0.5VDV)	21h	5.2+(VCOM+0.5VDV)
0Dh	4.2+(VCOM+0.5VDV)	22h	5.25+(VCOM+0.5VDV)
0Eh	4.25+(VCOM+0.5VDV)	23h	5.3+(VCOM+0.5VDV)
0Fh	4.3+(VCOM+0.5VDV)	24h	5.35+(VCOM+0.5VDV)
10h	4.35+(VCOM+0.5VDV)	25h	5.4+(VCOM+0.5VDV)
11h	4.4+(VCOM+0.5VDV)	26h	5.45+(VCOM+0.5VDV)
12h	4.45+(VCOM+0.5VDV)	27h	5.5+(VCOM+0.5VDV)
13h	4.5+(VCOM+0.5VDV)	28h~3Fh	Reserved
14h	4.55+(VCOM+0.5VDV)	--	--

VRH_DOT[5:0] :

Setting reference voltage for VREG2OUT in Dot inversion (RB1h setting).

VRH_DOT[5:0]	VREG2OUT (V)	VRH_DOT[5:0]	VREG2OUT (V)
00h	-3.55+(VCOM-0.5VDV)	15h	-4.6+(VCOM-0.5VDV)
01h	-3.6+(VCOM-0.5VDV)	16h	-4.65+(VCOM-0.5VDV)
02h	-3.65+(VCOM-0.5VDV)	17h	-4.7+(VCOM-0.5VDV)
03h	-3.7+(VCOM-0.5VDV)	18h	-4.75+(VCOM-0.5VDV)
04h	-3.75+(VCOM-0.5VDV)	19h	-4.8+(VCOM-0.5VDV)
05h	-3.8+(VCOM-0.5VDV)	1Ah	-4.85+(VCOM-0.5VDV)
06h	-3.85+(VCOM-0.5VDV)	1Bh	-4.9+(VCOM-0.5VDV)
07h	-3.9+(VCOM-0.5VDV)	1Ch	-4.95+(VCOM-0.5VDV)
08h	-3.95+(VCOM-0.5VDV)	1Dh	-5+(VCOM-0.5VDV)
09h	-4+(VCOM-0.5VDV)	1Eh	-5.05+(VCOM-0.5VDV)

	0Ah	-4.05+(VCOM-0.5VDV)	1Fh	-5.1+(VCOM-0.5VDV)
	0Bh	-4.1+(VCOM-0.5VDV)	20h	-5.15+(VCOM-0.5VDV)
	0Ch	-4.15+(VCOM-0.5VDV)	21h	-5.2+(VCOM-0.5VDV)
	0Dh	-4.2+(VCOM-0.5VDV)	22h	-5.25+(VCOM-0.5VDV)
	0Eh	-4.25+(VCOM-0.5VDV)	23h	-5.3+(VCOM-0.5VDV)
	0Fh	-4.3+(VCOM-0.5VDV)	24h	-5.35+(VCOM-0.5VDV)
	10h	-4.35+(VCOM-0.5VDV)	25h	-5.4+(VCOM-0.5VDV)
	11h	-4.4+(VCOM-0.5VDV)	26h	-5.45+(VCOM-0.5VDV)
	12h	-4.45+(VCOM-0.5VDV)	27h	-5.5+(VCOM-0.5VDV)
	13h	-4.5+(VCOM-0.5VDV)	28h~3Fh	Reserved
	14h	-4.55+(VCOM-0.5VDV)	--	--
Restriction	Access when EXTC_EN=1 (Set RDDh=01)			

5.3.10. Power Control 5 (CAh)

CAh	Power Control 5											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	1	0	CA
1st Parameter	1	1	↑	0	0	VRH_COL[5:0]						13

Description

VRH_COL[5:0] :

Setting reference voltage for VREG1OUT in Column inversion (RB1h setting).

VRH_COL[5:0]	VREG1OUT(V)	VRH_COL[5:0]	VREG1OUT (V)
00h	3.55+(VCOM+0.5VDV)	15h	4.6+(VCOM+0.5VDV)
01h	3.6+(VCOM+0.5VDV)	16h	4.65+(VCOM+0.5VDV)
02h	3.65+(VCOM+0.5VDV)	17h	4.7+(VCOM+0.5VDV)
03h	3.7+(VCOM+0.5VDV)	18h	4.75+(VCOM+0.5VDV)
04h	3.75+(VCOM+0.5VDV)	19h	4.8+(VCOM+0.5VDV)
05h	3.8+(VCOM+0.5VDV)	1Ah	4.85+(VCOM+0.5VDV)
06h	3.85+(VCOM+0.5VDV)	1Bh	4.9+(VCOM+0.5VDV)
07h	3.9+(VCOM+0.5VDV)	1Ch	4.95+(VCOM+0.5VDV)
08h	3.95+(VCOM+0.5VDV)	1Dh	5+(VCOM+0.5VDV)
09h	4+(VCOM+0.5VDV)	1Eh	5.05+(VCOM+0.5VDV)
0Ah	4.05+(VCOM+0.5VDV)	1Fh	5.1+(VCOM+0.5VDV)
0Bh	4.1+(VCOM+0.5VDV)	20h	5.15+(VCOM+0.5VDV)
0Ch	4.15+(VCOM+0.5VDV)	21h	5.2+(VCOM+0.5VDV)
0Dh	4.2+(VCOM+0.5VDV)	22h	5.25+(VCOM+0.5VDV)
0Eh	4.25+(VCOM+0.5VDV)	23h	5.3+(VCOM+0.5VDV)
0Fh	4.3+(VCOM+0.5VDV)	24h	5.35+(VCOM+0.5VDV)
10h	4.35+(VCOM+0.5VDV)	25h	5.4+(VCOM+0.5VDV)
11h	4.4+(VCOM+0.5VDV)	26h	5.45+(VCOM+0.5VDV)
12h	4.45+(VCOM+0.5VDV)	27h	5.5+(VCOM+0.5VDV)
13h	4.5+(VCOM+0.5VDV)	28h~3Fh	Reserved
14h	4.55+(VCOM+0.5VDV)	--	--

VRH_COL[5:0] :

Setting reference voltage for VREG2OUT in Column inversion (RB1h setting).

VRH_COL[5:0]	VREG2OUT (V)	VRH_COL[5:0]	VREG2OUT (V)
00h	-3.55+(VCOM-0.5VDV)	15h	-4.6+(VCOM-0.5VDV)
01h	-3.6+(VCOM-0.5VDV)	16h	-4.65+(VCOM-0.5VDV)
02h	-3.65+(VCOM-0.5VDV)	17h	-4.7+(VCOM-0.5VDV)
03h	-3.7+(VCOM-0.5VDV)	18h	-4.75+(VCOM-0.5VDV)
04h	-3.75+(VCOM-0.5VDV)	19h	-4.8+(VCOM-0.5VDV)
05h	-3.8+(VCOM-0.5VDV)	1Ah	-4.85+(VCOM-0.5VDV)
06h	-3.85+(VCOM-0.5VDV)	1Bh	-4.9+(VCOM-0.5VDV)
07h	-3.9+(VCOM-0.5VDV)	1Ch	-4.95+(VCOM-0.5VDV)
08h	-3.95+(VCOM-0.5VDV)	1Dh	-5+(VCOM-0.5VDV)
09h	-4+(VCOM-0.5VDV)	1Eh	-5.05+(VCOM-0.5VDV)

	0Ah	-4.05+(VCOM-0.5VDV)	1Fh	-5.1+(VCOM-0.5VDV)
	0Bh	-4.1+(VCOM-0.5VDV)	20h	-5.15+(VCOM-0.5VDV)
	0Ch	-4.15+(VCOM-0.5VDV)	21h	-5.2+(VCOM-0.5VDV)
	0Dh	-4.2+(VCOM-0.5VDV)	22h	-5.25+(VCOM-0.5VDV)
	0Eh	-4.25+(VCOM-0.5VDV)	23h	-5.3+(VCOM-0.5VDV)
	0Fh	-4.3+(VCOM-0.5VDV)	24h	-5.35+(VCOM-0.5VDV)
	10h	-4.35+(VCOM-0.5VDV)	25h	-5.4+(VCOM-0.5VDV)
	11h	-4.4+(VCOM-0.5VDV)	26h	-5.45+(VCOM-0.5VDV)
	12h	-4.45+(VCOM-0.5VDV)	27h	-5.5+(VCOM-0.5VDV)
	13h	-4.5+(VCOM-0.5VDV)	28h~3Fh	Reserved
	14h	-4.55+(VCOM-0.5VDV)	--	--
Restriction	Access when EXTC_EN=1 (Set RDDh=01)			

5.3.11. Power Control 6 (CBh)

CBh	Power Control 6											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	1	0	CB
1st Parameter	1	1	↑	0	0	VDV[5:0]						20

Description

VDV[5:0]：

Setting VDV reference voltage.

VDV[5:0]	VDV(V)	VDV[5:0]	VDV(V)	VDV[5:0]	VDV(V)	VDV[5:0]	VDV(V)
00h	-0.8	10h	-0.4	20h	0	30h	0.4
01h	-0.775	11h	-0.375	21h	0.025	31h	0.425
02h	-0.75	12h	-0.35	22h	0.05	32h	0.45
03h	-0.725	13h	-0.325	23h	0.075	33h	0.475
04h	-0.7	14h	-0.3	24h	0.1	34h	0.5
05h	-0.675	15h	-0.275	25h	0.125	35h	0.525
06h	-0.65	16h	-0.25	26h	0.15	36h	0.55
07h	-0.625	17h	-0.225	27h	0.175	37h	0.575
08h	-0.6	18h	-0.2	28h	0.2	38h	0.6
09h	-0.575	19h	-0.175	29h	0.225	39h	0.625
0Ah	-0.55	1Ah	-0.15	2Ah	0.25	3Ah	0.65
0Bh	-0.525	1Bh	-0.125	2Bh	0.275	3Bh	0.675
0Ch	-0.5	1Ch	-0.1	2Ch	0.3	3Ch	0.7
0Dh	-0.475	1Dh	-0.075	2Dh	0.325	3Dh	0.725
0Eh	-0.45	1Eh	-0.05	2Eh	0.35	3Eh	0.75
0Fh	-0.425	1Fh	-0.025	2Fh	0.375	3Fh	0.775

Restriction: Access when EXTC_EN=1 (Set RDDh=01)

5.3.12. RGB Interface Signal Control (D0h)

D0h	RGB Interface Signal Control											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	0	0	0	D0
1st Parameter	1	1	↑	ByPass _MODE	0	RCM[1]	RCM[0]	VSPL	HSPL	DPL	EPL	20

Description

Sets the operation status of the display interface.

The setting becomes effective as soon as the command is received.

EPL:

DE polarity ("0"= High enable for RGB interface, "1"= Low enable for RGB interface)

DPL:

DOTCLK polarity set ("0"= data fetched at the rising time, "1"= data fetched at the falling time)

HSPL:

HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

VSPL:

VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

RCM [1:0]:

RGB interface selection (refer to the RGB interface section).

RCM[1:0]		Description
1	0	DE Mode
1	1	SYNC Mode

ByPass_MODE:

Select display data path whether Memory or Direct to Shift register when RGB Interface is used.

ByPass_MODE	Display Data Path
0	Direct to Shift Register (**default**)
1	Memory

Restriction: Access when EXTC_EN=1 (Set RDDh=01)

5.3.13. Blanking Porch Control (D1h)

D1	TCON Control 11												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	1	D1
1st Parameter	1	1	↑	XX	VFP[7:0]								02
2nd Parameter	1	1	↑	XX	VBP[7:0]								02
3rd Parameter	1	1	↑	XX	0	0	0	0	1	0	1	0	0A
4th Parameter	1	1	↑	XX	HBP[7:0]								14

Description

VFP [7:0] / VBP [7:0]:

The VFP [7:0] and VBP [7:0] bits specify the line number of vertical front and back porch period respectively.

VFP [7:0] VBP [7:0]	Number of VSYNC of front/back porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
00000100	4
00000101	5
00000110	6
00000111	7
00001000	8
00001001	9
00001010	10
00001011	11
00001100	12
00001101	13
: :	: :
00111101	61
00111110	62
00111111	63
: :	: :
11111101	253
11111110	254
11111111	255

HBP [7:0]:

The HBP [7:0] bits specify the line number of horizontal back porch period respectively.

The HBP[7:0] setting only for RGB Sync mode.

HBP [7:0]	Number of HSYNC of back porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
00000100	4
00000101	5
00000110	6
00000111	7
00001000	8

		00001001	9
		00001010	10
		00001011	11
		00001100	12
		00001101	13
		:	:
		00111101	61
		00111110	62
		00111111	63
		:	:
		10110001	177
		10110010	178
		10110011	179
		10110100	180
		10110101	181
		10110110	182
		10110111	Setting prohibited
		10111000	Setting prohibited
		:	:
		11111110	Setting prohibited
		11111111	Setting prohibited
Restriction	Access when Command 2 enable = 1		

5.3.14. Display Function Control (D2h)

D2h	Display Function Control												
W/R	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2
1st Parameter	1	1	↑	XX	0	0	0	0	PTG[1:0]		PT[1:0]		0A
2nd Parameter	1	1	↑	XX	REV	GS	SS	SM	ISC[3:0]				82
3rd Parameter	1	1	↑	XX	0	NL[6:0]							77

Description

PTG [1:0]:

Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area
0	0	Normal scan	Set with the PT [1:0] bits
0	1	Setting prohibited	---
1	0	Interval scan	Set with the PT [1:0] bits
1	1	Setting prohibited	---

PT [1:0]:

Determine source/VCOM output in a non-display area in the partial display mode.

PT [1:0]		Source output on non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS:

This bit controls MCU to memory write/read direction by column address order.

REV:

Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]:

Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan. Then scan cycle is set as odd number from 1~31 frame periods. The polarity is inverted every scan cycle.

ISC [3:0]	Scan Cycle	f_{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms
1000	17 frames	289ms
1001	19 frames	323ms

1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

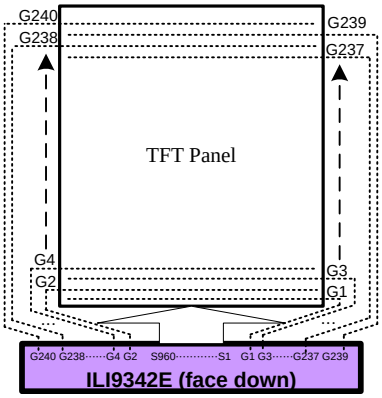
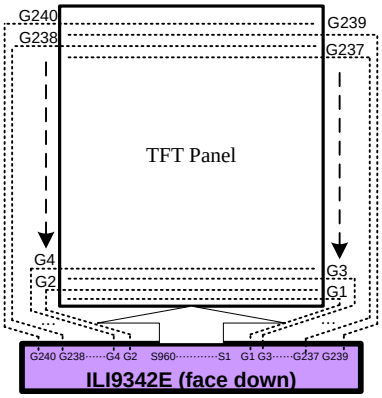
GS:

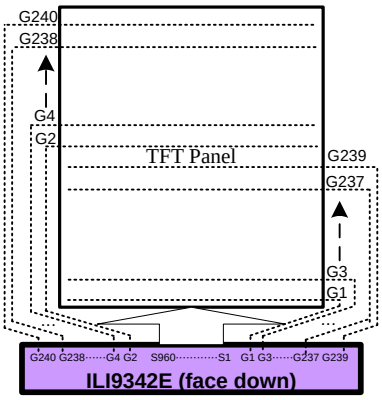
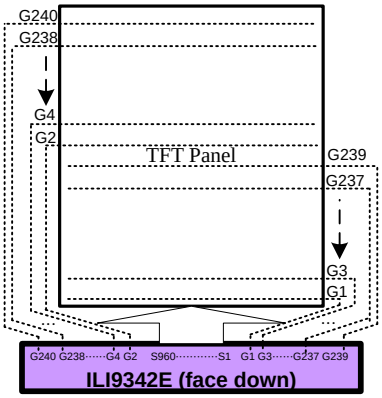
Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1 → G240
1	G240 → G1

SM:

Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G237→G238→G239→G240
0	1		G240→G239->G238→G237→…… …. →G4→G3→G2→G1

1	0		G1→G3→……..→G237→G239→ G2→G4→……→G238→G240
1	1		G240→G238→……..→G4→G2→ G239→G237→……→G3→G1

NL [6:0]:

Sets the number of lines to drive the LCD at an interval of 2 lines. The GRAM address mapping is not affected by the number of lines set by NL [6:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [6:0]	Number of HSYNC of back porch
Others	Setting prohibited
0111111	128 lines
1000000	130 lines
1000001	132 lines
1000010	134 lines
1000011	136 lines
1000100	138 lines
1000101	140 lines
1000110	142 lines
1000111	144 lines
:	:
1110000	226 lines
1110001	228 lines
1110010	230 lines
1110011	232 lines
1110100	234 lines
1110101	236 lines
1110110	238 lines
1110111	240 lines

		Others	Setting prohibited
Restriction	Access when EXTC_EN=1 (Set RDDh=01)		

5.3.15. MADCTL_EOR Control (D5h)

D5h	MADCTL_EOR Control											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	0	1	0	1	D5
1st Parameter	1	1	↑	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	0	0	00

Description

This register can be read/written and OTP programmed, and MADCTL_EOR(RD5h) is exclusive or(EOR) relation with R36h P1 setting.(This register can be programmed 2 times)

MY_EOR :

R36h P1 MY bit	RD5h P1 MY_EOR bit	R36h P1 MY bit actual effect
0	0	0
0	1	1
1	0	1
1	1	0

MX_EOR :

R36h P1 MX bit	RD5h P1 MX_EOR bit	R36h P1 MX bit actual effect
0	0	0
0	1	1
1	0	1
1	1	0

MV_EOR :

R36h P1 MV bit	RD5h P1 MV_EOR bit	R36h P1 MV bit actual effect
0	0	0
0	1	1
1	0	1
1	1	0

ML_EOR :

R36h P1 ML bit	RD5h P1 ML_EOR bit	R36h P1 ML bit actual effect
0	0	0
0	1	1
1	0	1
1	1	0

BGR_EOR :

R36h P1 BGR bit	RD5h P1 BGR_EOR bit	R36h P1 BGR bit actual effect
0	0	0
0	1	1
1	0	1
1	1	0

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.16. Interface Control (D8h)

D8h	Interface Control											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	0	0	D8
1st Parameter	1	1	↑	0	0	EPF[1:0]		0	0	MDT[1:0]		00
2nd Parameter	1	1	↑	0	0	ENDIAN	0	DM[1:0]		RM	RIM	00

Description

MDT [1:0]:

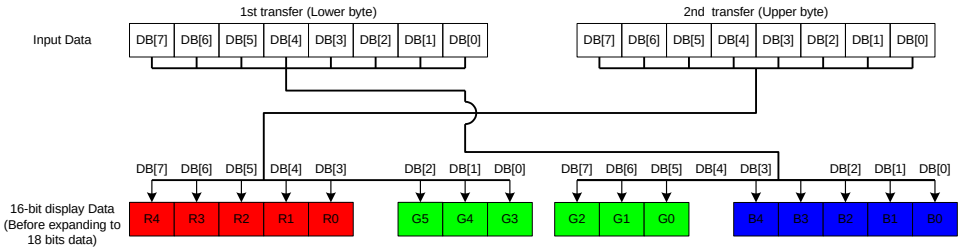
Select the method of display data transferring (MCU system interface).

ENDIAN:

Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transfer Mode
0	Normal (MSB first, default)
1	Little Endian (LSB first)

Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.



DM [1:0]:

Select the display operation mode.

DM [1]	DM [0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface mode
1	1	Setting disabled

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM:

Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM:

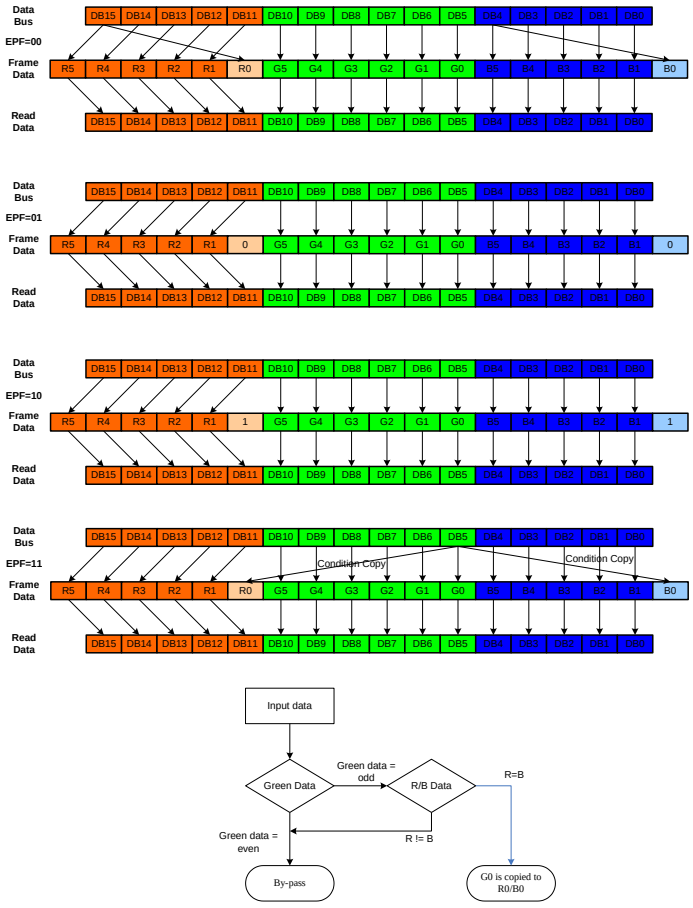
Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through

the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	111 (16.77M color)	8- bit RGB interface (3 transfer/pixel)
	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]:

65K color mode data format.



EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)
00	MSB is inputted to LSB r [5:0] = {R [4:0], R [4]} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], B [4]}
01	"0" is inputted to LSB r [5:0] = {R [4:0], 0} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 0} Exception: R [4:0], B[4:0] = 5'h1F → r [5:0], b[5:0] = 6'h3F
10	"1" is inputted to LSB r [5:0] = {R [4:0], 1} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 1}

			Exception: R [4:0], B[4:0] = 5'h00 → r [5:0], b[5:0] = 6'h00
		11	Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 3: R=G≠B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}
Restriction	Access when EXTC_EN=1 (Set RDDh=01)		

5.3.17. Get External Register for SPI (D9h)

D9h	Get External Register for SPI											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	0	1	D9
1st Parameter	1	1	↑	0	0	0	ext_spi_read_en	ext_spi_cnt[3:0]				00

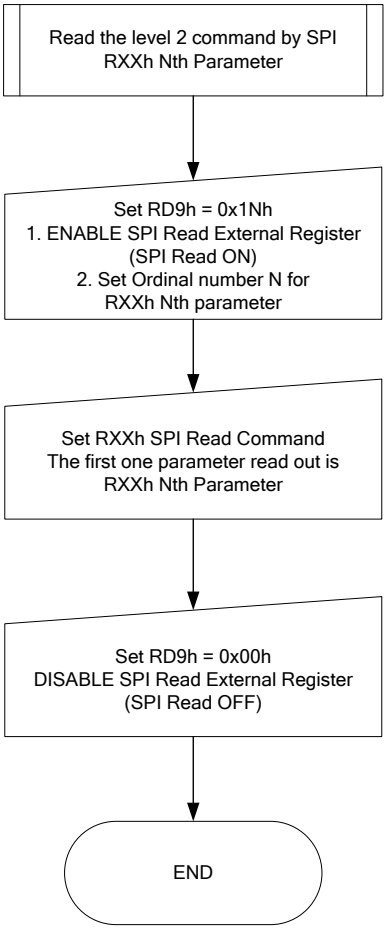
Description

ext_spi_read_en :

This command is used to enable the SPI interface to access the level 2 commands.

Ext_spi_cnt [3:0] :

Th SPI will get the one desired parameter of the external register by setting this ordinal number.



Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.18. Set EXTC (DDh)

DDh	Get External Register for SPI											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	0	1	DD
1st Parameter	1	1	↑	0	0	0	0	0	0	0	EXTC_EN	00
Description	**EXTC_EN :** This command is used to enable All interface to write the level 2 commands. Turn on the level 2 commands if setting EXTC_EN=1. Turn off the level 2 commands if setting EXTC_EN=0.											
Restriction	None											

5.3.19. NV Memory Program Setting (DEh)

DEh	NV Memory Program Setting											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	1	0	DE
1st Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
2nd Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
3rd Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
4th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
5th Parameter	1	1	↑	otp_te_sel[3:0]				0	0	0	0	00

Description

TE/TE1 pin output OTP finish flag signal setting (NV memory program use).

otp_te_sel[3:0]：TE/TE1 pin output OTP finish flag signal setting.

reg_test_te_sel[3:0]	TE / TE1 pin output
Ch	TE / TE1 pin output OTP finish flag signal (output signal can be selected by otp_finish_flag_sel[1:0] (RF8h P9) setting)
others	Reserved

Restriction: Access when EXTC_EN=1 (Set RDDh=01)

5.3.20. Smart Resolution Setting (DFh)

DFh	Smart Resolution Setting											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	1	1	DF
1st Parameter	1	1	↑	0	0	0	reso _gm	sreso _en	0	0	sreso_ col_ num[8]	01
2nd Parameter	1	1	↑	sreso_col_num[7:0]								40

Description

reso_gm：

Display resolution setting.

sreso_en：

Smart resolution enable.

sreso_col_num[8:0]：

Horzorital (X) resolution setting for smart resolution.

reg_sreso_en	reg_reso_gm	Resolution
0	0	320RGBx240
0	1	240RGBx240
1	X	X: reg_sreso_col_num[8:0] Y: 240 (It can be adjusted by NL[6:0] setting)

(X: Don't care)

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.21. Memory Control (E1h)

E1h	Memory Control											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	0	1	E1
1st Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
2nd Parameter	1	1	↑	0	0	1	0	0	0	0	wemode	20
Description	**wemode：** WEMODE=0：When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. WEMODE=1：When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.											
Restriction	Access when EXTC_EN=1 (Set RDDh=01)											

5.3.22. Positive Gamma Correction (E4h)

E4h	Positive Gamma Correction											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	1	0	0	E4
1st Parameter	1	1	↑	0	0	0	0	VP0[3:0]				00
2nd Parameter	1	1	↑	0	0	VP1[5:0]						05
3rd Parameter	1	1	↑	0	0	VP2[5:0]						12
4th Parameter	1	1	↑	0	0	0	0	VP4[3:0]				09
5th Parameter	1	1	↑	0	0	0	VP6[4:0]					17
6th Parameter	1	1	↑	0	0	0	0	VP13[3:0]				08
7th Parameter	1	1	↑	0	VP20[6:0]							40
8th Parameter	1	1	↑	VP36[3:0]				VP27[3:0]				55
9th Parameter	1	1	↑	0	VP43[6:0]							50
10th Parameter	1	1	↑	0	0	0	0	VP50[3:0]				04
11th Parameter	1	1	↑	0	0	0	VP57[4:0]					0A
12th Parameter	1	1	↑	0	0	0	0	VP59[3:0]				07
13th Parameter	1	1	↑	0	0	VP61[5:0]						21
14th Parameter	1	1	↑	0	0	VP62[5:0]						24
15th Parameter	1	1	↑	0	0	0	0	VP63[3:0]				0D
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	Access when EXTC_EN=1 (Set RDDh=01)											

5.3.23. Negative Gamma Correction (E5h)

E5h	Negative Gamma Correction											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	1	0	1	E5
1st Parameter	1	1	↑	0	0	0	0	VN0[3:0]				00
2nd Parameter	1	1	↑	0	0	VN1[5:0]						05
3rd Parameter	1	1	↑	0	0	VN2[5:0]						11
4th Parameter	1	1	↑	0	0	0	0	VN4[3:0]				09
5th Parameter	1	1	↑	0	0	0	VN6[4:0]					17
6th Parameter	1	1	↑	0	0	0	0	VN13[3:0]				09
7th Parameter	1	1	↑	0	VN20[6:0]							40
8th Parameter	1	1	↑	VN36[3:0]				VN27[3:0]				46
9th Parameter	1	1	↑	0	VN43[6:0]							4E
10th Parameter	1	1	↑	0	0	0	0	VN50[3:0]				08
11th Parameter	1	1	↑	0	0	0	VN57[4:0]					0F
12th Parameter	1	1	↑	0	0	0	0	VN59[3:0]				0C
13th Parameter	1	1	↑	0	0	VN61[5:0]						21
14th Parameter	1	1	↑	0	0	VN62[5:0]						25
15th Parameter	1	1	↑	0	0	0	0	VN63[3:0]				0D
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	Access when EXTC_EN=1 (Set RDDh=01)											

5.3.24. Backlight Control 1 (E8h)

E8h	Backlight Control 1											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	0	0	E8
1st Parameter	1	1	↑	1	1	1	1	1	1	1	1	FF
2nd Parameter	1	1	↑	0	0	0	0	0	0	0	pwm_pol	00

Description

pwm_pol :

The bit is used to define polarity of LEDPWM signal.

BL (Cmd. 53h)	PWM_POL	PWM Output Signal
0	0	Always Low
0	1	Always High
1	0	Original Polarity of PWM Signal
1	1	Inversed Polarity of PWM Signal

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.25. Backlight Control 2 (E9h)

E9h	Backlight Control 2											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	0	1	E9
1st Parameter	1	1	↑	THRES_MOV[3:0]				THRES_STILL[3:0]				BB
2nd Parameter	1	1	↑	0	0	0	0	THRES_UI[3:0]				0B

Description

THRES_MOV[3:0]：

These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

THRES_MOV [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

THRES_MOV [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

THRES_STILL[3:0]：

These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

THRES_STILL [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

THRES_STILL [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

THRES_UI[3:0]：

These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

THRES_UI [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

THRES_UI [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.26. Backlight Control 3 (EAh)

EAh	Backlight Control 3											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	1	0	EA
1st Parameter	1	1	↑	DTH_MOV[3:0]				DTH_STILL[3:0]				A8
2nd Parameter	1	1	↑	0	0	0	0	DTH_UI[3:0]				03

Description

DTH_MOV[3:0]：

dither ratio for moving image mode.

This parameter is used set the minimum limitation of grayscale threshold value.

This register setting will limit the minimum Dth value in moving image mode to prevent the display image from being too white and the display quality is not acceptable.

DTH_MOV [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_MV [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_STILL[3:0]：

dither ratio for still picture mode.

This parameter is used set the minimum limitation of grayscale threshold value.

This register setting will limit the minimum Dth value in still picture mode to prevent the display image from being too white and the display quality is not acceptable.

DTH_STILL [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_STILL [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_UI[3:0]：

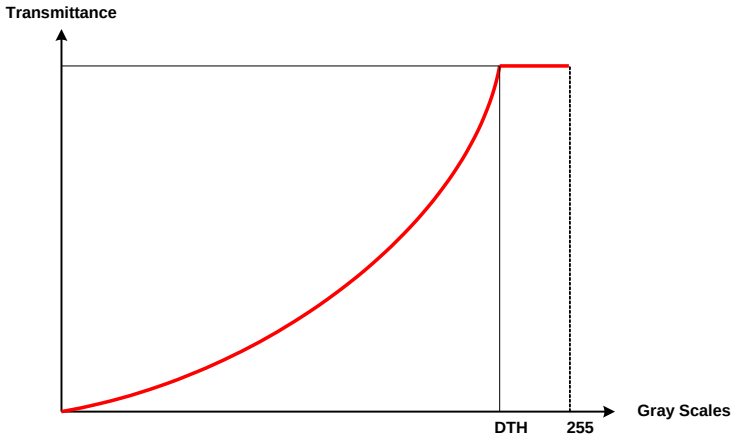
dither ratio for User Icon(UI) image mode.

This parameter is used set the minimum limitation of grayscale threshold value.

This register setting will limit the minimum Dth value in User Icon(UI) image mode to prevent the display image from being too white and the display quality is not acceptable.

DTH_UI [3:0]	Description
4'0h	252
4'1h	248
4'2h	244
4'3h	240
4'4h	236
4'5h	232
4'6h	228
4'7h	224

DTH_UI [3:0]	Description
4'8h	220
4'9h	216
4'Ah	212
4'Bh	208
4'Ch	204
4'Dh	200
4'Eh	196
4'Fh	192



Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.27. Backlight Control 4 (EBh)

EBh	Backlight Control 4											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	1	1	EB
1st Parameter	1	1	↑	0	cabc_dim_mov[2:0]			0	cabc_dim_still[2:0]			43
2nd Parameter	1	1	↑	cabc_dim_min[3:0]				0	cabc_dim_ui[2:0]			02

Description

cabc_dim_mov[2:0]：

This parameter is used to set the transition time of brightness level in moving image mode to avoid the sharp brightness transition on vision.

cabc_dim_mov [2:0]	Description
3'0h	1~2 frames
3'1h	1~3 frames
3'2h	2~6 frames
3'3h	4~12 frames
3'4h	8~24 frames
3'5h	16~48 frames
3'6h	32~96 frames
3'7h	64~192 frames

cabc_dim_still[2:0]：

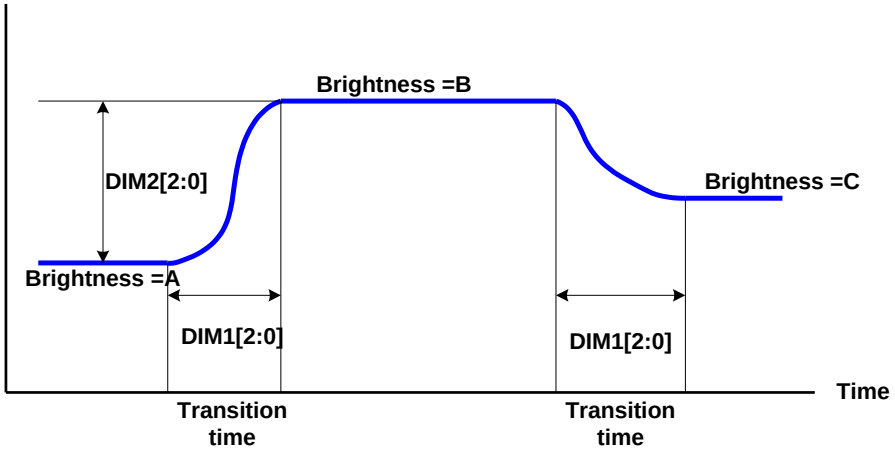
This parameter is used to set the transition time of brightness level in still picture mode to avoid the sharp brightness transition on vision.

cabc_dim_still [2:0]	Description
3'0h	1~2 frames
3'1h	1~3 frames
3'2h	2~6 frames
3'3h	4~12 frames
3'4h	8~24 frames
3'5h	16~48 frames
3'6h	32~96 frames
3'7h	64~192 frames

cabc_dim_ui[2:0]：

This parameter is used to set the transition time of brightness level in User Icon(UI) image mode to avoid the sharp brightness transition on vision.

cabc_dim_ui [2:0]	Description
3'0h	1~2 frames
3'1h	1~3 frames
3'2h	2~6 frames
3'3h	4~12 frames
3'4h	8~24 frames
3'5h	16~48 frames
3'6h	32~96 frames
3'7h	64~192 frames



cabc_dim_min[3:0]：

This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than cabc_dim_min[3:0], the brightness transition will be ignored.

For example：

If | brightness B – brightness A| < cabc_dim_min[3:0], the brightness transition will be ignored and keep the brightness A.

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.28. Backlight Control 5 (ECh)

ECh	Backlight Control 5											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	1	0	0	EC
1st Parameter	1	1	↑	PWM_DIV[7:0]								D0

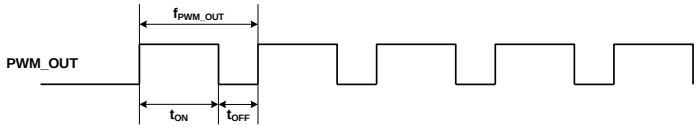
Description

PWM_DIV [7:0]：

PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{PWM\_OUT} = \frac{16MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

PWM_DIV [7:0]	f_{PWM_OUT}
8'h0	62.74 KHz
8'h1	31.38 KHz
8'h2	20.915KHz
8'h3	15.686KHz
8'h4	12.549 KHz
…	…
8'hFB	249Hz
8'hFC	248Hz
8'hFD	247Hz
8'hFE	246Hz
8'hFF	245Hz



Note: The output frequency tolerance of internal frequency divider in CABC is ±10%

Restriction: Access when EXTC_EN=1 (Set RDDh=01)

5.3.29. ID code setting (EFh)

EFh	ID code setting											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	1	1	1	EF
1st Parameter	1	1	↑	REG_ID1[7:0]								E3
2nd Parameter	1	1	↑	REG_ID2[7:0]								00
3rd Parameter	1	1	↑	REG_ID3[7:0]								00
Description	**REG_ID1[7:0] :** ID1 code setting (Setting data map to RDAh P1, reading ID1[7:0] code from RDAh P1) **REG_ID2[7:0] :** ID2 code setting (Setting data map to RDBh P1, reading ID2[7:0] code from RDBh P1) **REG_ID3[7:0] :** ID3 code setting (Setting data map to RDCh P1, reading ID3[7:0] code from RDCh P1)											
Restriction	Access when EXTC_EN=1 (Set RDDh=01)											

5.3.30. NV Memory Control and Status Read (F8h)

F8h	NV Memory Control and Status Read											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	0	F8
1st Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
2nd Parameter	1	1	↑	0	0	0	1	0	0	0	0	10
3rd Parameter	1	1	↑	0	0	0	1	0	0	1	0	12
4th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
5th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
6th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
7th Parameter	1	1	↑	0	0	0	0	0	0	0	0	00
8th Parameter (R)	1	1	↑	prog_ finish	prog_fini sh_fail	0	0	0	0	0	0	00
9th Parameter (W/R)	1	1	↑	0	0	0	0	0	0	otp_finish_flag_sel [1:0]		00

Description

prog_finish：

OTP program finish and pass flag

prog_finish_fail：

OTP program finish and fail flag

OTP program status (by reading data)		
prog_finish	prog_finish_fail	Description
1	0	OTP program finish and pass
0	1	OTP program finish and fail

otp_finish_flag_sel[1:0]：

OTP flag signal selection, it can output from TE/TE1 pin by otp_te_sel[3:0] setting.

otp_finish_flag_sel[1:0]	Description
2'b00	OTP busy
2'b10	OTP program finish and pass

Restriction: Access when EXTC_EN=1 (Set RDDh=01)

5.3.31. NV Memory Control (F9h)

F9h	NV Memory Control											
W/R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	0	0	1	F9
1st Parameter	1	1	↑	0	0	0	0	0	0	0	mtp_pump_set_en	00
Description	**mtp_pump_set_en :** VGL selection when OTP program 1'b0 : VGL for normal display 1'b1 : VGL for OTP program (VGL = Typical OTP program voltage)											
Restriction	Access when EXTC_EN=1 (Set RDDh=01)											

5.3.32. NV Memory Write(FDh)

FDh	NV Memory Write											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	0	1	FD
1st Parameter	1	1	↑	pgm_adr[7:0]								00
2nd Parameter	1	1	↑	pgm_adr[15:8]								00
3rd Parameter	1	1	↑	pgm_data[7:0]								xx

Description

This command is used to program the NV memory data. After a successful NV memory programming operation, the information of PGM_DATA [7:0] will programmed to NV memory.

pgm_adr[15:0]：

The programmed address.

The select bits of ID1, ID2, ID3 ,VCOM , MADCTL and Gamma OTP programming.

pgm_data[7:0]：

The programmed data.

PGM_ADR [15:0]	PGM_DATA [7:0]								Programmed NV Memory Selection	Check ADDR
0038h	ID1[7:0] OTP program 1st time (ID1 can be programmed 2 times)								ID1 programming	RDAh P1 REFh P1
0039h	ID1[7:0] OTP program 2nd time (ID1 can be programmed 2 times)								ID1 programming	RDAh P1 REFh P1
003Ah	ID2[7:0] OTP program 1st time (ID2 can be programmed 2 times)								ID2 programming	RDBh P1 REFh P2
003Bh	ID2[7:0] OTP program 2nd time (ID2 can be programmed 2 times)								ID2 programming	RDBh P1 REFh P2
003Ch	ID3[7:0] OTP program 1st time (ID3 can be programmed 2 times)								ID3 programming	RDCh P1 REFh P3
003Dh	ID3[7:0] OTP program 2nd time (ID3 can be programmed 2 times)								ID3 programming	RDCh P1 REFh P3
0040h	VCOM[6:0] OTP program 1st time (VCOM can be programmed 3 times)								VCOM programming	RC8h P1
0041h	VCOM[6:0] OTP program 2nd time (VCOM can be programmed 3 times)								VCOM programming	RC8h P1
0042h	VCOM[6:0] OTP program 3rd time (VCOM can be programmed 3 times)								VCOM programming	RC8h P1
003Eh	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	0	0	MADCTL_EOR programming	RD5h P1
003Fh	MY_EOR	MX_EOR	MV_EOR	ML_EOR	BGR_EOR	0	0	0	MADCTL_EOR programming	RD5h P1
(MADCTL_EOR can be programmed 2 times, 1st time set 003Eh , 2nd time set 003Fh)										
0043h	0	0	0	0	VP0[3:0]				(Positive Gamma Control) programming	RE4h P1
0044h	0	0	VP1[5:0]							RE4h P2
0045h	0	0	VP2[5:0]							RE4h P3
0046h	0	0	0	0	VP4[3:0]					RE4h P4
0047h	0	0	0	VP6[4:0]						RE4h P5
0048h	0	0	0	0	VP13[3:0]					RE4h P6
0049h	0	VP20[6:0]								RE4h P7
004Ah	VP36[3:0]				VP27[3:0]					RE4h P8
004Bh	0	VP43[6:0]								RE4h P9
004Ch	0	0	0	0	VP50[3:0]					RE4h P10
004Dh	0	0	0	VP57[4:0]						EE4h P11

	004Eh	0	0	0	0	VP59[3:0]		RE4h P12
	004Fh	0	0	VP61[5:0]				RE4h P13
	0050h	0	0	VP62[5:0]				RE4h P14
	0051h	0	0	0	0	VP63[3:0]		RE4h P15
	0052h	0	0	0	0	VP0[3:0]	(Negative Gamma Control) programming	RE5h P1
	0053h	0	0	VP1[5:0]				RE5h P2
	0054h	0	0	VP2[5:0]				RE5h P3
	0055h	0	0	0	0	VP4[3:0]		RE5h P4
	0056h	0	0	0	VP6[4:0]			RE5h P5
	0057h	0	0	0	0	VP13[3:0]		RE5h P6
	0058h	0	VP20[6:0]					RE5h P7
	0059h	VP36[3:0]				VP27[3:0]		RE5h P8
	005Ah	0	VP43[6:0]					RE5h P9
	005Bh	0	0	0	0	VP50[3:0]		RE5h P10
	005Ch	0	0	0	VP57[4:0]			RE5h P11
	005Dh	0	0	0	0	VP59[3:0]		RE5h P12
	005Eh	0	0	VP61[5:0]				RE5h P13
	005Fh	0	0	VP62[5:0]				RE5h P14
	0060h	0	0	0	0	VP63[3:0]		RE5h P15

(Positive/Negative Gamma Control can be programmed 1 time)

Restriction	Access when EXTC_EN=1 (Set RDDh=01)

5.3.33. NV Memory Protection Key (FEh)

FEh	NV Memory Protection Key											
W	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	1	0	FE
1st Parameter	1	1	↑	key[23:16]								55
2nd Parameter	1	1	↑	key[15:8]								AA
3rd Parameter	1	1	↑	key[7:0]								66
Description	**KEY [23:0]:** NV memory programming protection key. When writing programming data, this register must be set 0x55AA66h to enable NV memory programming. If this register is not written with 0x55AA66h, then NV memory programming will be aborted.											
Restriction	Access when EXTC_EN=1 (Set RDDh=01)											

5.3.34. NV Memory Status Read(FFh)

FFh	NV Memory Status Read											
R	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	1	1	FF
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	0	0	0	0	0	0	0	0	00
3rd Parameter	1	↑	1	madctrl_mark[1:0]		id3_mark[1:0]		id2_mark[1:0]		id1_mark[1:0]		00
4th Parameter	1	↑	1	0	0	0	gamma _mark	0	vcm_mark[2:0]			00

Description

Id1_mark [1:0] / id2_mark [1:0] / id3_mark [1:0] / madctrl_mark [1:0]：

NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

Id1_mark [1:0] / id2_mark [1:0] Id3_mark [1:0] / madctrl_mark [1:0]		Description
Status		Availability
0	0	No Programmed
0	1	Programmed 1 time
1	1	Programmed 2 times

vcm_mark [2:0]：

NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

vcm_mark [2:0]			Description
Status			Availability
0	0	0	No Programmed
0	0	1	Programmed 1 time
0	1	1	Programmed 2 times
1	1	1	Programmed 3 times

gamma_mark：

NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

gamma_mark	Description
Status	Availability
0	No Programmed
1	Programmed 1 time

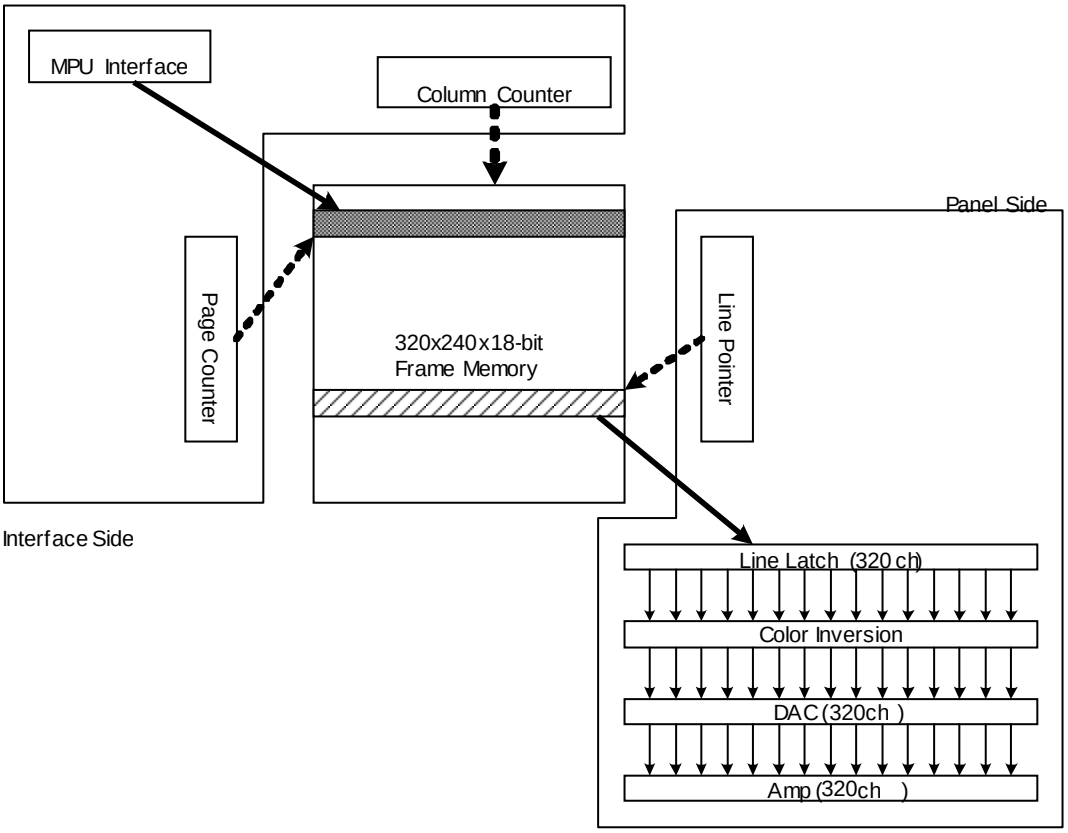
Note：1st Parameter：Dummy Read

Restriction: Access when EXTC_EN=1 (Set RDDh=01)

6. Display Data RAM

6.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (320x18x240 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

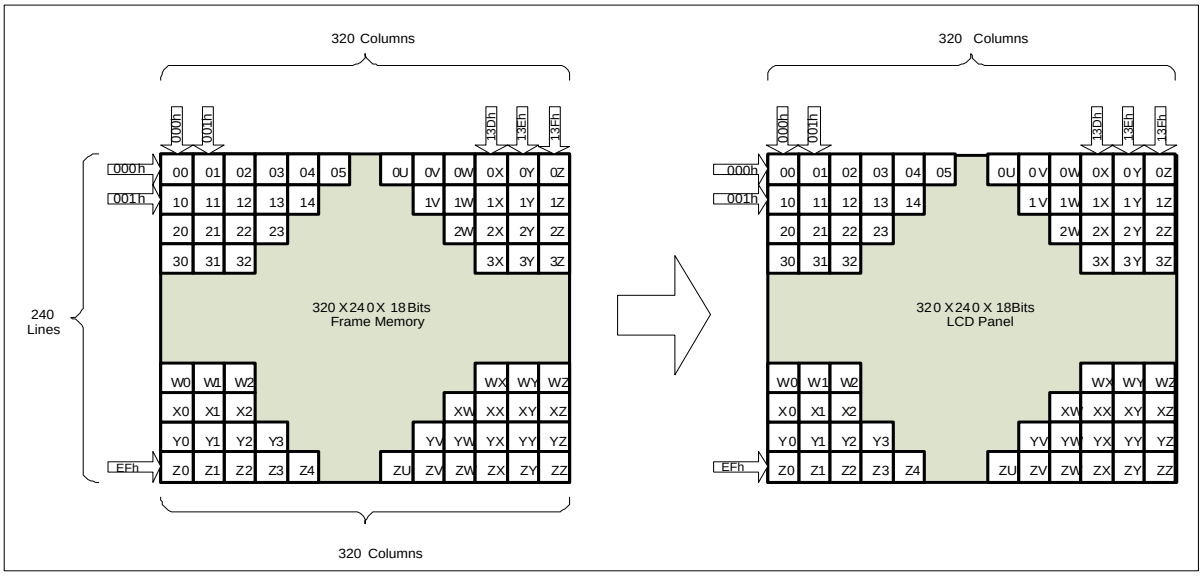


6.2. Memory to Display Address Mapping

6.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 00EFh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

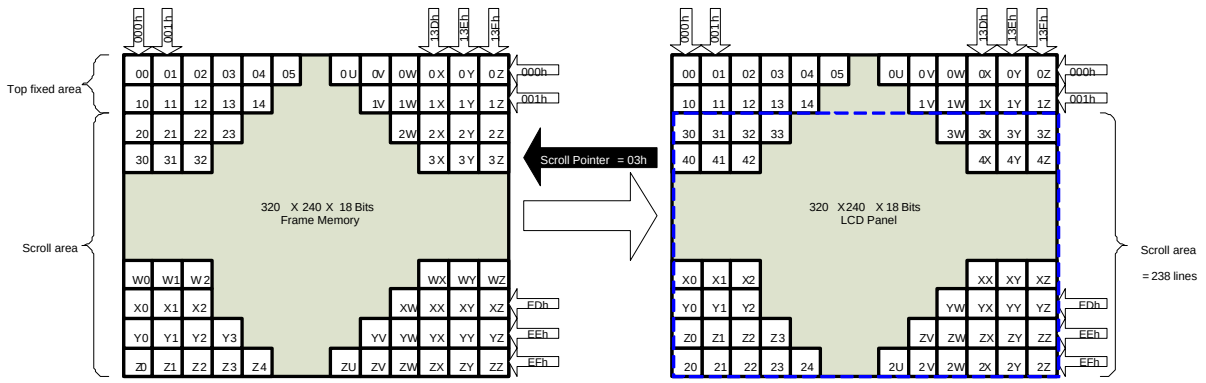


6.2.2. Vertical Scroll Mode

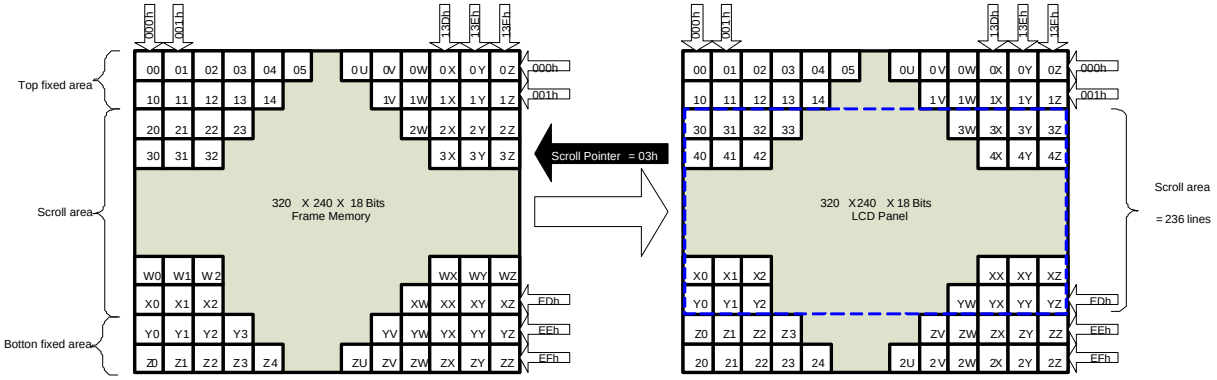
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.

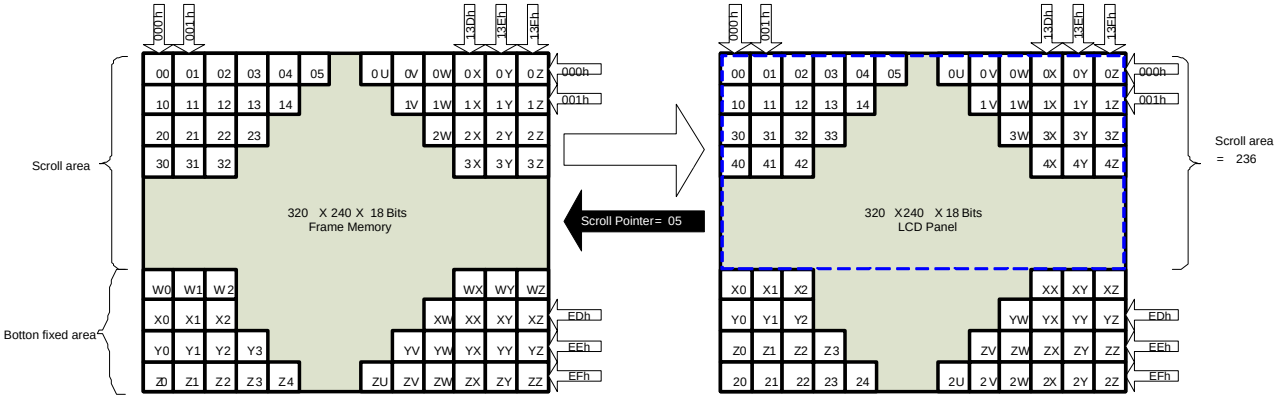
TFA=2, VSA=238, BFA=0 when MADCTL ML bit =0



TFA=2, VSA=236, BFA=2 when MADCTL ML bit =0



TFA=0, VSA=236, BFA=4 when MADCTL ML bit =0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 240, Scrolling Mode is undefined.

6.2.3. Vertical Scroll Example

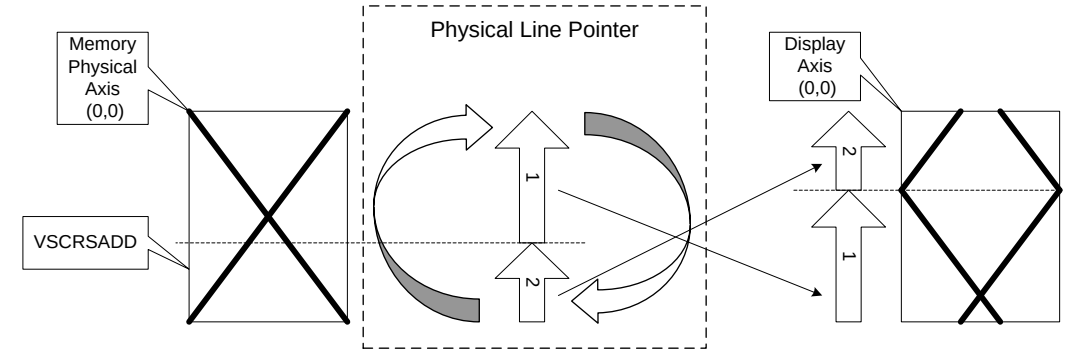
6.2.4. Case1: TFA+VSA+BFA < 240

This setting is prohibited, unless unexpected picture will be shown.

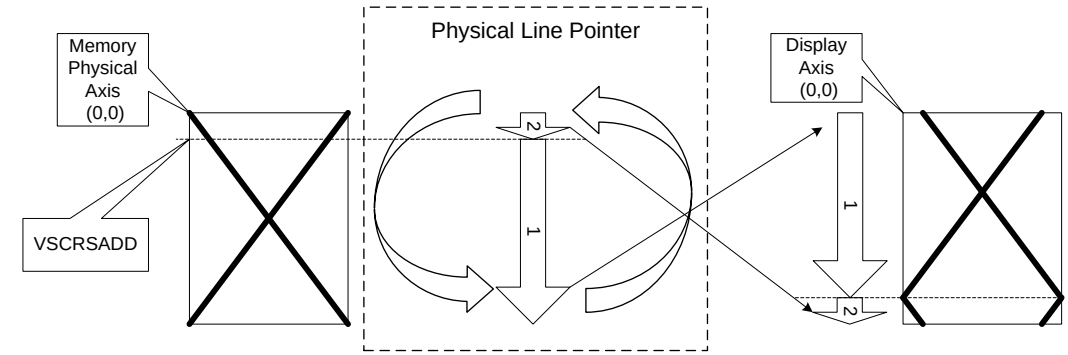
6.2.5. Case2: TFA+VSA+BFA = 240 (Rolling Scrolling)

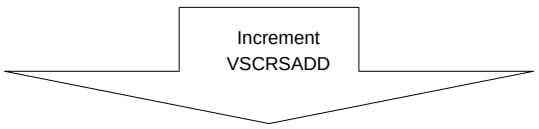
The operation of Rolling Scrolling is explained by these examples in the following.

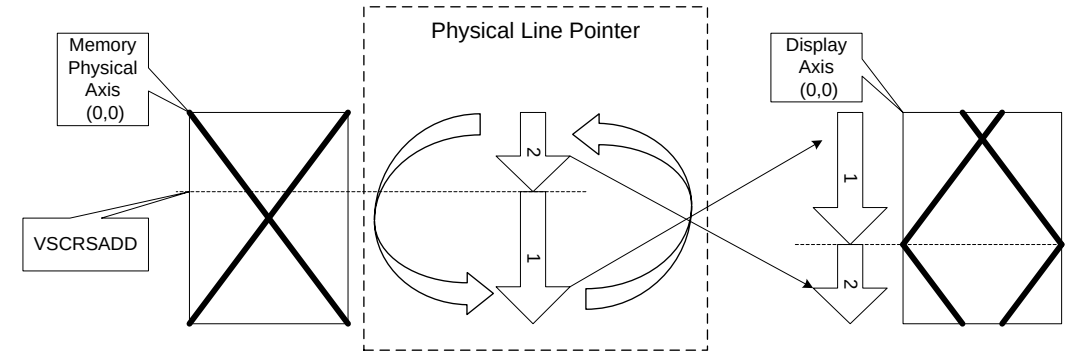
When TFA=0, VSA=240, BFA=0, VSCRSADD=40 and MADCTL ML D4 bit = 1



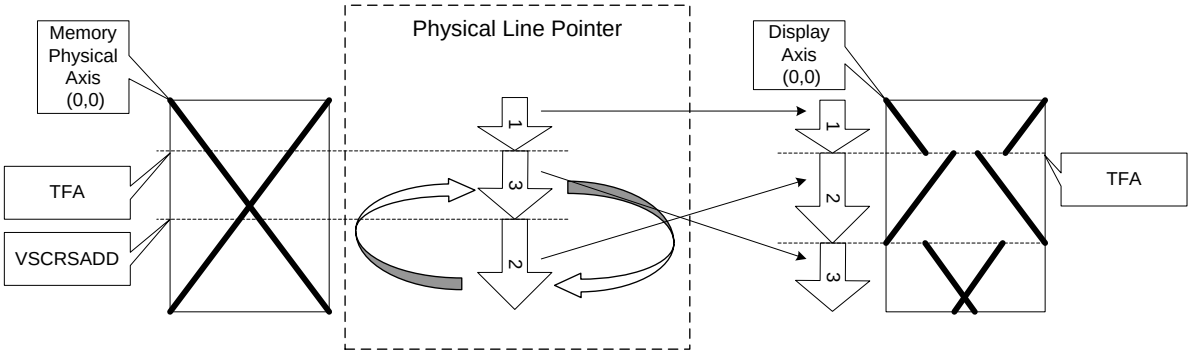
When TFA=0, VSA=240, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



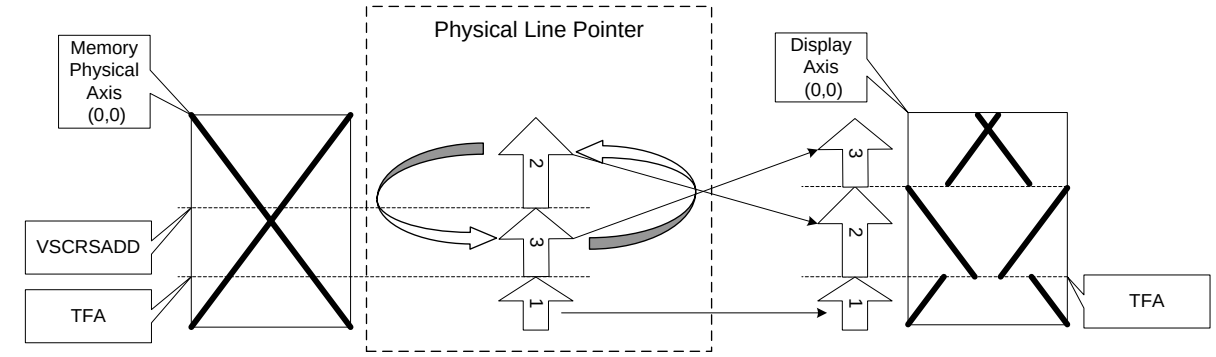


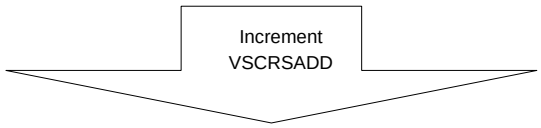


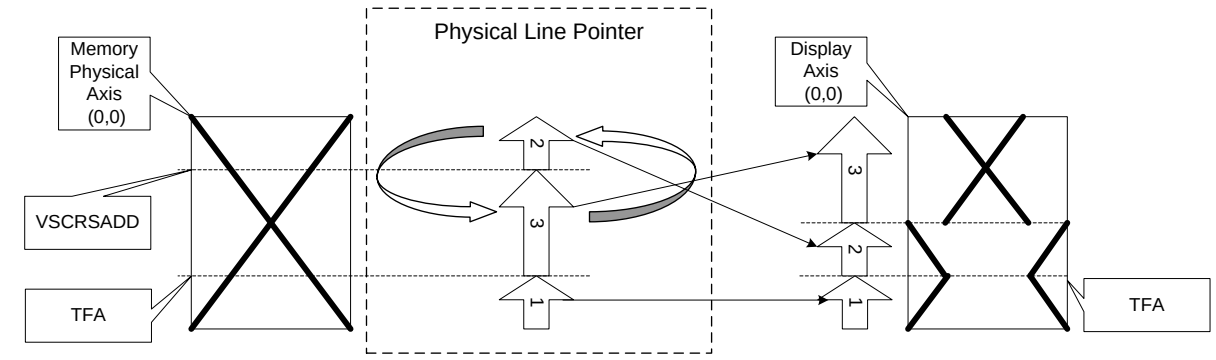
When TFA=30, VSA=210, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



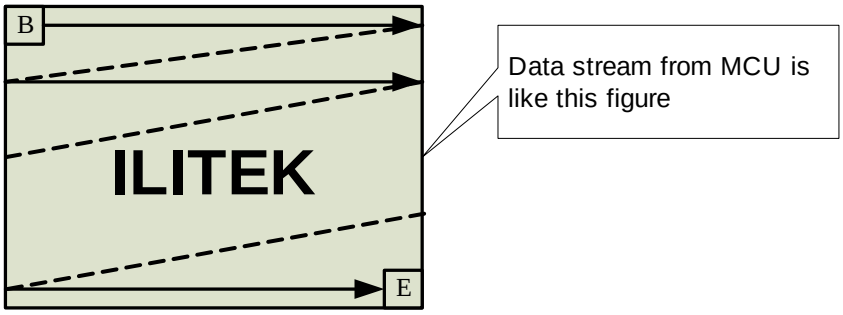
When TFA=30, VSA=210, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



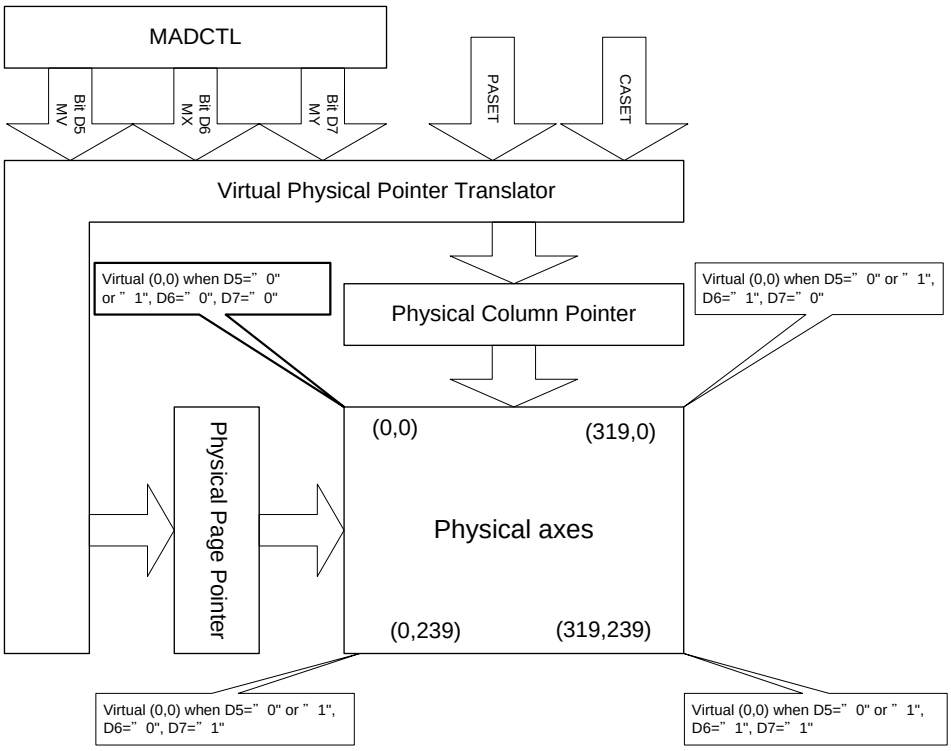




6.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, Bits D5, D6, and D7 as described below.



D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (239-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (239-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (239-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (239-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to "Start column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than "End Column"	Return to "Start column"	Increment by 1
The Page counter is large than "End Page"	Return to "Start column"	Return to "Start Page"

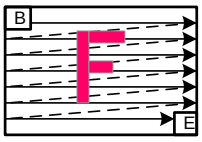
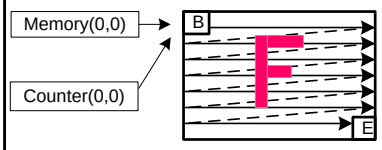
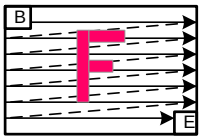
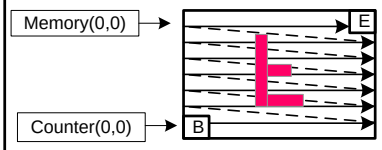
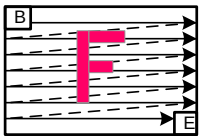
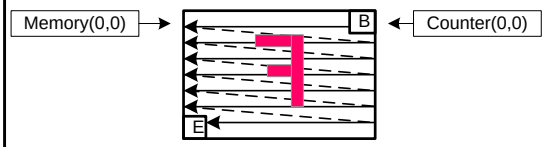
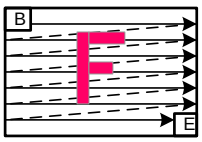
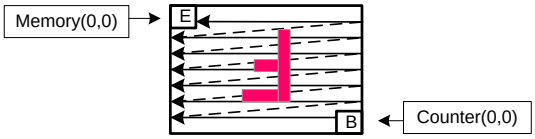
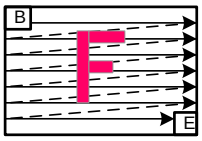
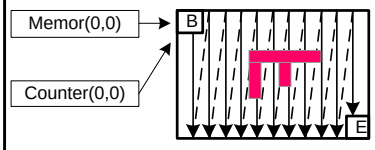
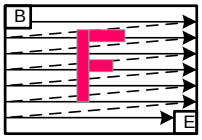
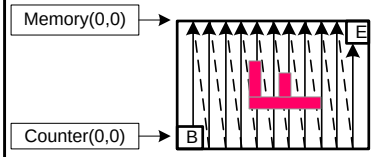
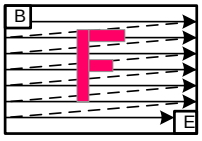
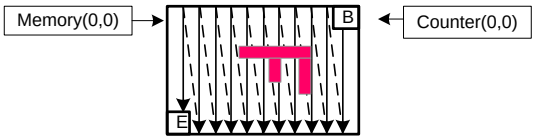
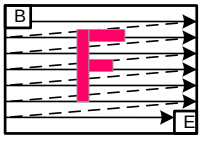
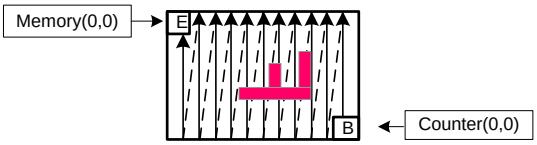
Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by

MADCTL bits D7, D6 and D5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

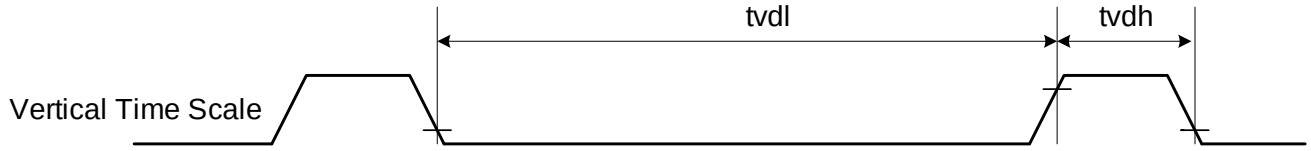
7. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

7.1. Tearing Effect Line Modes

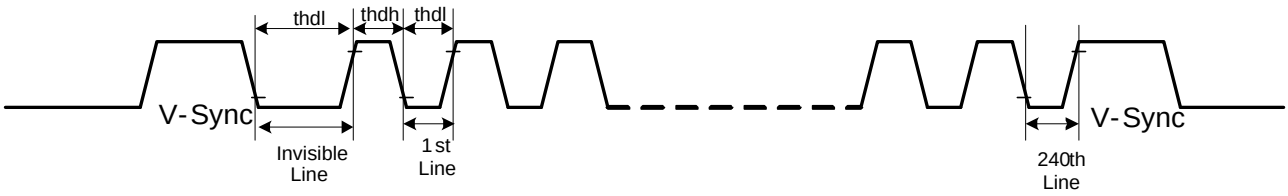
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

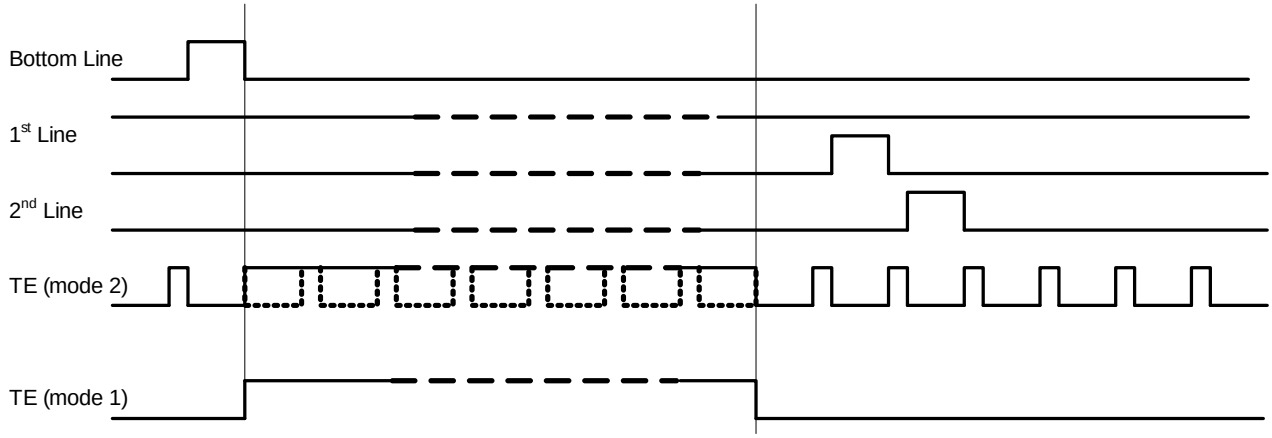
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 240 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

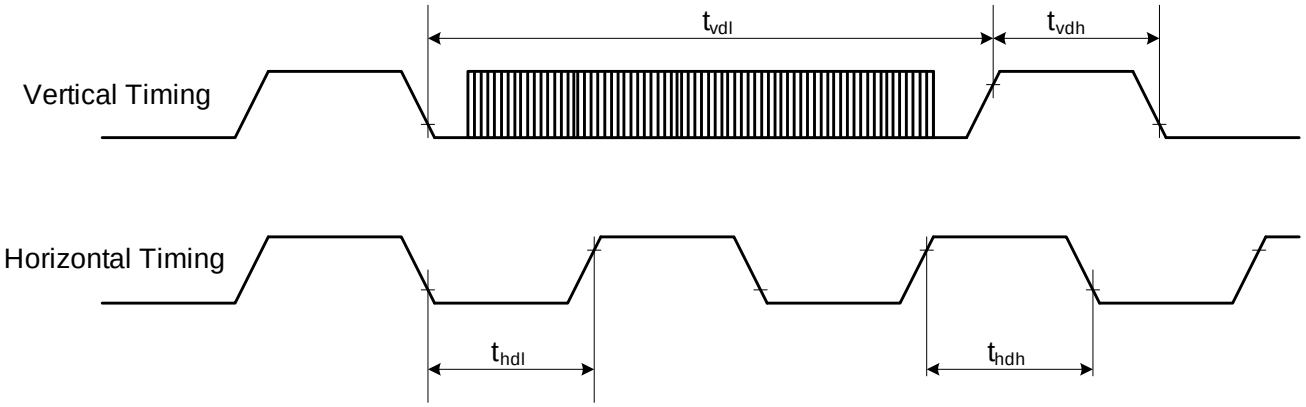
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

7.2. Tearing Effect Line Timings

The tearing effect signal is described below:

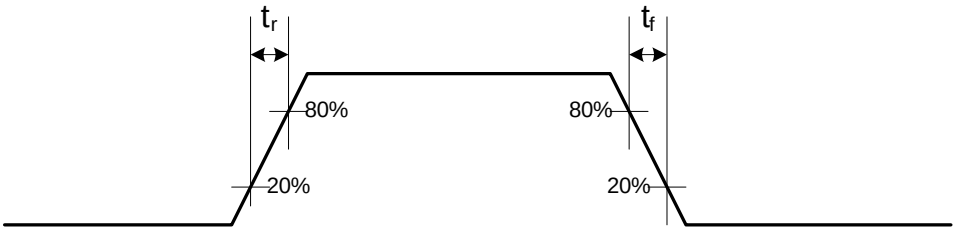


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	--	--	--	ms	
t_{vdh}	Vertical timing high duration	1000	--	--	us	
t_{hdl}	Horizontal timing low duration	--	--	--	us	
t_{hdh}	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL D4=0 and D4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

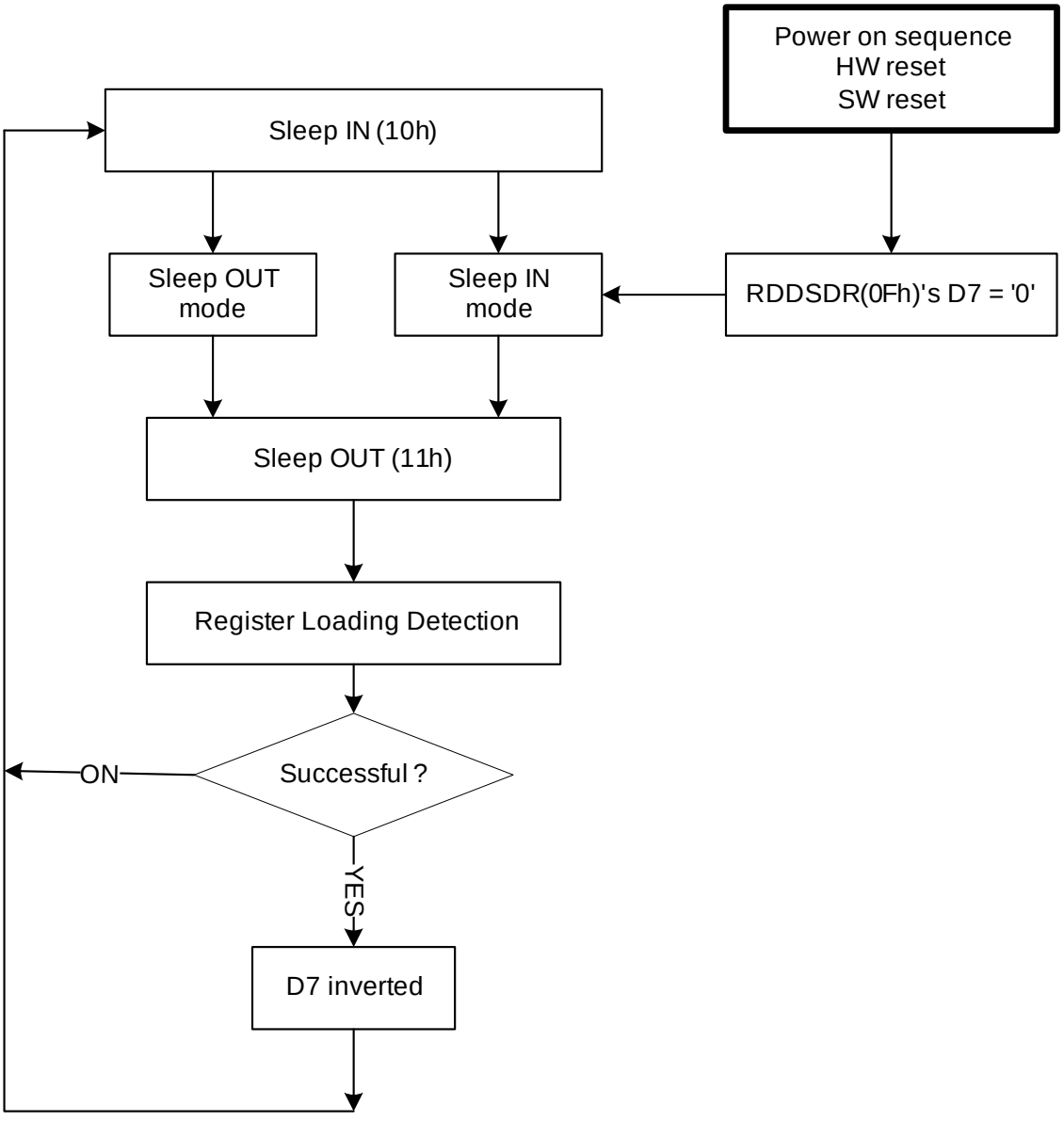
8. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

8.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

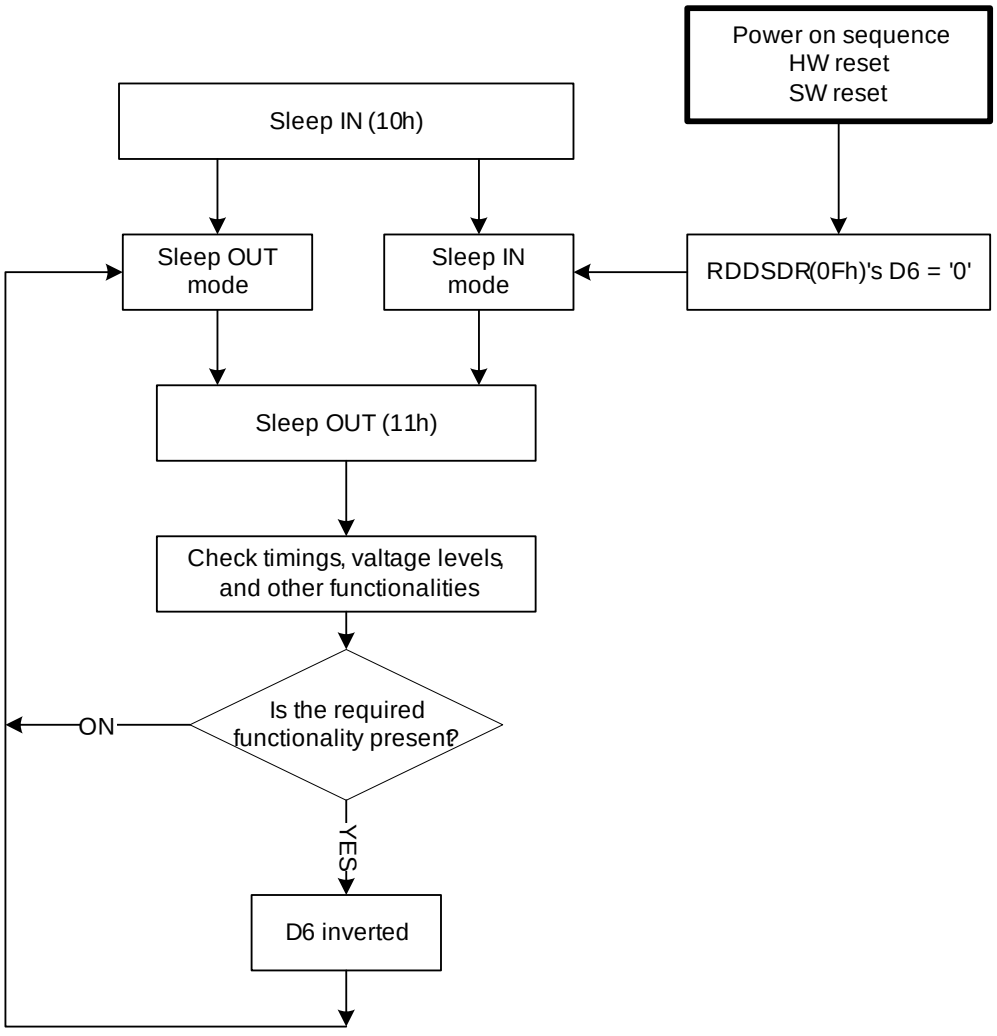


8.2. Functionality Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

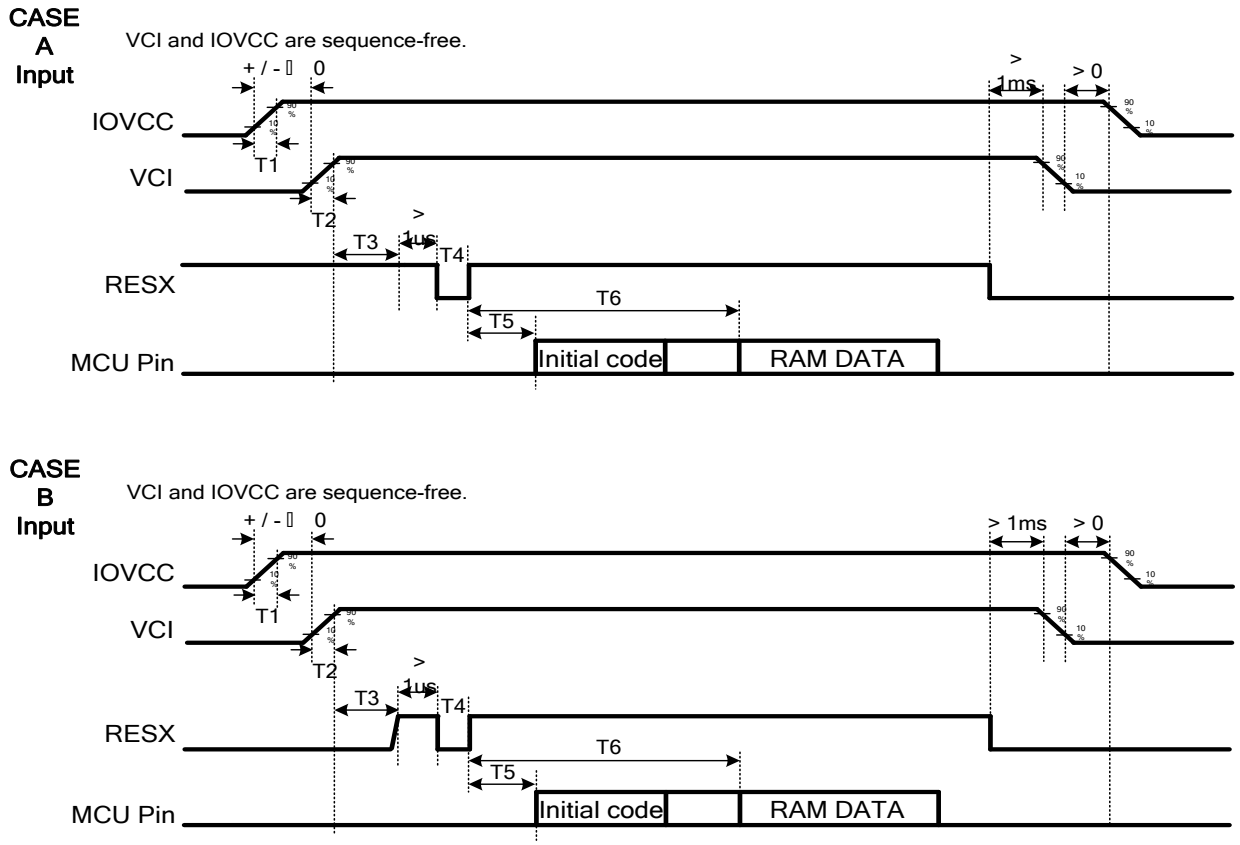
The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

9. Power ON/OFF Sequence

9.1. Power On/Off Sequence



T1 : IOVCC rise time
T2 : VCI rise time
T3 : All Power on to RESX high
T4 : Time of RESX LOW pulse width
T5 : Time of RESX to first command
T6 : Time of RESX to write ram data

Figure 73 The Power ON/OFF Sequence of 2-Power Mode

Symbol	description	Min.	Typ.	Max.	Unit
T1	CASE A：IOVCC rise time	100	-	-	us
	CASE B：IOVCC rise time	100	-	-	us
T2	CASE A：VCI rise time	100	-	-	us
	CASE B：VCI rise time	100	-	-	us
T3	All Power on to RESX high	5	-	-	ms
T4	Time of RESX LOW pulse width	10	-	-	us
T5	Time of RESX to first command	5	-	-	ms
T6	Time of RESX to write ram data	40	-	-	ms

Table 33 Power ON / OFF Timming

9.2. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9342E will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” actives.

10. Power Level Definition

10.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

   In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

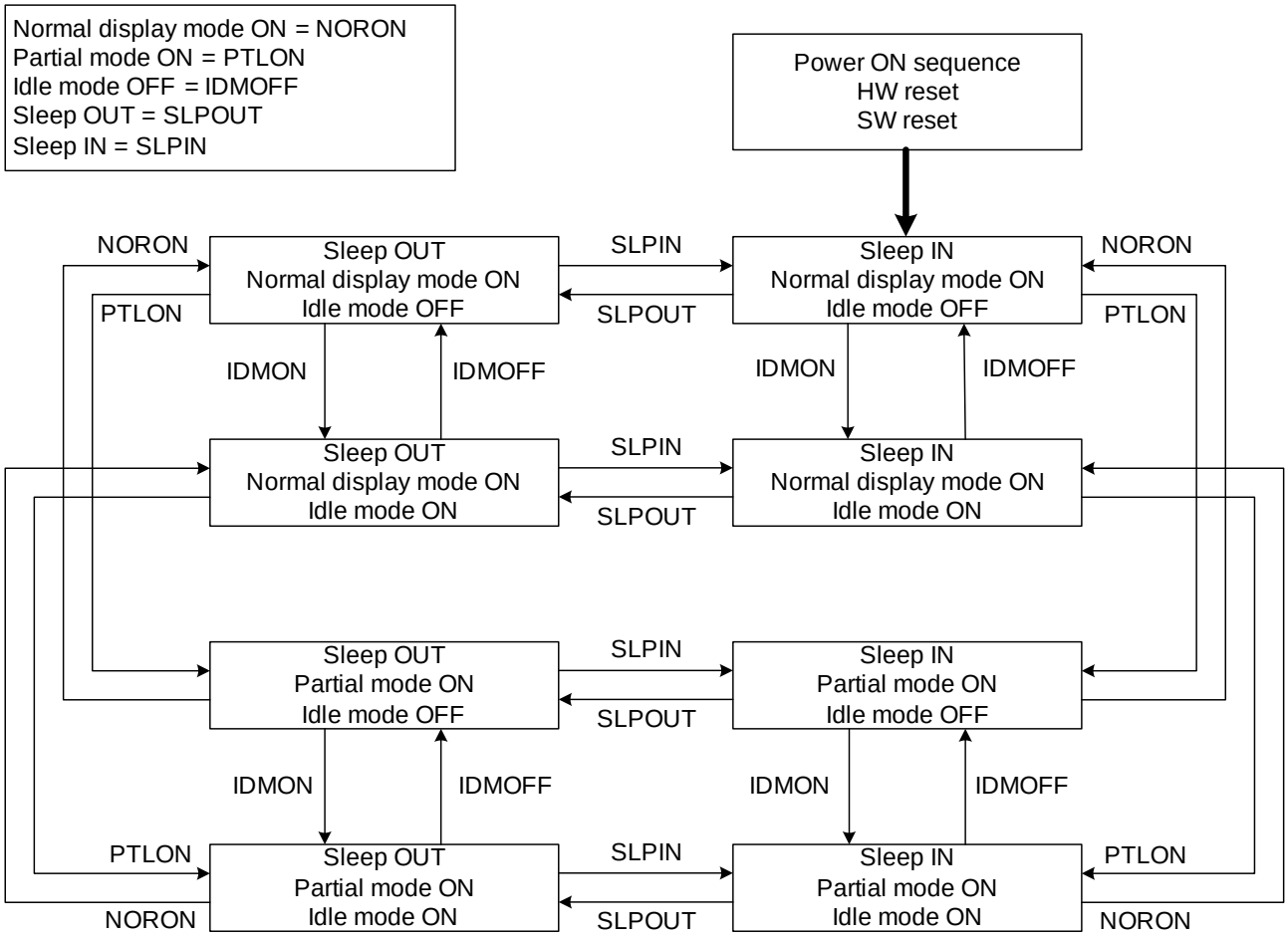
   In this mode, the DC/DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory can work. Contents of the memory are saved and not lost.

6. Power Off Mode.

   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

10.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

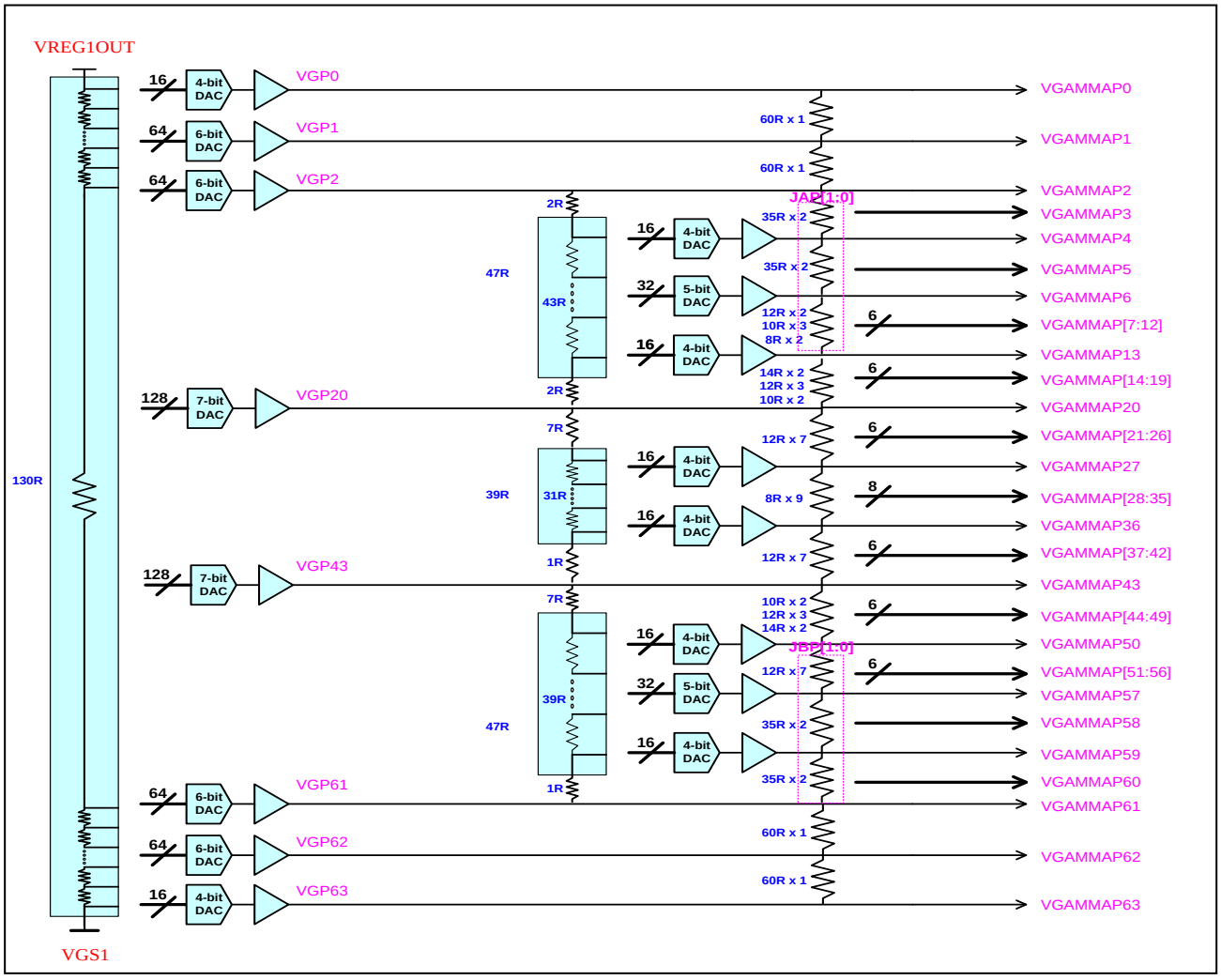
Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

11. Gamma Curves Selection

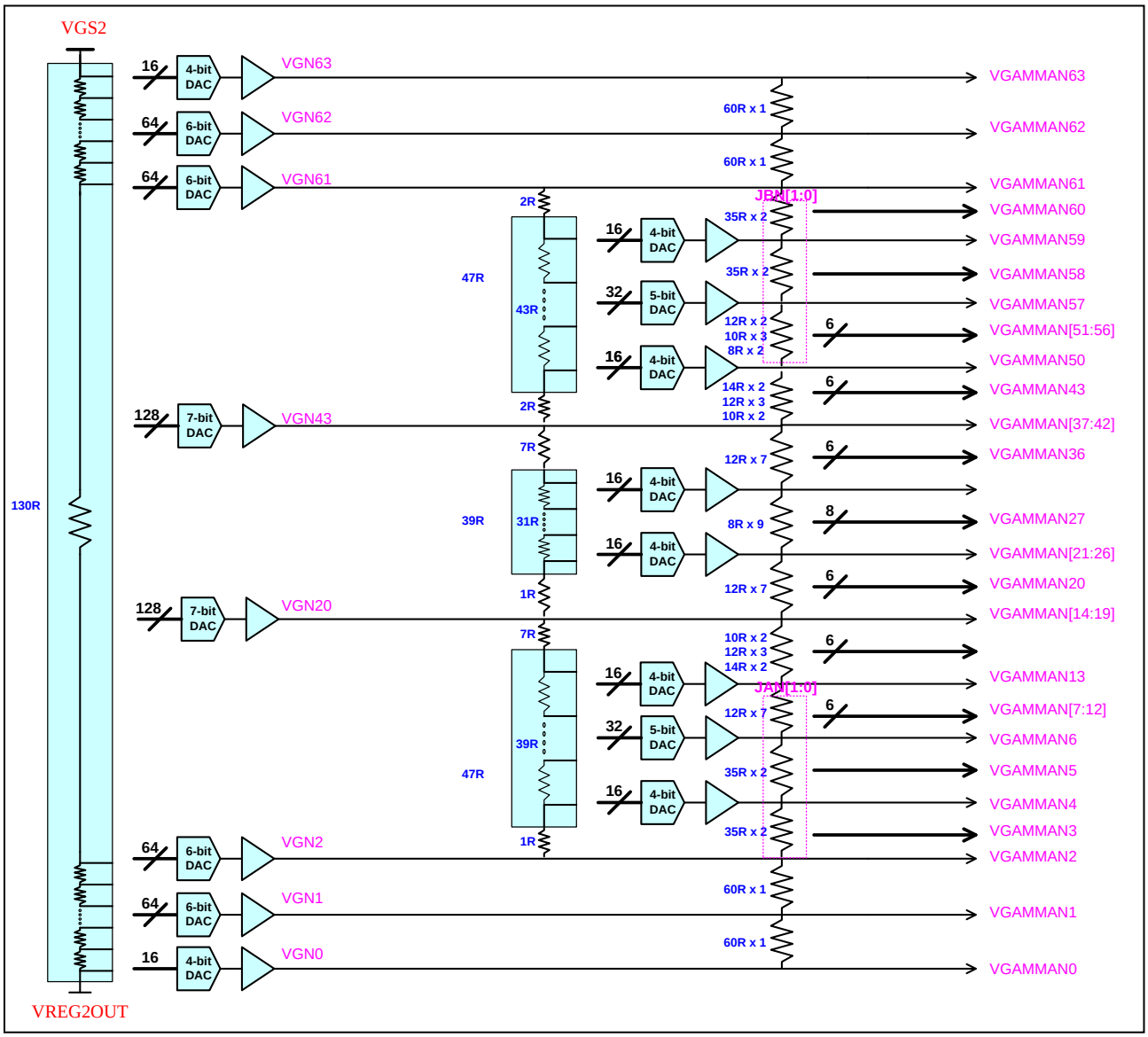
ILI9342E provide one gamma curves (Gamma2.2).

11.1. Gamma Default Values

Positive Gamma Control (E4h)



Negative Gamma Control (E5h)



Positive polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGAMMAP0	non	VGS1+ΔVDHP(130R-1R*VP0[3:0])/130R
VGAMMAP1	non	VGS1+ΔVDHP(130R-1R*VP0[5:0])/130R
VGAMMAP2	non	VGS1+ΔVDHP(130R-1R*VP0[5:0])/130R
VGAMMAP3	variable	VGAMMAP4+(VGAMMP2-VGAMMAP4)*JAP[1:0]
VGAMMAP4	variable	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((40R-1R*VP4[3:0])/47R)
VGAMMAP5	variable	VGAMMAP6+(VGAMMP4-VGAMMAP6)*JAP[1:0]
VGAMMAP6	variable	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((45R-1R*VP6[4:0])/47R)
VGAMMAP7	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP8	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP9	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP10	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP11	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP12	variable	VGAMMAP13+(VGAMMP6-VGAMMAP13)*JAP[1:0]
VGAMMAP13	variable	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((17R-1R*VP13[3:0])/47R)
VGAMMAP14	1.4R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(7R)/(8.4R)
VGAMMAP15	1.4R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(5.6R)/(8.4R)
VGAMMAP16	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(4.4R)/(8.4R)
VGAMMAP17	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(3.2R)/(8.4R)
VGAMMAP18	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(2R)/(8.4R)
VGAMMAP19	1R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(1R)/(8.4R)
VGAMMAP20	1R	VGS1+ΔVDHP(130R-1R*VP20 [6:0])/130R : VP20 [6:0] = 0~63 VGS1+ΔVDHP(129R-1R*VP20 [6:0])/130R : VP20 [6:0] = 64~127
VGAMMAP21	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(7.2R)/(8.4R)
VGAMMAP22	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(6R)/(8.4R)
VGAMMAP23	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(4.8R)/(8.4R)
VGAMMAP24	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(3.6R)/(8.4R)
VGAMMAP25	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(2.4R)/(8.4R)
VGAMMAP26	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(1.2R)/(8.4R)
VGAMMAP27	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((32R-1R*VP27[3:0])/39R)
VGAMMAP28	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(9.6R)/(10.8R)
VGAMMAP29	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(8.4R)/(10.8R)
VGAMMAP30	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(7.2R)/(10.8R)
VGAMMAP31	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(6R)/(10.8R)
VGAMMAP31	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(4.8R)/(10.8R)
VGAMMAP33	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(3.6R)/(10.8R)
VGAMMAP34	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(2.4R)/(10.8R)

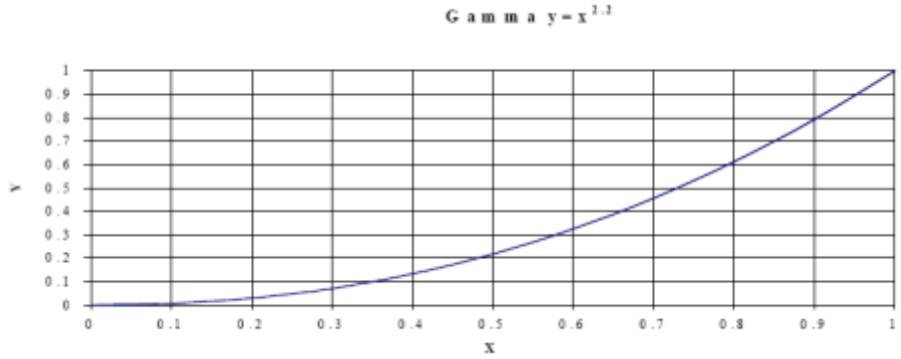
VGAMMAP35	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(1.2R)/(10.8R)
VGAMMAP36	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((16R-1R*VP36[3:0])/39R)
VGAMMAP31	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(7.2R)/(8.4R)
VGAMMAP38	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(6R)/(8.4R)
VGAMMAP39	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(4.8R)/(8.4R)
VGAMMAP40	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(3.6R)/(8.4R)
VGAMMAP41	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(2.4R)/(8.4R)
VGAMMAP42	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(1.2R)/(8.4R)
VGAMMAP43	1.2R	VGS1+ΔVDHP(130R-1R*VP43 [6:0])/130R : VP43 [6:0] = 0~63 VGS1+ΔVDHP(129R-1R*VP43 [6:0])/130R : VP43 [6:0] = 64~127
VGAMMAP44	1R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(7.4R)/(8.4R)
VGAMMAP45	1R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(6.4R)/(8.4R)
VGAMMAP46	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(5.2R)/(8.4R)
VGAMMAP47	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(4R)/(8.4R)
VGAMMAP48	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(2.8R)/(8.4R)
VGAMMAP49	1.4R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(1.4R)/(8.4R)
VGAMMAP50	1.4R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((40R-1R*VP50[3:0])/47R)
VGAMMAP51	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP52	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP53	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP54	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP55	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP56	variable	VGAMMAP57+(VGAMMP50-VGAMMAP57)*JBP[1:0]
VGAMMAP57	variable	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((31R-1R*VP57[3:0])/47R)
VGAMMAP58	variable	VGAMMAP59+(VGAMMP57-VGAMMAP59)*JBP[1:0]
VGAMMAP59	variable	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((21R-1R*VP59[3:0])/47R)
VGAMMAP60	variable	VGAMMAP61+(VGAMMP59-VGAMMAP61)*JBP[1:0]
VGAMMAP61	variable	VGS1+ΔVDHP(65R-1R*VP61[5:0])/130R
VGAMMAP62	non	VGS1+ΔVDHP(65R-1R*VP62[5:0])/130R
VGAMMAP63	non	VGS1+ΔVDHP(23R-1R*VP63[3:0])/130R

Negative polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGAMMAN0	non	VGS2+ΔVDHN(130R-1R*VN0[3:0])/130R
VGAMMAN1	non	VGS2+ΔVDHN(130R-1R*VN0[5:0])/130R
VGAMMAN2	non	VGS2+ΔVDHN(130R-1R*VN0[5:0])/130R
VGAMMAN3	variable	VGAMMAN4+(VGAMMN2-VGAMMAN4)*JAN[1:0]
VGAMMAN4	variable	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((40R-1R*VN4[3:0])/47R)
VGAMMAN5	variable	VGAMMAN6+(VGAMMN4-VGAMMAN6)*JAN[1:0]
VGAMMAN6	variable	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((45R-1R*VN6[4:0])/47R)
VGAMMAN7	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN8	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN9	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN10	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN11	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN12	variable	VGAMMAN13+(VGAMMN6-VGAMMAN13)*JAN[1:0]
VGAMMAN13	variable	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((17R-1R*VN13[3:0])/47R)
VGAMMAN14	1.4R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(7R)/(8.4R)
VGAMMAN15	1.4R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(5.6R)/(8.4R)
VGAMMAN16	1.2R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(4.4R)/(8.4R)
VGAMMAN17	1.2R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(3.2R)/(8.4R)
VGAMMAN18	1.2R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(2R)/(8.4R)
VGAMMAN19	1R	VGAMMAN20+(VGAMMN13-VGAMMAN20)*(1R)/(8.4R)
VGAMMAN20	1R	VGS2+ΔVDHN(130R-1R*VN20 [6:0])/130R : VN20 [6:0] = 0~63 VGS2+ΔVDHN(129R-1R*VN20 [6:0])/130R : VN20 [6:0] = 64~127
VGAMMAN21	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(7.2R)/(8.4R)
VGAMMAN22	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(6R)/(8.4R)
VGAMMAN23	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(4.8R)/(8.4R)
VGAMMAN24	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(3.6R)/(8.4R)
VGAMMAN25	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(2.4R)/(8.4R)
VGAMMAN26	1.2R	VGAMMAN27+(VGAMMN20-VGAMMAN27)*(1.2R)/(8.4R)
VGAMMAN27	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((32R-1R*VN27[3:0])/39R)
VGAMMAN28	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(9.6R)/(10.8R)
VGAMMAN29	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(8.4R)/(10.8R)
VGAMMAN30	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(7.2R)/(10.8R)
VGAMMAN31	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(6R)/(10.8R)
VGAMMAN31	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(4.8R)/(10.8R)
VGAMMAN33	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(3.6R)/(10.8R)
VGAMMAN34	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(2.4R)/(10.8R)

VGAMMAN35	1.2R	VGAMMAN36+(VGAMMN27-VGAMMAN36)*(1.2R)/(10.8R)
VGAMMAN36	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((16R-1R*VN36[3:0])/39R)
VGAMMAN31	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(7.2R)/(8.4R)
VGAMMAN38	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(6R)/(8.4R)
VGAMMAN39	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(4.8R)/(8.4R)
VGAMMAN40	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(3.6R)/(8.4R)
VGAMMAN41	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(2.4R)/(8.4R)
VGAMMAN42	1.2R	VGAMMAN43+(VGAMMN36-VGAMMAN43)*(1.2R)/(8.4R)
VGAMMAN43	1.2R	VGS2+ΔVDHN(130R-1R*VN43 [6:0])/130R : VN43 [6:0] = 0~63 VGS2+ΔVDHN(129R-1R*VN43 [6:0])/130R : VN43 [6:0] = 64~127
VGAMMAN44	1R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(7.4R)/(8.4R)
VGAMMAN45	1R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(6.4R)/(8.4R)
VGAMMAN46	1.2R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(5.2R)/(8.4R)
VGAMMAN47	1.2R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(4R)/(8.4R)
VGAMMAN48	1.2R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(2.8R)/(8.4R)
VGAMMAN49	1.4R	VGAMMAN50+(VGAMMN43-VGAMMAN50)*(1.4R)/(8.4R)
VGAMMAN50	1.4R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((40R-1R*VN50[3:0])/47R)
VGAMMAN51	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN52	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN53	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN54	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN55	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN56	variable	VGAMMAN57+(VGAMMN50-VGAMMAN57)*JBN[1:0]
VGAMMAN57	variable	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((31R-1R*VN57[3:0])/47R)
VGAMMAN58	variable	VGAMMAN59+(VGAMMN57-VGAMMAN59)*JBN[1:0]
VGAMMAN59	variable	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((21R-1R*VN59[3:0])/47R)
VGAMMAN60	variable	VGAMMAN61+(VGAMMN59-VGAMMAN61)*JBN[1:0]
VGAMMAN61	variable	VGS2+ΔVDHN(65R-1R*VN61[5:0])/130R
VGAMMAN62	non	VGS2+ΔVDHN(65R-1R*VN62[5:0])/130R
VGAMMAN63	non	VGS2+ΔVDHN(23R-1R*VN63[3:0])/130R

11.2. Gamma Curves

Gamma Curve 2.2 (GC0), applies the function $y=x^{2.2}$



12. Reset

12.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's D5=0:00EF h If MADCTL's D5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's D5 = 0:013F h If MADCTL's D5=1:00EF h
Gamma Setting	GC0(Gamma 2.2)	GC0(Gamma 2.2)	GC0(Gamma 2.2)
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	00EF h	00EF h	00EF h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI *& IOVCC are applied.*

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

12.2. Output Pins, I/O Pins

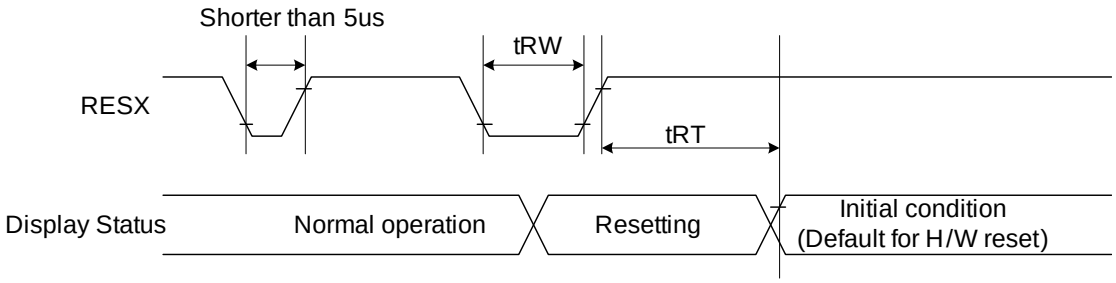
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

12.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

12.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

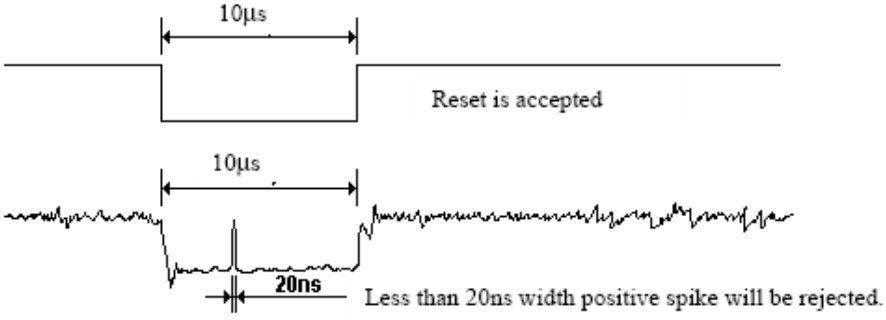
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



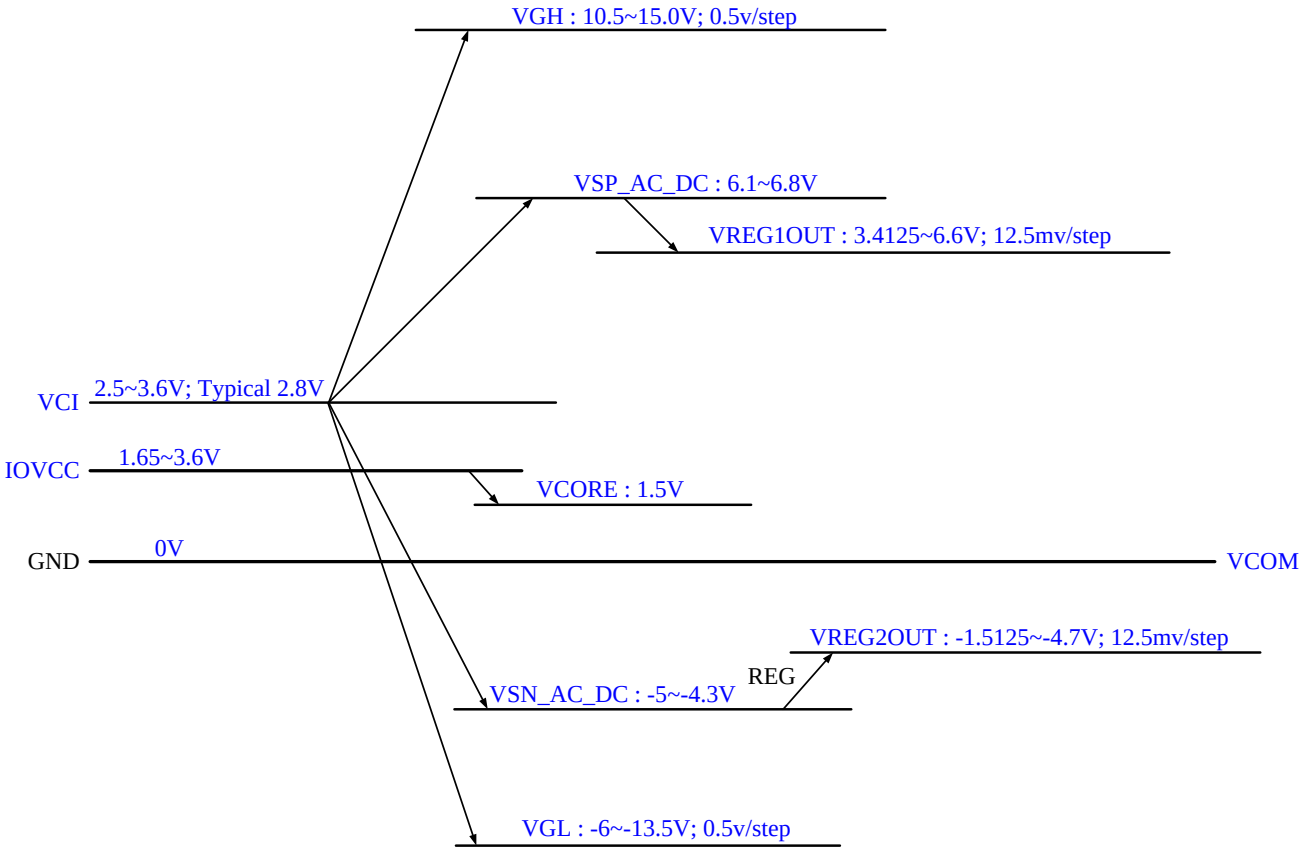
Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

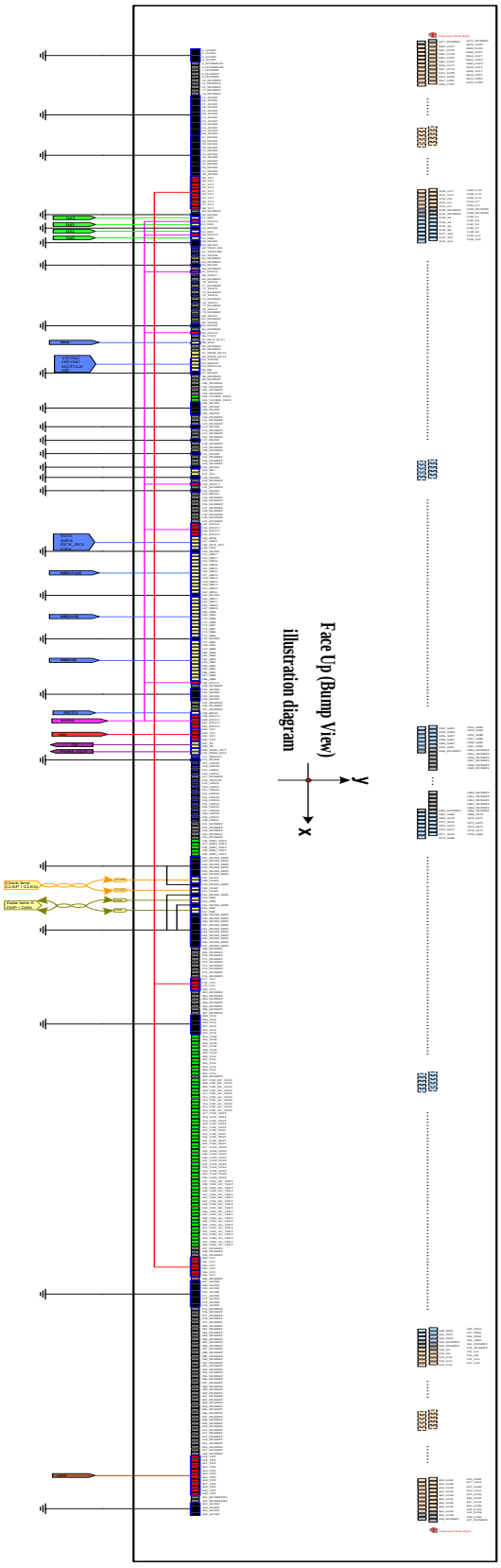
Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

13. Application Circuit

13.1. Power Structure

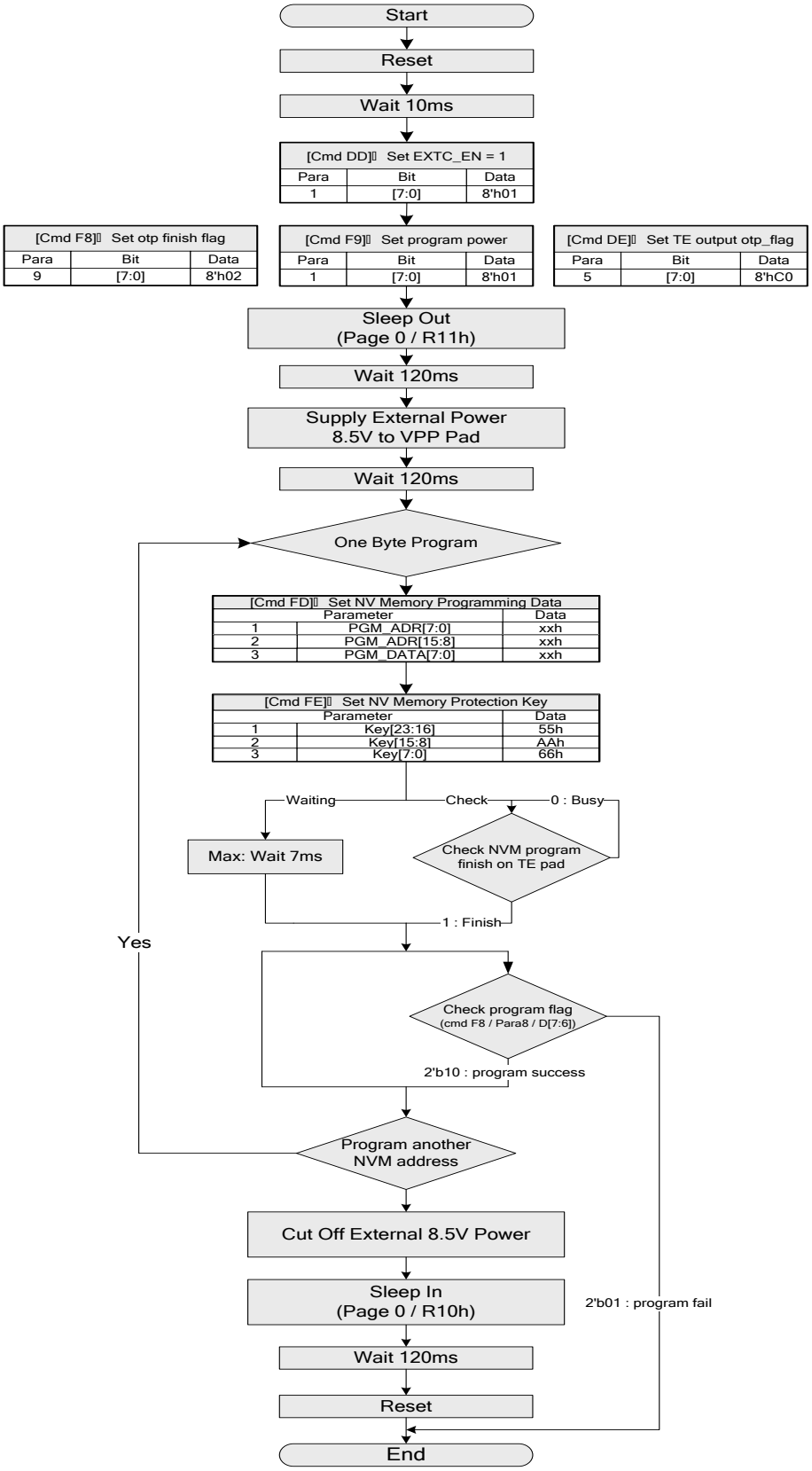


13.2. Configuration of Power Supply Circuit



The above figure shows the ILI9342E's power supply circuit. No capacitor and diode are needed in ILI9342E.

14. NV Memory Programming Flow



15. Electrical Characteristics

15.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9342E is used out of the absolute maximum ratings, ILI9342E may be permanently damaged. To use ILI9342E within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9342E will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +3.6
Supply voltage (Logic)	IOVCC	V	-0.3 ~ +3.6
OTP supply voltage	VPP-AGND	V	-0.3 ~ +8.5
Driver supply voltage	VGH-VGL	V	-0.3 ~ +30.0
Logic input voltage range	VIN	V	-0.3 ~ IOVCC
Logic output voltage range	VO	V	-0.3 ~ IOVCC
Operating temperature	Topr	℃	-30 ~ +70
Storage temperature	Tstg	℃	-55 ~ +110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

15.2. DC Characteristics

15.2.1. General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.6	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	1.8	3.6	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.5	-	15.0	Note3
Gate Driver Low Voltage	VGL	V	-	-10.5	-	-6.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	-	-	30.0	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	GND	-	0.3*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	GND	-	0.2*IOVCC	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or GND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM Amplitude	VCOMA	V	-		GND		Note3
Source Driver							
Source Output Range	Vsout	V	-	VREG2OUT	-	VREG1OUT	Note4
Source Output Deviation	V_{DEV}	V	-	TBD	-	TBD	-
Source Output Offset	V_{OFFSET}	V	-	TBD	-	TBD	-
Current consumption during sleep in mode operation (MIPI Interface)							
IOVCC_Sleep in mode current	I_{STB}	uA	IOVCC=1.8V T=*25°C*	-	18	TBD	-
VCI_Sleep in mode current	I_{STB}	uA	VCI=2.8V T=*25°C*	-	40	TBD	-
Current consumption during sleep in mode operation (Other Interface)							
IOVCC_Sleep in mode current	I_{STB}	uA	IOVCC=1.8V T=*25°C*	-	18	TBD	-
VCI_Sleep in mode current	I_{STB}	uA	IOVCC=1.8V T=*25°C*	-	1	TBD	-

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 3.6V, AGND=GND=0V, Ta=25°C

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], DCX_SCL, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

15.3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

Note: *Ta = -30℃ to 70℃ (to +85℃ no damage)*

15.3.1. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Notes:

1.Ta = -30℃ to 70℃ (to +85℃ no damage)

2. DSI High Speed mode is off.

15.3.2. Spike/Glitch Rejection

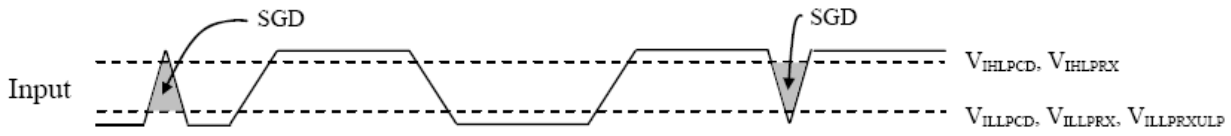


Figure 74: Spike/Glitch Rejection

Notes:

1. *A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and Interference Frequency is 450MHz (at the very least).*

Table 34: Spike/Glitch Rejection

Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N, D0P/N	SGD	Input pulse rejection for DSI	-	300	Vps

15.3.3. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	D0P/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	D0P/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	D0P/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	D0P/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	D0P/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, D0P/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, D0P/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, D0P/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, D0P/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, D0P/N Note 5, Note 6	-	-	14	pF

Notes:

1. Ta = -30℃ to 70℃ (to +85℃ no damage) , VCI = 2.5V to 3.6V, VDDI = 1.65V to 3.6V

2. Includes 50mV (-50mV to 50mV) ground difference

3. Without VCMRCLKM450/VCMRDATAM450

4. Without 50mV (-50mV to 50mV) ground difference

5. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than VTHH (CLKP/D0P). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than VTHL (CLKN/D0N). There is undefined state if the differential voltage is less than VTHH (CLKP/D0P) and less than VTHL (CLKN/D0N). A reference figure is below.

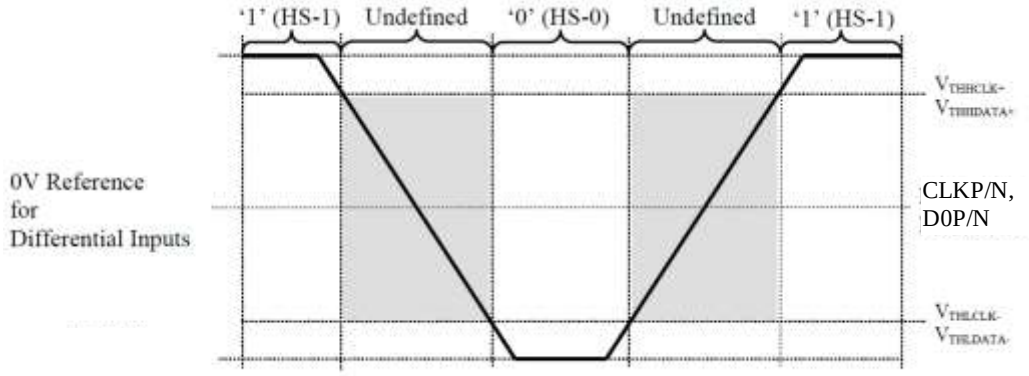


Figure 75: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range

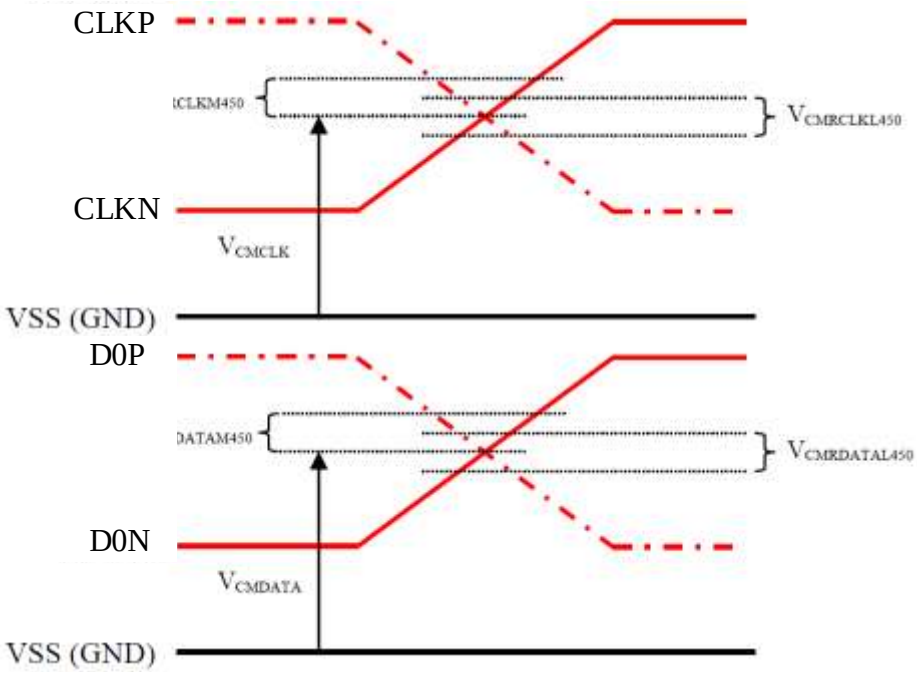


Figure 76: Common Mode Voltage on Clock and Data Channels

The termination resistor (RTERM) of the differential DSI receiver can be driven to two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

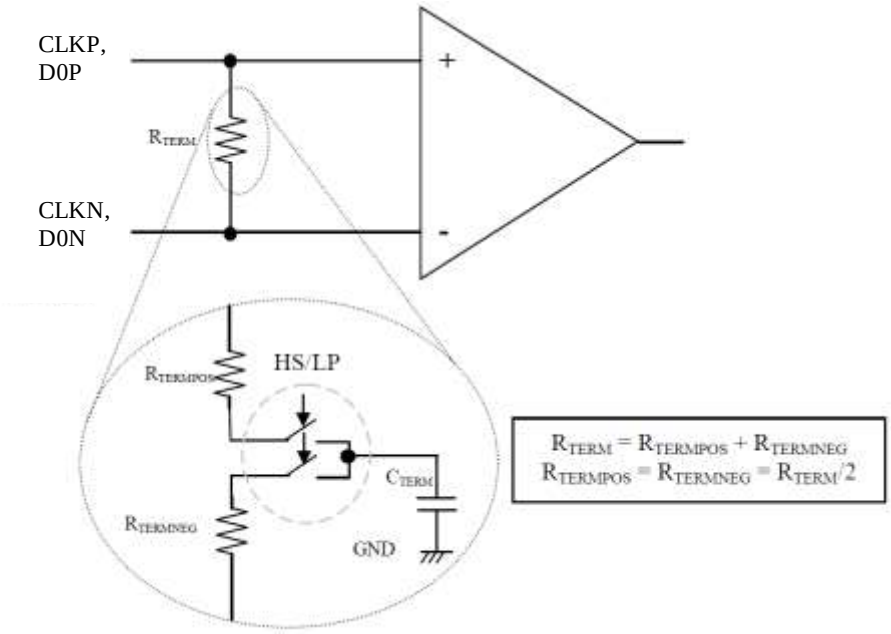
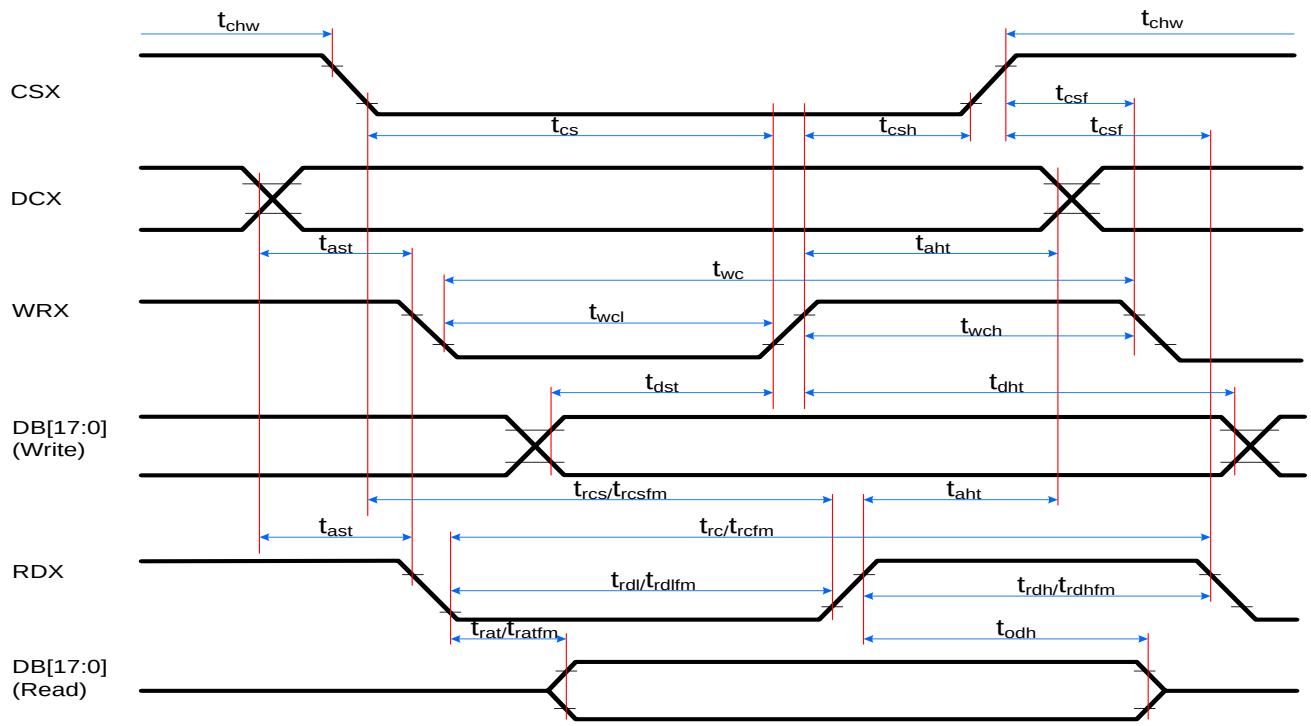


Figure 77: Differential Pair Termination Resistor on the Receiver Side

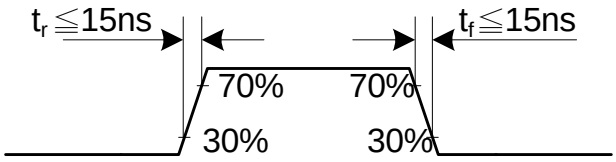
15.4. AC Characteristics

15.4.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅰ system)

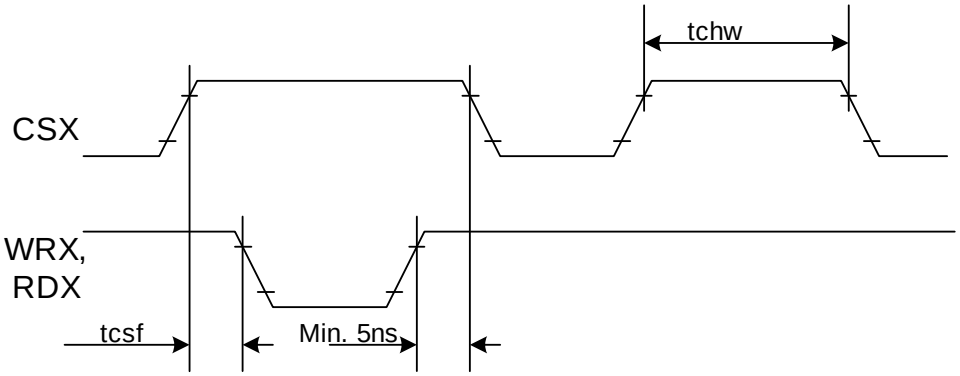


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, GND=0V

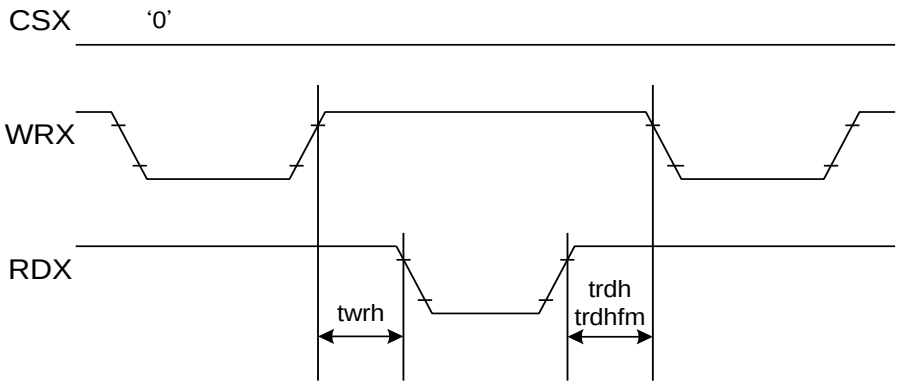


CSX timings :



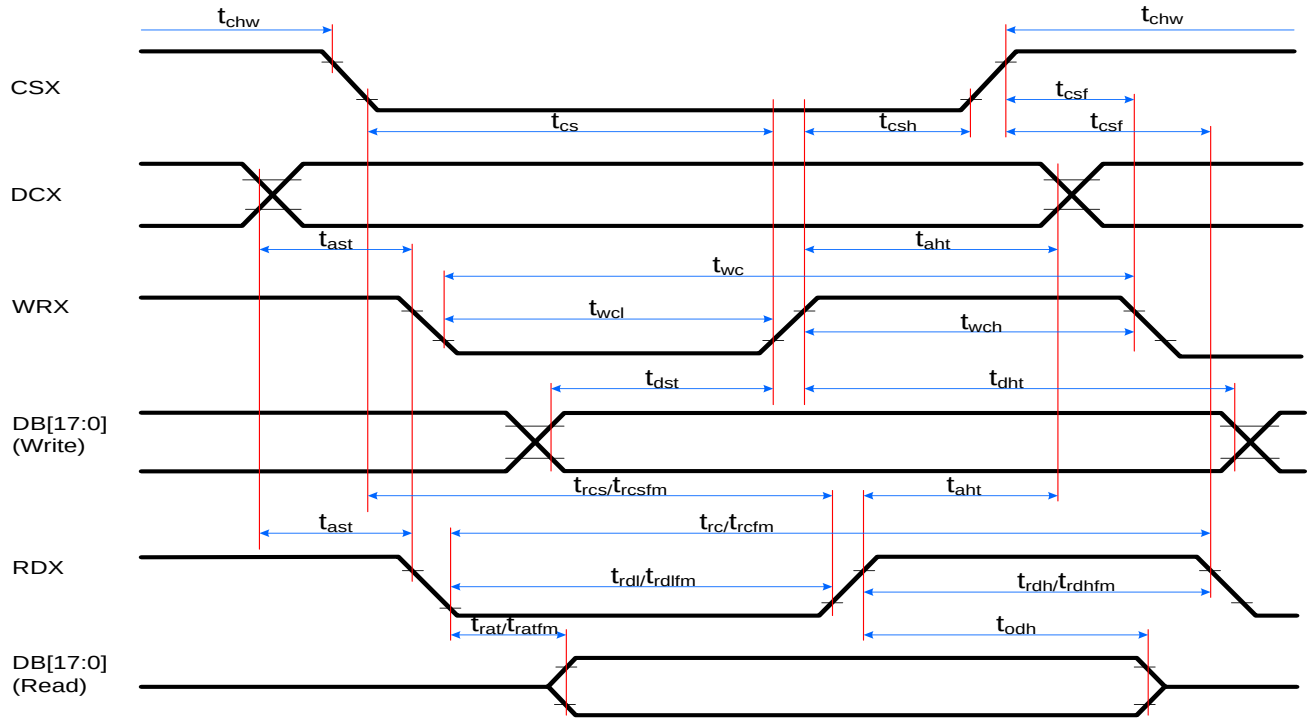
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



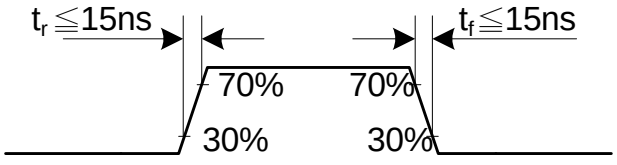
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

15.4.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)

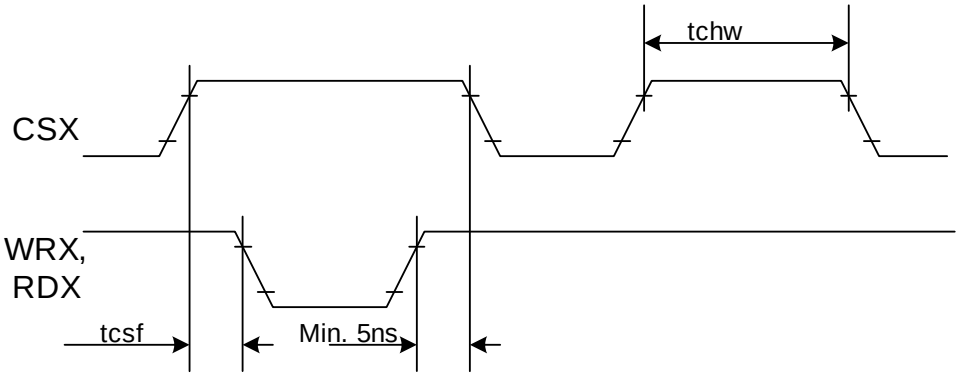


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = 25°C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, GND=0V.

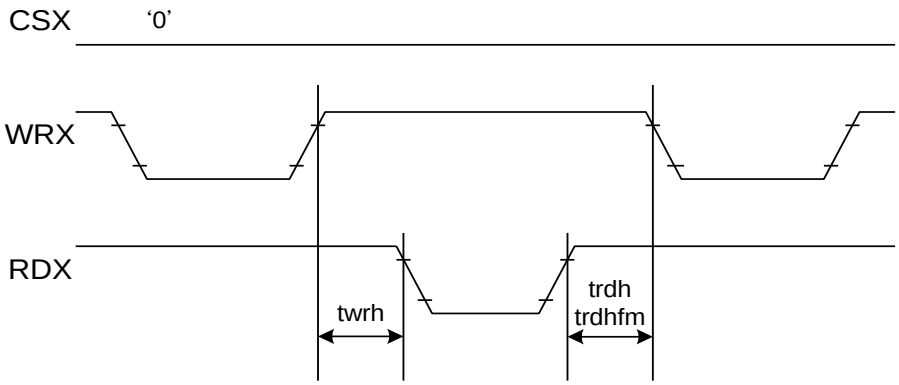


CSX timins :



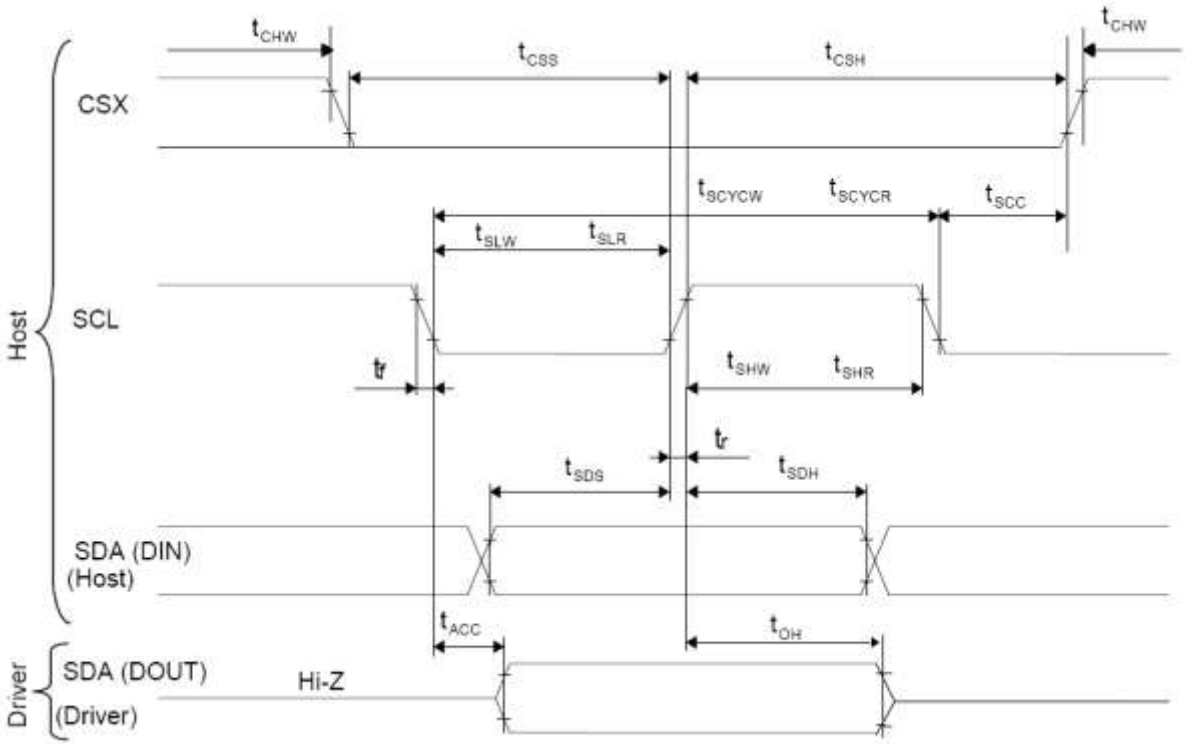
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



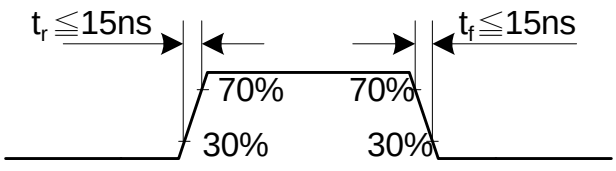
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

15.4.3. Display Serial Interface Timing Characteristics (3-line SPI system)

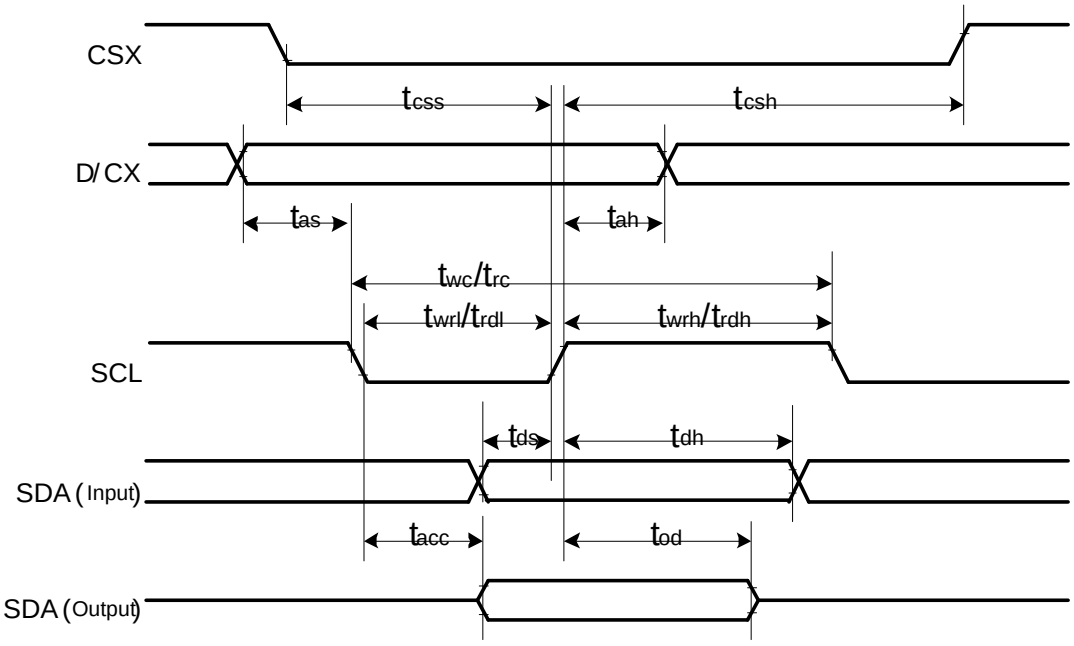


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	35	-	ns	
	tslw	SCL "L" Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time(write)	30	-	ns	
	tcsh		30	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=GND=0V

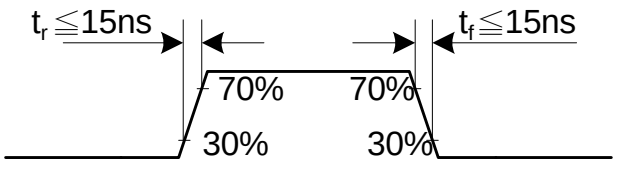


15.4.4. Display Serial Interface Timing Characteristics (4-line SPI system)

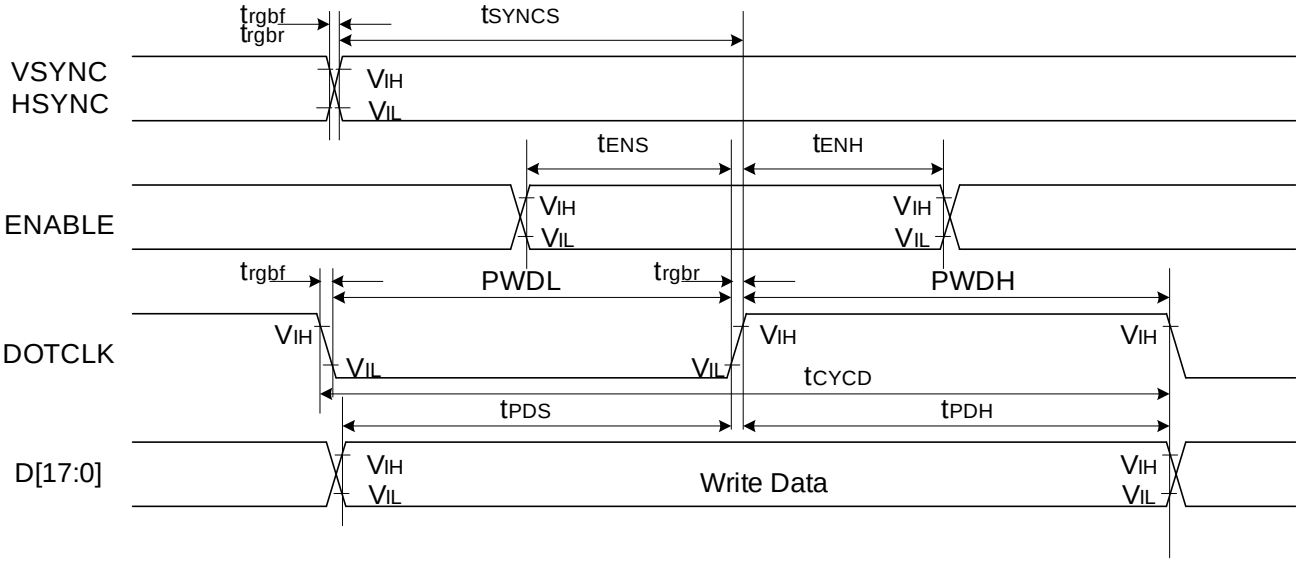


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	30	-	ns	
	tcsh	Chip select hold time (write)	30	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	35	-	ns	
	twrl	SCL “L” pulse width (Write)	35	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	-	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=GND=0V

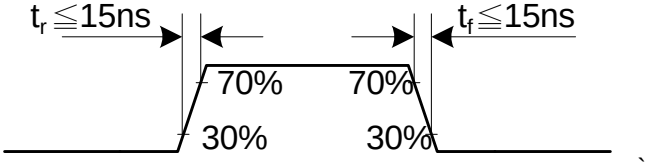


15.4.5. Parallel 18/16/8/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	8/6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=GND=0V



15.4.6. DSI Timing Characteristics

15.4.6.1. High Speed Mode – Clock Channel Timing

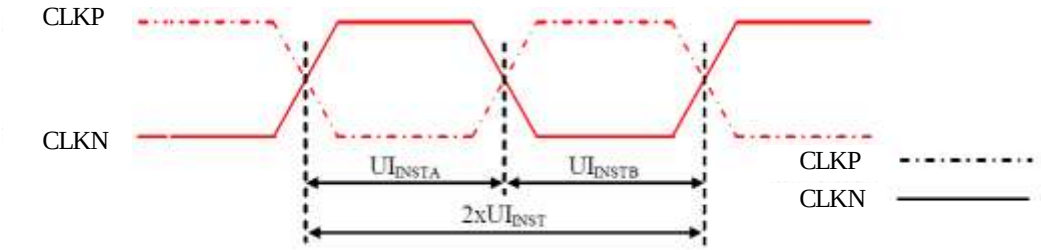


Figure 78: DSI Clock Channel Timing

Table 35: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*11.12*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*5.56*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 36.

Table 36: Limited Clock Channel Speed

Data type	One Lane speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	180 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	180 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	180 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	180 Mbps

15.4.6.2. High Speed Mode – Data Clock Channel Timing

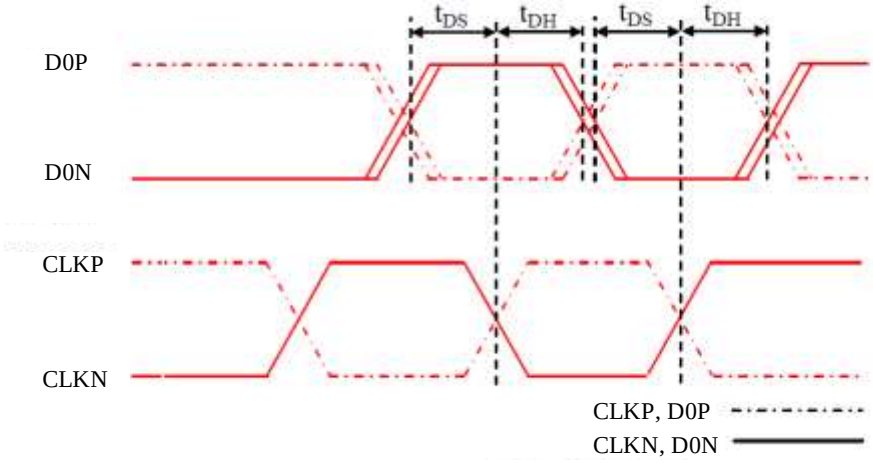


Figure 79: DSI Data to Clock Channel Timings

Table 37: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
D0P/N	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

15.4.6.3. High Speed Mode – Rising and Falling Timings

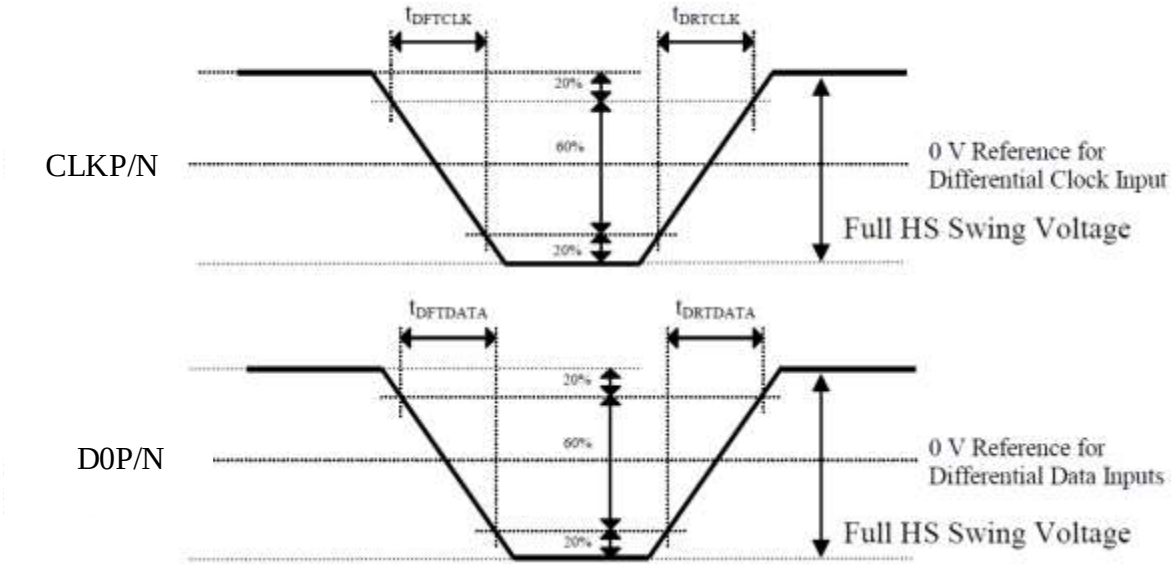


Figure 80: Rising and Falling Timings on Clock and Data Channels

Table 38: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	D0P/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	D0P/N	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

15.4.6.4. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9342E) are illustrated for reference purposes below.

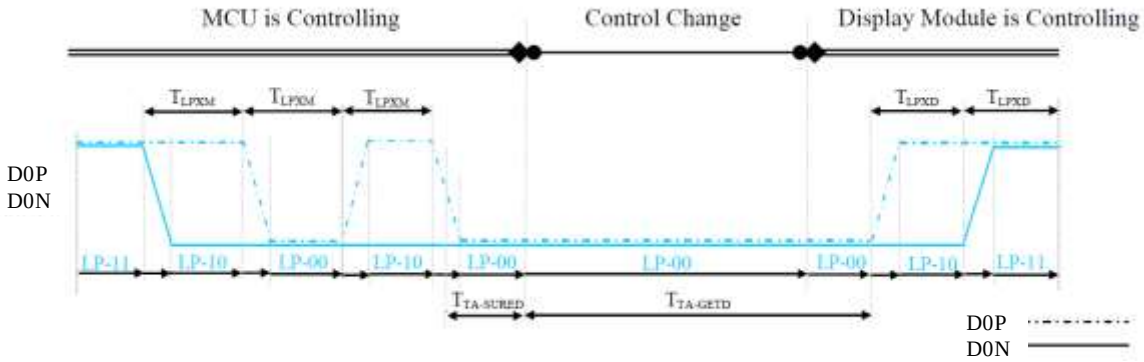


Figure 81: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9342E) to the MCU are illustrated for reference purposes below.

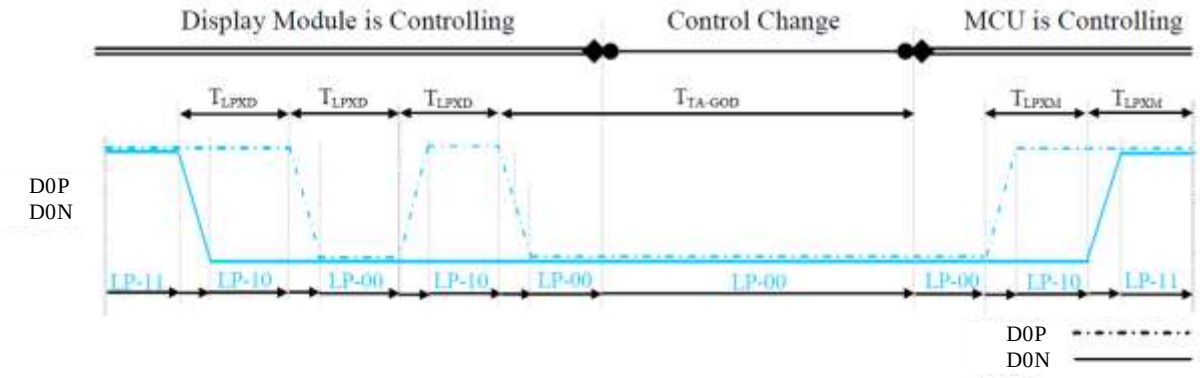


Figure 82: BTA from the Display Module to the MCU

Table 39: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9342E)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9342E) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9342E) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 40: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9342E)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

15.4.6.5. Data Lanes from Low Power Mode to High Speed Mode

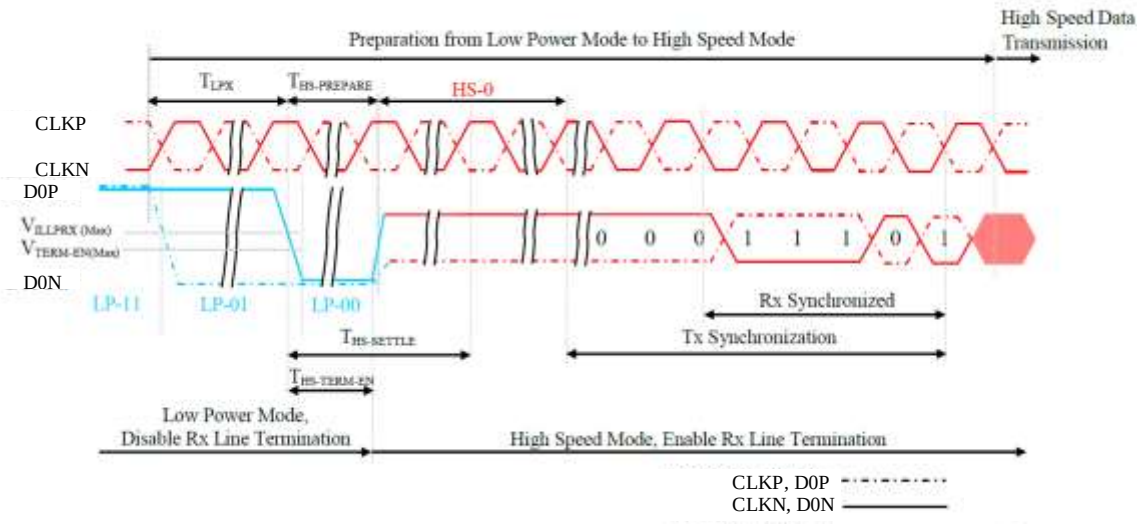


Figure 83: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 41: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPX}	Length of any Low Power State Period	50	-	ns
D0P/N	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
D0P/N	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

15.4.6.6. Data Lanes from High Speed Mode to Low Power Mode

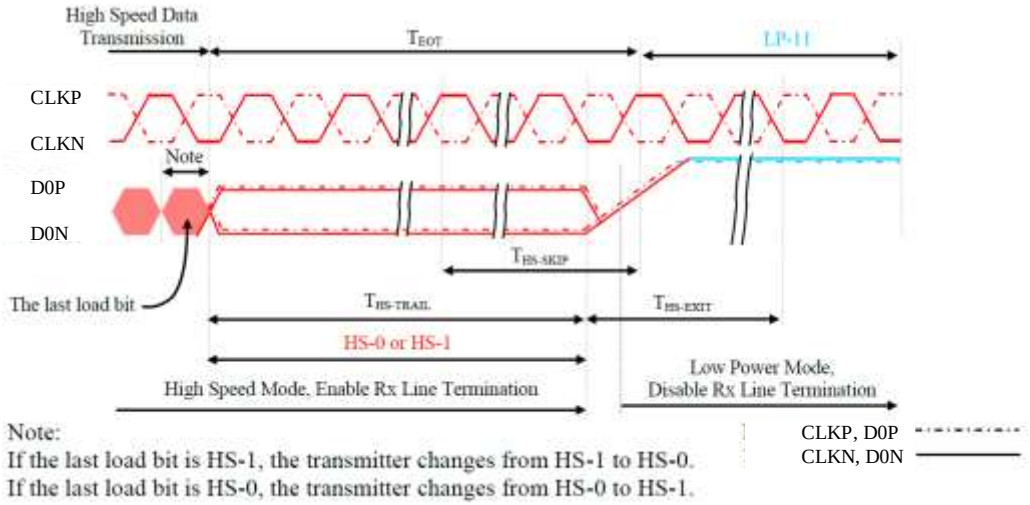


Figure 84: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 42: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
D0P/N	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9342E) to ignore transition period of EoT	40	55+4xUI	ns
D0P/N	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

15.4.6.7. DSI Clock Burst – High Speed Mode to/from Low Power Mode

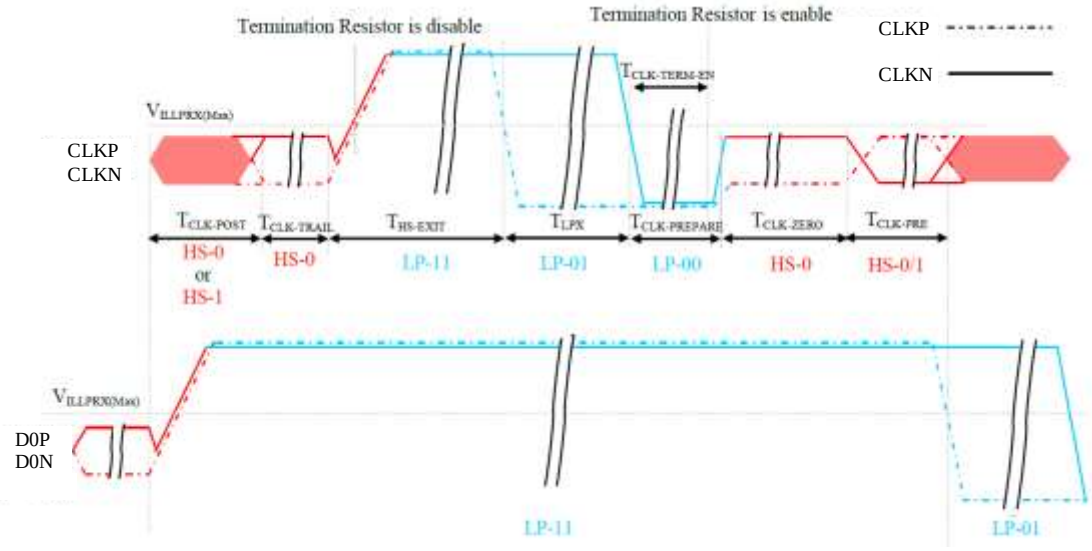
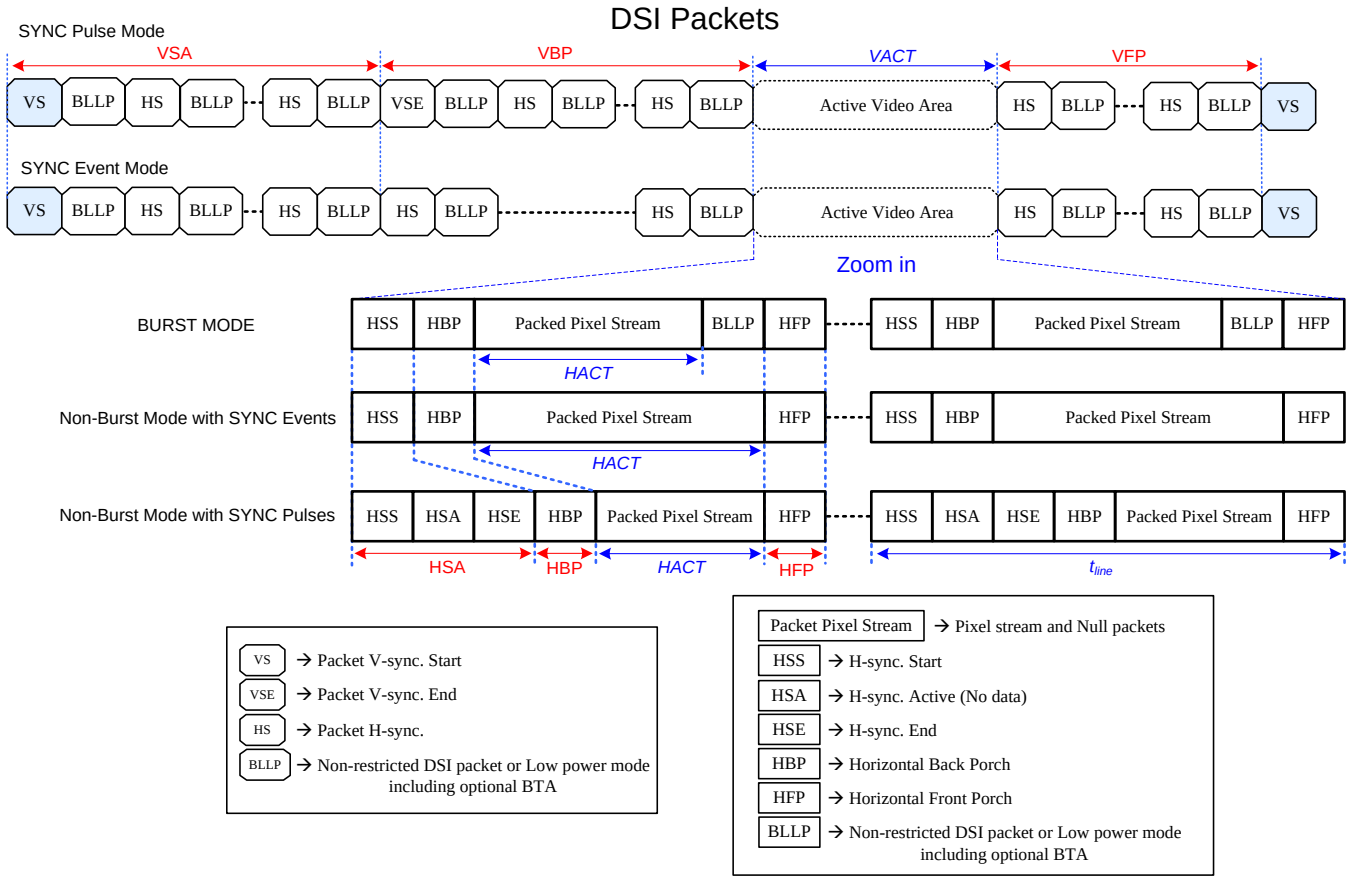


Figure 85: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 43: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

15.4.7. Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	1 (Note 6)	-	-	Line
Vertical Back Porch	VBP	2 (Note 6)	-	-	Line
Vertical Front Porch	VFP	2 (Note 6)	-	-	Line
Active lines per frame	VACT	-	240	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	4	-	-	us
Active pixels per line	HACT	-	320	-	Pixel
Bit rate	BR_{bps}	180		Note 5	Mbps/lane

1 UI=1/Bit rate

HAS(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 180Mbps/lane, 1UI=5.6ns, Frame rate=60Hz, VACT=240, VSA=1, VBP=7, VFP=8, HACT=320, HSA+HBP+HFP=256, $Lane_{num}$=1(lane), Pixel Format=18(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to "4.4DSI System Interface".
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to "Table 36: Limited Clock Channel Speed".
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

16. Maximum Layout Resistance

Pad Name	Type	Maximum Series Resistance	Unit
IOVCC	Power	5	Ω
VCI	Power	5	Ω
AGND	Ground	5	Ω
DGND	Ground	5	Ω
VGS	Ground	10	Ω
DGND_MIPI	Ground	5	Ω
VGH	Analog	100	Ω
VGL	Analog	100	Ω
MIPI_TEST	Analog	100	Ω
VCORE_TEST	Analog	100	Ω
VSP_DC_TEST	Analog	100	Ω
VSN_DC_TEST	Analog	100	Ω
VAP_TEST	Analog	100	Ω
VAN_TEST	Analog	100	Ω
VSP_AC_TEST	Analog	100	Ω
VSN_AC_TEST	Analog	100	Ω
VPP	Power	10	Ω
IM[3:0]	Input	50	Ω
RESX	Input	50	Ω
CSX	Input	50	Ω
DCX_SCL	Input	50	Ω
RDX	Input	50	Ω
WRX	Input	50	Ω
D[17:0]	Input / Output	50	Ω
SDA	Input / Output	50	Ω
TE	Output	50	Ω
TE1	Output	50	Ω
DOTCLK	Input	50	Ω
VSYNC	Input	50	Ω
HSYNC	Input	50	Ω
DE	Input	50	Ω
CLKP/N	Input	5	Ω
D0P/N	Input / Output	5	Ω

PWM_OUT	Output	50	Ω
PWM_OUT1	Output	50	Ω
RESX1 CSX1 DCX_SCL1	Input	50	Ω
TEST_EN TESTOSC	Input	50	Ω
TEST0~8	Input	50	Ω
TESTO1~O2	Input / Output	50	Ω
GPIO0~7	Input / Output	50	Ω

17. Revision History

Version No.	Date	Page	Description
V100	2019/08/16	All	New created